

## Automotive P-Channel 12 V (D-S) 175 °C MOSFET

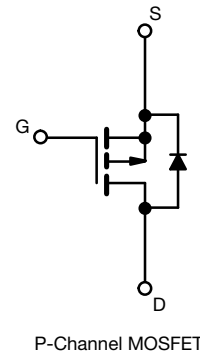
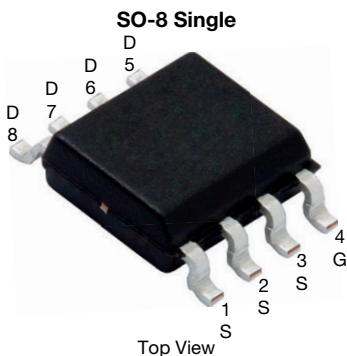
 AUTOMOTIVE  
GRADE

**RoHS**  
COMPLIANT  
HALOGEN  
**FREE**

PRODUCT SUMMARY	
$V_{DS}$ (V)	-12
$R_{DS(on)}$ ( $\Omega$ ) at $V_{GS} = -4.5$ V	0.00832
$R_{DS(on)}$ ( $\Omega$ ) at $V_{GS} = -2.5$ V	0.01000
$R_{DS(on)}$ ( $\Omega$ ) at $V_{GS} = -1.8$ V	0.01430
$I_D$ (A)	-25
Configuration	Single
Package	SO-8

### FEATURES

- TrenchFET® power MOSFET
- AEC-Q101 qualified
- 100 %  $R_g$  and UIS tested
- Material categorization:  
for definitions of compliance please see  
[www.vishay.com/doc?99912](http://www.vishay.com/doc?99912)



ABSOLUTE MAXIMUM RATINGS ( $T_C = 25$ °C, unless otherwise noted)				
PARAMETER		SYMBOL	LIMIT	UNIT
Drain-Source Voltage		$V_{DS}$	-12	V
Gate-Source Voltage		$V_{GS}$	$\pm 8$	
Continuous Drain Current <sup>a</sup>	$T_C = 25$ °C	$I_D$	-25	A
	$T_C = 125$ °C		-14	
Continuous Source Current (Diode Conduction) <sup>a</sup>		$I_S$	-6.5	
Pulsed Drain Current <sup>b</sup>		$I_{DM}$	-100	
Single Pulse Avalanche Current	L = 0.1 mH	$I_{AS}$	-19	
Single Pulse Avalanche Energy		$E_{AS}$	18	
Maximum Power Dissipation <sup>b</sup>	$T_C = 25$ °C	$P_D$	7.1	W
	$T_C = 125$ °C		2.3	
Operating Junction and Storage Temperature Range		$T_J, T_{stg}$	-55 to +175	°C

THERMAL RESISTANCE RATINGS				
PARAMETER		SYMBOL	LIMIT	UNIT
Junction-to-Ambient	PCB Mount <sup>c</sup>	$R_{thJA}$	85	°C/W
Junction-to-Foot (Drain)		$R_{thJF}$	21	

### Notes

- Package limited.
- Pulse test; pulse width  $\leq 300$   $\mu$ s, duty cycle  $\leq 2$  %.
- When mounted on 1" square PCB (FR4 material).



SPECIFICATIONS ( $T_C = 25\text{ }^\circ\text{C}$ , unless otherwise noted)							
PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
<b>Static</b>							
Drain-Source Breakdown Voltage	$V_{DS}$	$V_{GS} = 0, I_D = -250\text{ }\mu\text{A}$		-12	-	-	V
Gate-Source Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = -250\text{ }\mu\text{A}$		-0.4	-0.6	-0.9	
Gate-Source Leakage	$I_{GSS}$	$V_{DS} = 0\text{ V}, V_{GS} = \pm 8\text{ V}$		-	-	$\pm 100$	nA
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{GS} = 0\text{ V}$	$V_{DS} = -12\text{ V}$	-	-	-1	$\mu\text{A}$
		$V_{GS} = 0\text{ V}$	$V_{DS} = -12\text{ V}, T_J = 125\text{ }^\circ\text{C}$	-	-	-50	
		$V_{GS} = 0\text{ V}$	$V_{DS} = -12\text{ V}, T_J = 175\text{ }^\circ\text{C}$	-	-	-150	
On-State Drain Current <sup>a</sup>	$I_{D(on)}$	$V_{GS} = -4.5\text{ V}$	$V_{DS} \geq -5\text{ V}$	-30	-	-	A
Drain-Source On-State Resistance <sup>a</sup>	$R_{DS(on)}$	$V_{GS} = -4.5\text{ V}$	$I_D = -14\text{ A}$	-	0.00510	0.00832	$\Omega$
		$V_{GS} = -4.5\text{ V}$	$I_D = -14\text{ A}, T_J = 125\text{ }^\circ\text{C}$	-	-	0.00900	
		$V_{GS} = -4.5\text{ V}$	$I_D = -14\text{ A}, T_J = 175\text{ }^\circ\text{C}$	-	-	0.01100	
		$V_{GS} = -2.5\text{ V}$	$I_D = -13\text{ A}$	-	0.00650	0.01000	
		$V_{GS} = -1.8\text{ V}$	$I_D = -12\text{ A}$	-	0.00940	0.01430	
Forward Transconductance <sup>a</sup>	$g_{fs}$	$V_{DS} = -6\text{ V}, I_D = -10.5\text{ A}$		-	54	-	S
<b>Dynamic <sup>b</sup></b>							
Input Capacitance	$C_{iss}$	$V_{GS} = 0\text{ V}$	$V_{DS} = -6\text{ V}, f = 1\text{ MHz}$	-	7500	11 000	$\mu\text{F}$
Output Capacitance	$C_{oss}$			-	2800	4200	
Reverse Transfer Capacitance	$C_{rss}$			-	2400	3600	
Total Gate Charge <sup>c</sup>	$Q_g$	$V_{GS} = -4.5\text{ V}$	$V_{DS} = -6\text{ V}, I_D = -10.5\text{ A}$	-	101	151	nC
Gate-Source Charge <sup>c</sup>	$Q_{gs}$			-	15	-	
Gate-Drain Charge <sup>c</sup>	$Q_{gd}$			-	45	-	
Gate Resistance	$R_g$	$f = 1\text{ MHz}$		1.1	2.2	3.2	$\Omega$
Turn-On Delay Time <sup>c</sup>	$t_{d(on)}$	$V_{DD} = -6\text{ V}, R_L = 15\text{ }\Omega$ $I_D \cong -10.5\text{ A}, V_{GEN} = -4.5\text{ V}, R_g = 6\text{ }\Omega$		-	31	42	ns
Rise Time <sup>c</sup>	$t_r$			-	168	224	
Turn-Off Delay Time <sup>c</sup>	$t_{d(off)}$			-	310	412	
Fall Time <sup>c</sup>	$t_f$			-	283	376	
<b>Source-Drain Diode Ratings and Characteristics <sup>b</sup></b>							
Pulsed Current <sup>a</sup>	$I_{SM}$			-	-	-100	A
Forward Voltage	$V_{SD}$	$I_F = -10.5\text{ A}, V_{GS} = 0$		-	-0.8	-1.2	V

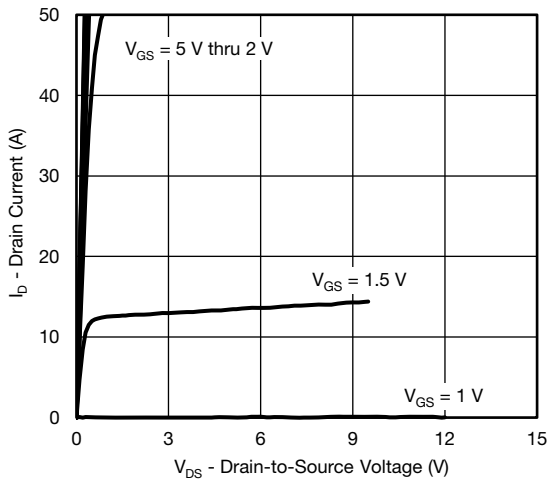
**Notes**

- Pulse test; pulse width  $\leq 300\text{ }\mu\text{s}$ , duty cycle  $\leq 2\%$ .
- Guaranteed by design, not subject to production testing.
- Independent of operating temperature.

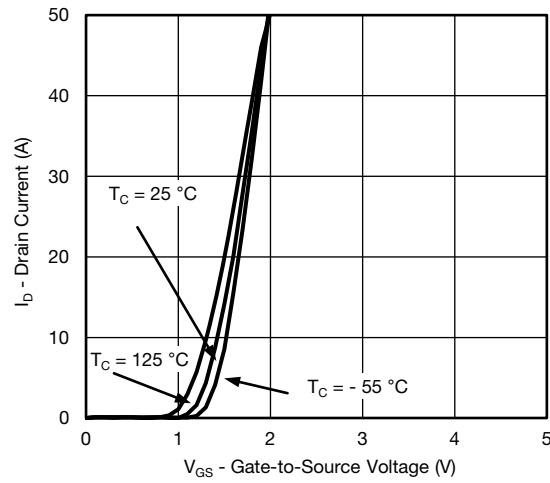
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.



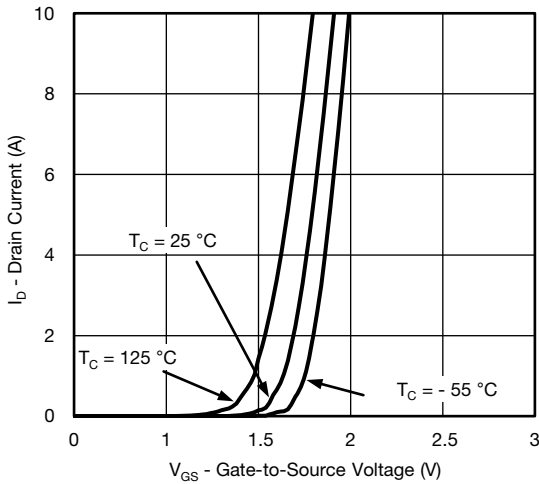
**TYPICAL CHARACTERISTICS** ( $T_A = 25\text{ }^\circ\text{C}$ , unless otherwise noted)



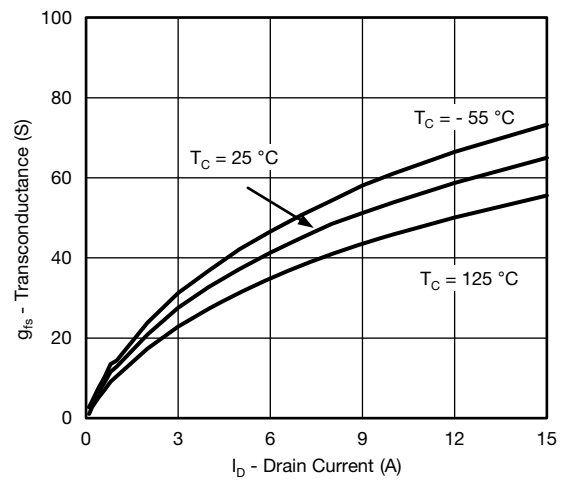
**Output Characteristics**



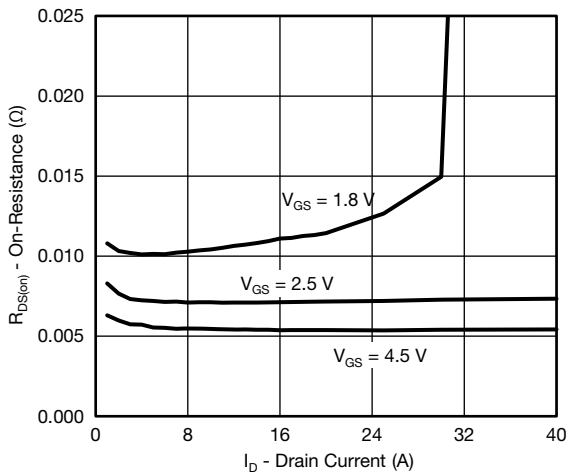
**Transfer Characteristics**



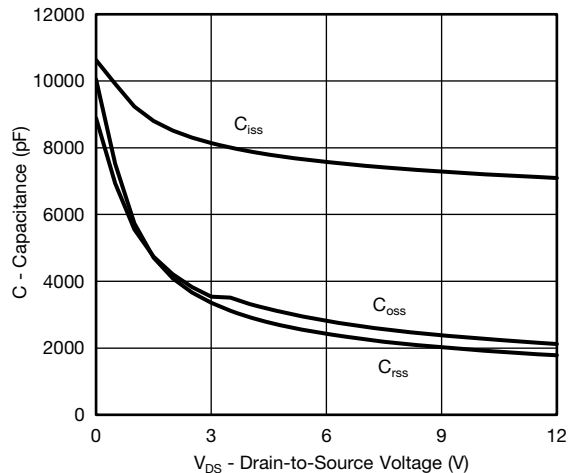
**Transfer Characteristics**



**Transconductance**

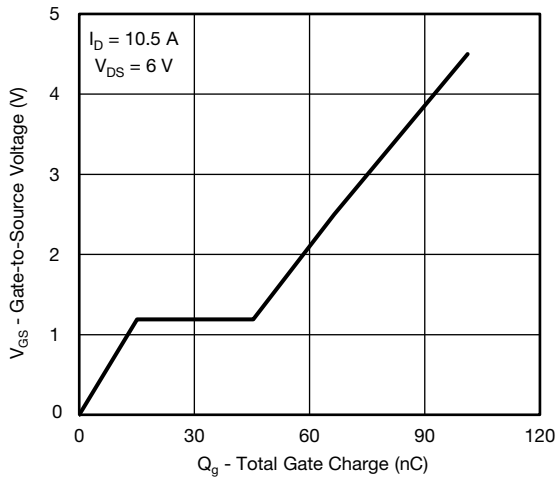


**On-Resistance vs. Drain Current**

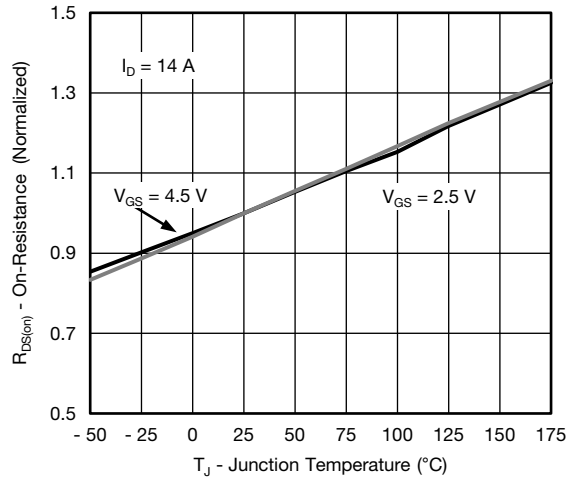


**Capacitance**

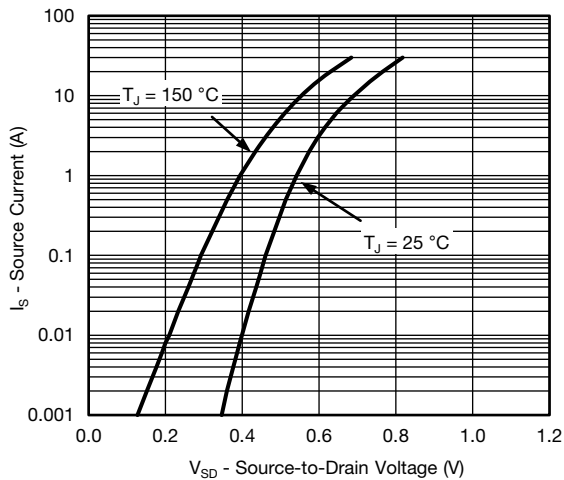
**TYPICAL CHARACTERISTICS** ( $T_A = 25\text{ }^\circ\text{C}$ , unless otherwise noted)



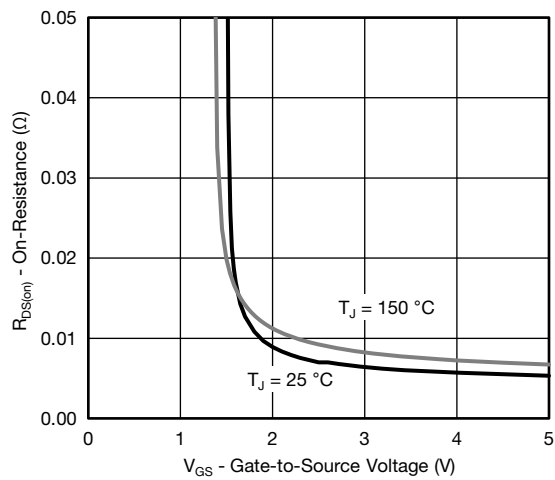
**Gate Charge**



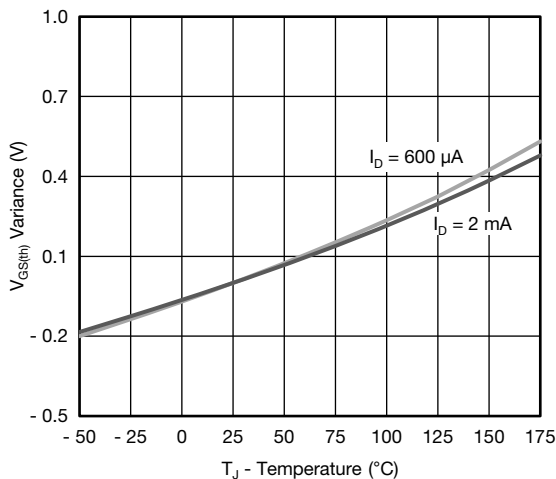
**On-Resistance vs. Junction Temperature**



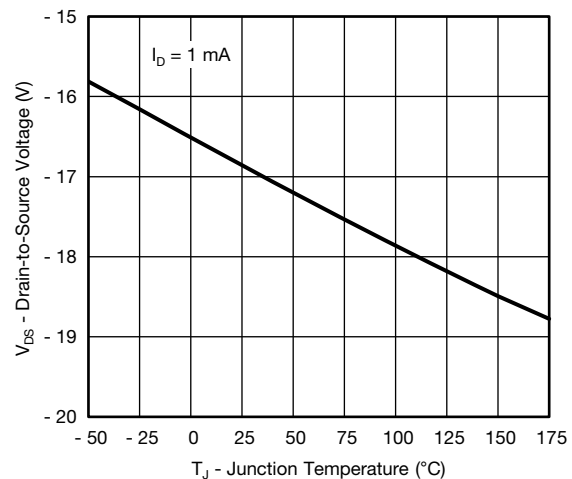
**Source Drain Diode Forward Voltage**



**On-Resistance vs. Gate-to-Source Voltage**

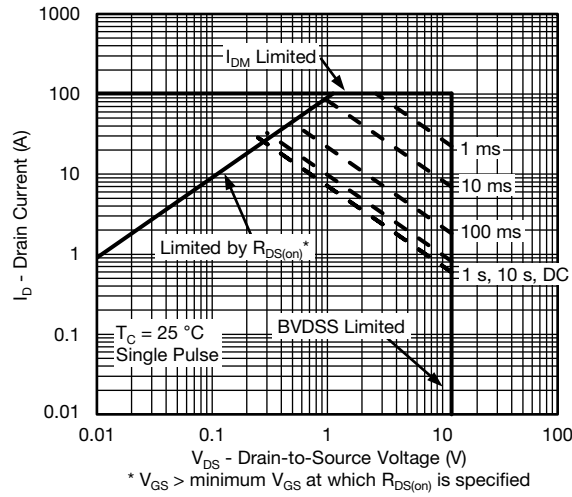


**Threshold Voltage**

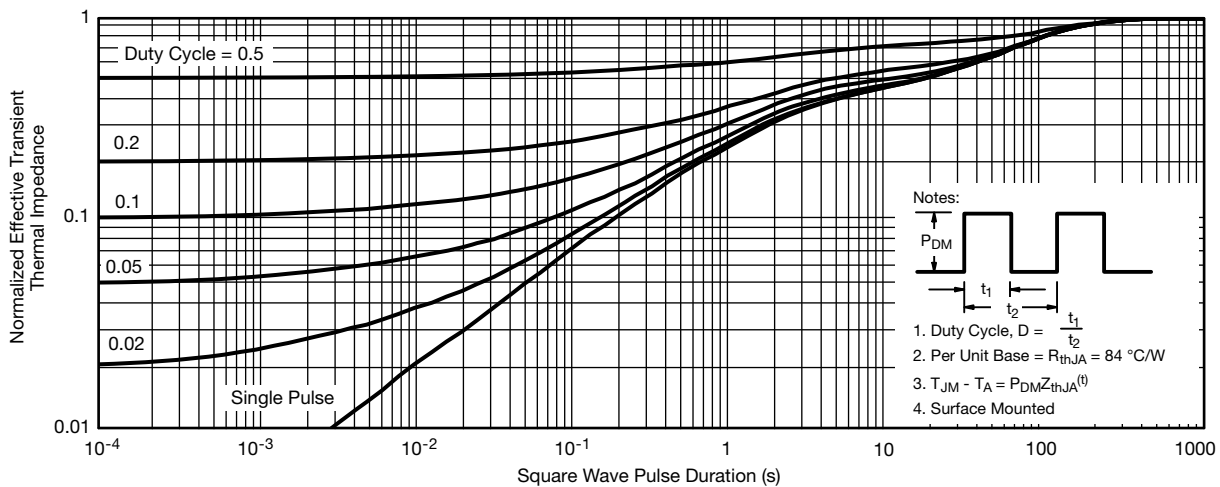


**Breakdown Voltage vs. Junction Temperature**

**THERMAL RATINGS** ( $T_A = 25\text{ }^\circ\text{C}$ , unless otherwise noted)



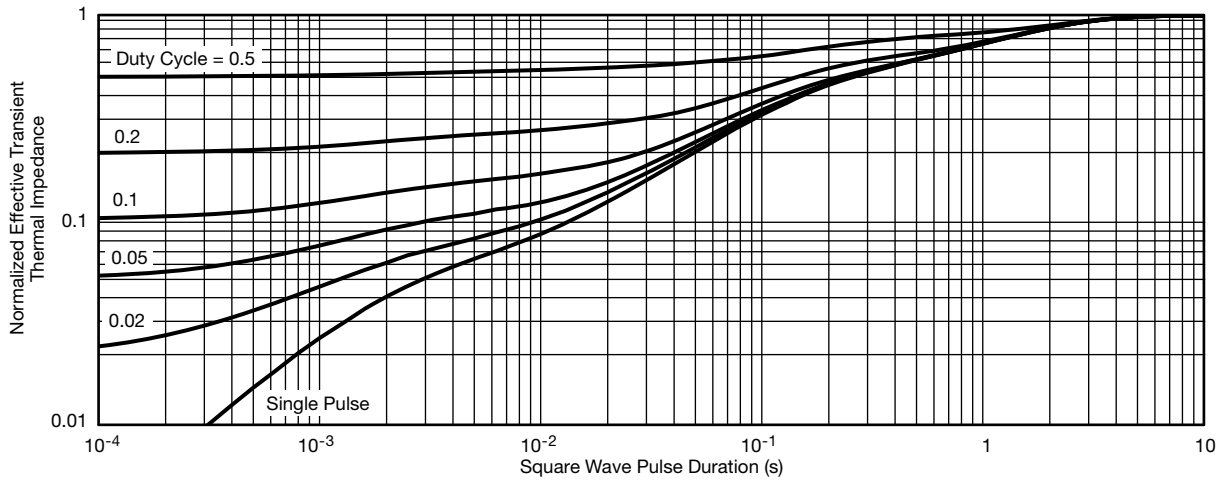
**Safe Operating Area**



**Normalized Thermal Transient Impedance, Junction-to-Ambient**



**THERMAL RATINGS** ( $T_A = 25\text{ }^\circ\text{C}$ , unless otherwise noted)



**Normalized Thermal Transient Impedance, Junction-to-Foot**

**Note**

- The characteristics shown in the two graphs
    - Normalized Transient Thermal Impedance Junction-to-Ambient (25 °C)
    - Normalized Transient Thermal Impedance Junction-to-Foot (25 °C)
- are given for general guidelines only to enable the user to get a “ball park” indication of part capabilities. The data are extracted from single pulse transient thermal impedance characteristics which are developed from empirical measurements. The latter is valid for the part mounted on printed circuit board - FR4, size 1" x 1" x 0.062", double sided with 2 oz. copper, 100 % on both sides. The part capabilities can widely vary depending on actual application parameters and operating conditions.

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<b>REVISION HISTORY <sup>a</sup></b>		
<b>REVISION</b>	<b>DATE</b>	<b>DESCRIPTION OF CHANGE</b>
B	15-Jan-16	<ul style="list-style-type: none"><li>• Maximum on-resistance changed</li><li>• I<sub>GSS</sub> test condition changed</li></ul>

**Note**

a. As of April 2014

## SOIC (NARROW): 8-LEAD

JEDEC Part Number: MS-012



DIM	MILLIMETERS		INCHES	
	Min	Max	Min	Max
A	1.35	1.75	0.053	0.069
A <sub>1</sub>	0.10	0.20	0.004	0.008
B	0.35	0.51	0.014	0.020
C	0.19	0.25	0.0075	0.010
D	4.80	5.00	0.189	0.196
E	3.80	4.00	0.150	0.157
e	1.27 BSC		0.050 BSC	
H	5.80	6.20	0.228	0.244
h	0.25	0.50	0.010	0.020
L	0.50	0.93	0.020	0.037
q	0°	8°	0°	8°
S	0.44	0.64	0.018	0.026
ECN: C-06527-Rev. I, 11-Sep-06				
DWG: 5498				



## RECOMMENDED MINIMUM PADS FOR SO-8



Recommended Minimum Pads  
Dimensions in Inches/(mm)

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