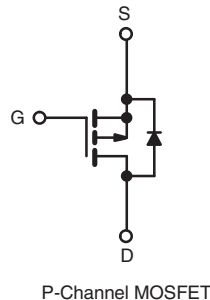
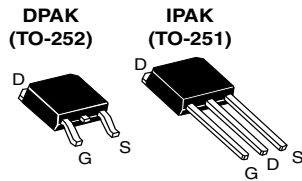


## Power MOSFET

PRODUCT SUMMARY	
$V_{DS}$ (V)	- 250
$R_{DS(on)}$ ( $\Omega$ )	$V_{GS} = - 10$ V   3.0
$Q_g$ (Max.) (nC)	14
$Q_{gs}$ (nC)	3.1
$Q_{gd}$ (nC)	6.8
Configuration	Single



P-Channel MOSFET

### FEATURES

- P-Channel
- Surface Mount (IRFR9214, SiHFR9214)
- Straight Lead (IRFU9214, SiHFU9214)
- Advanced Process Technology
- Fast Switching
- Fully Avalanche Rated
- Material categorization: For definitions of compliance please see [www.vishay.com/doc?99912](http://www.vishay.com/doc?99912)



RoHS  
COMPLIANT  
HALOGEN  
**FREE**  
Available

### DESCRIPTION

Third generation power MOSFETs from Vishay utilize advanced processing techniques to achieve low on-resistance per silicon area. This benefit, combined with the fast switching speed and ruggedized device design that power MOSFETs are well known for, provides the designer with an extremely efficient and reliable device for use in a wide variety of applications.

The DPAK is designed for surface mounting using vapor phase, infrared, or wave soldering techniques. The straight lead version (IRFU, SiHFU series) is for through-hole mounting applications. Power dissipation levels up to 1.5 W are possible in typical surface mount applications.

ORDERING INFORMATION				
Package	DPAK (TO-252)	DPAK (TO-252)	DPAK (TO-252)	IPAK (TO-251)
Lead (Pb)-free and Halogen-free	SiHFR9214-GE3	SiHFR9214TRL-GE3	SiHFR9214TR-GE3	SiHFU9214-GE3
Lead (Pb)-free	IRFR9214PbF	IRFR9214TRLPbF <sup>a</sup>	IRFR9214TRPbF <sup>a</sup>	IRFU9214PbF
	SiHFR9214-E3	SiHFR9214TL-E3 <sup>a</sup>	SiHFR9214T-E3 <sup>a</sup>	SiHFU9214-E3

#### Note

- a. See device orientation.

ABSOLUTE MAXIMUM RATINGS ( $T_C = 25$ °C, unless otherwise noted)					
PARAMETER	SYMBOL		LIMIT	UNIT	
Drain-Source Voltage	$V_{DS}$		- 250	V	
Gate-Source Voltage	$V_{GS}$		$\pm 20$		
Continuous Drain Current	$V_{GS}$ at - 10 V	$T_C = 25$ °C	- 2.7	A	
		$T_C = 100$ °C	- 1.7		
Pulsed Drain Current <sup>a</sup>	$I_{DM}$		- 11		
Linear Derating Factor			0.40	W/°C	
Single Pulse Avalanche Energy <sup>b</sup>	$E_{AS}$		100	mJ	
Repetitive Avalanche Current <sup>a</sup>	$I_{AR}$		- 2.7	A	
Repetitive Avalanche Energy <sup>a</sup>	$E_{AR}$		5.0	mJ	
Maximum Power Dissipation	$T_C = 25$ °C		$P_D$	50	W
Peak Diode Recovery $dV/dt$ <sup>c</sup>	$dV/dt$		- 5.0	V/ns	
Operating Junction and Storage Temperature Range	$T_J, T_{stg}$		- 55 to + 150	°C	
Soldering Recommendations (Peak Temperature) <sup>d</sup>	for 10 s		260		

#### Notes



- a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).  
 b. Starting  $T_J = 25$  °C,  $L = 27$  mH,  $R_g = 25$   $\Omega$ ,  $I_{AS} = - 2.7$  A (see fig. 12).  
 c.  $I_{SD} \leq - 2.7$  A,  $dI/dt \leq 600$  A/ $\mu$ s,  $V_{DD} \leq V_{DS}$ ,  $T_J \leq 150$  °C.  
 d. 1.6 mm from case.



THERMAL RESISTANCE RATINGS					
PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Maximum Junction-to-Ambient	$R_{thJA}$	-	-	110	°C/W
Maximum Junction-to-Ambient (PCB Mount) <sup>a</sup>	$R_{thJA}$	-	-	50	
Maximum Junction-to-Case (Drain)	$R_{thJC}$	-	-	2.5	

**Note**

a. When mounted on 1" square PCB (FR-4 or G-10 material).

SPECIFICATIONS ( $T_J = 25\text{ }^\circ\text{C}$ , unless otherwise noted)							
PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
<b>Static</b>							
Drain-Source Breakdown Voltage	$V_{DS}$	$V_{GS} = 0\text{ V}, I_D = -250\text{ }\mu\text{A}$		- 250	-	-	V
$V_{DS}$ Temperature Coefficient	$\Delta V_{DS}/T_J$	Reference to $25\text{ }^\circ\text{C}$ , $I_D = -1\text{ mA}$		-	- 0.25	-	V/°C
Gate-Source Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = -250\text{ }\mu\text{A}$		- 2.0	-	- 4.0	V
Gate-Source Leakage	$I_{GSS}$	$V_{GS} = \pm 20\text{ V}$		-	-	$\pm 100$	nA
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS} = -250\text{ V}, V_{GS} = 0\text{ V}$		-	-	- 100	$\mu\text{A}$
		$V_{DS} = -200\text{ V}, V_{GS} = 0\text{ V}, T_J = 125\text{ }^\circ\text{C}$		-	-	- 500	
Drain-Source On-State Resistance	$R_{DS(on)}$	$V_{GS} = -10\text{ V}$	$I_D = -1.7\text{ A}^b$	-	-	3.0	$\Omega$
Forward Transconductance	$g_{fs}$	$V_{DS} = -50\text{ V}, I_D = -1.7\text{ A}$		0.9	-	-	S
<b>Dynamic</b>							
Input Capacitance	$C_{iss}$	$V_{GS} = 0\text{ V}, V_{DS} = -25\text{ V}, f = 1.0\text{ MHz}$ , see fig. 5		-	220	-	pF
Output Capacitance	$C_{oss}$			-	75	-	
Reverse Transfer Capacitance	$C_{rss}$			-	11	-	
Total Gate Charge	$Q_g$	$V_{GS} = -10\text{ V}$	$I_D = -1.7\text{ A}, V_{DS} = -200\text{ V}$ , see fig. 6 and 13 <sup>b</sup>	-	-	14	nC
Gate-Source Charge	$Q_{gs}$			-	-	3.1	
Gate-Drain Charge	$Q_{gd}$			-	-	6.8	
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = -125\text{ V}, I_D = -1.7\text{ A}, R_g = 21\text{ }\Omega, R_D = 70\text{ }\Omega$ , see fig. 10 <sup>b</sup>		-	11	-	ns
Rise Time	$t_r$			-	14	-	
Turn-Off Delay Time	$t_{d(off)}$			-	20	-	
Fall Time	$t_f$			-	17	-	
Internal Drain Inductance	$L_D$	Between lead, 6 mm (0.25") from package and center of die contact 		-	4.5	-	nH
Internal Source Inductance	$L_S$			-	7.5	-	
<b>Drain-Source Body Diode Characteristics</b>							
Continuous Source-Drain Diode Current	$I_S$	MOSFET symbol showing the integral reverse p-n junction diode 		-	-	- 2.7	A
Pulsed Diode Forward Current <sup>a</sup>	$I_{SM}$			-	-	- 11	
Body Diode Voltage	$V_{SD}$	$T_J = 25\text{ }^\circ\text{C}, I_S = -2.7\text{ A}, V_{GS} = 0\text{ V}^b$		-	-	- 5.8	V
Body Diode Reverse Recovery Time	$t_{rr}$	$T_J = 25\text{ }^\circ\text{C}, I_F = -1.7\text{ A}, dI/dt = 100\text{ A}/\mu\text{s}^b$		-	150	220	ns
Body Diode Reverse Recovery Charge	$Q_{rr}$			-	870	1300	nC
Forward Turn-On Time	$t_{on}$	Intrinsic turn-on time is negligible (turn-on is dominated by $L_S$ and $L_D$ )					

**Notes**

- a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).
- b. Pulse width  $\leq 300\text{ }\mu\text{s}$ ; duty cycle  $\leq 2\text{ }\%$ .



## TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

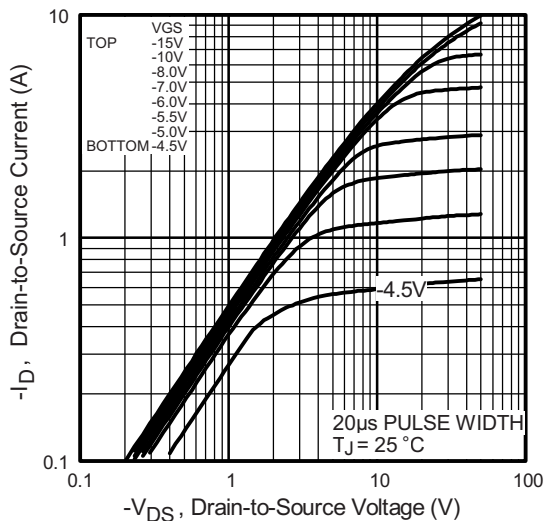


Fig. 1 - Typical Output Characteristics, T<sub>C</sub> = 25 °C

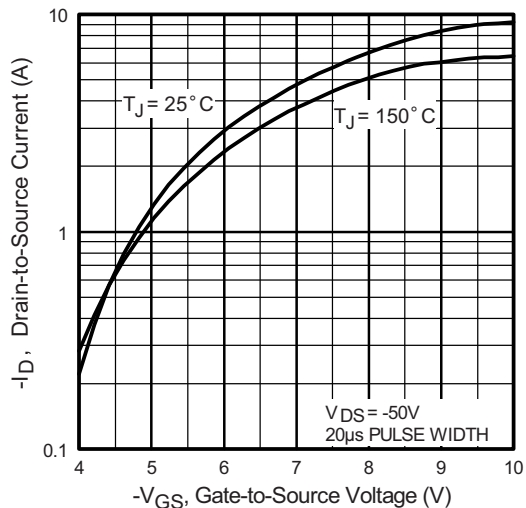


Fig. 3 - Typical Transfer Characteristics

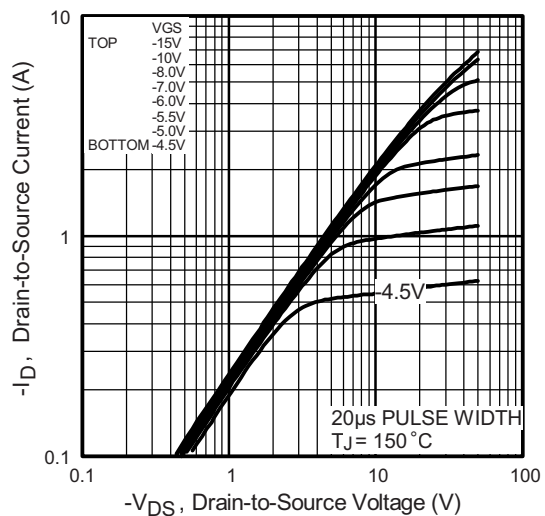


Fig. 2 - Typical Output Characteristics, T<sub>C</sub> = 150 °C

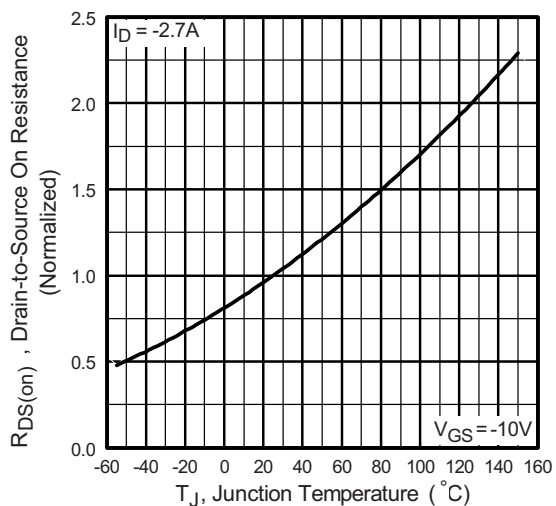


Fig. 4 - Normalized On-Resistance vs. Temperature

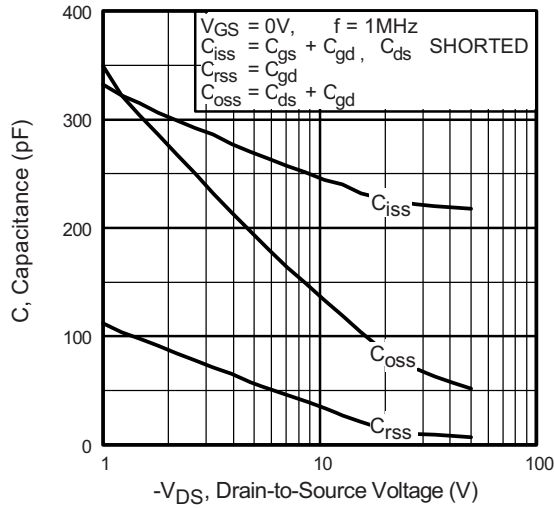


Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage

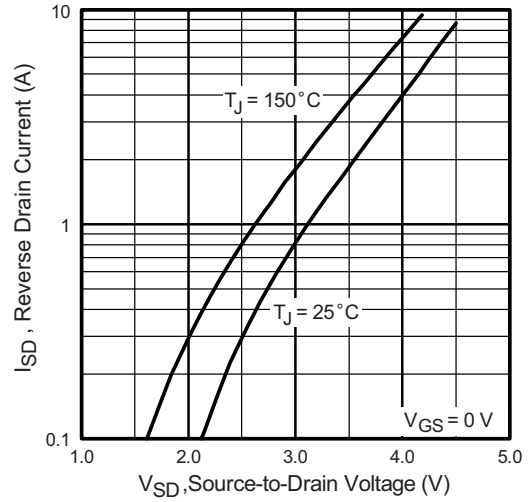


Fig. 7 - Typical Source-Drain Diode Forward Voltage

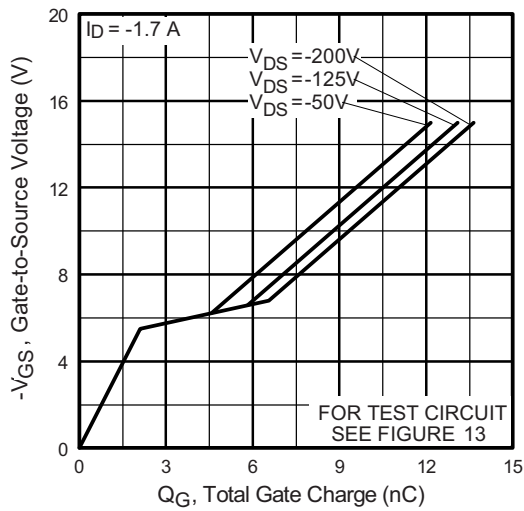


Fig. 6 - Typical Gate Charge vs. Gate-to-Source Voltage

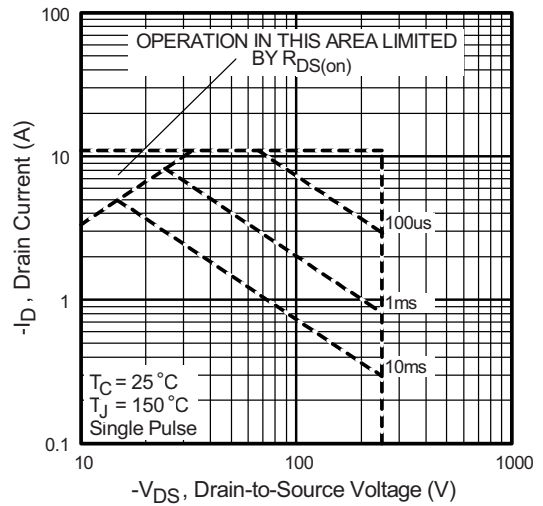


Fig. 8 - Maximum Safe Operating Area

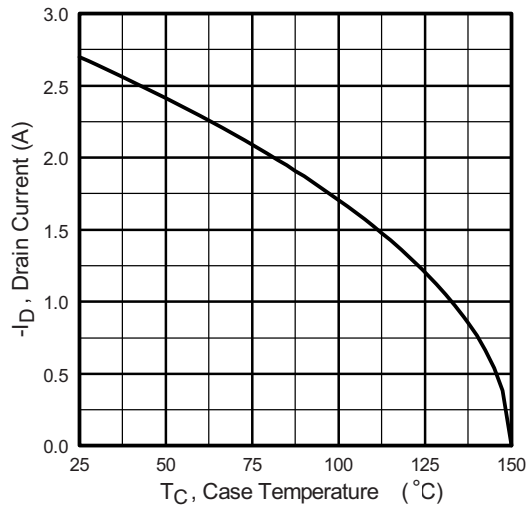


Fig. 9 - Maximum Drain Current vs. Case Temperature

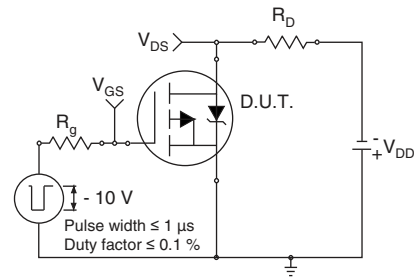


Fig. 10a - Switching Time Test Circuit

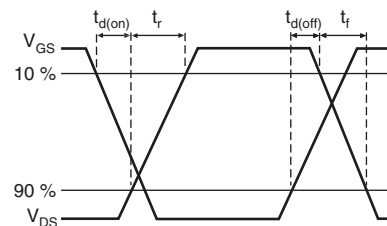


Fig. 10b - Switching Time Waveforms

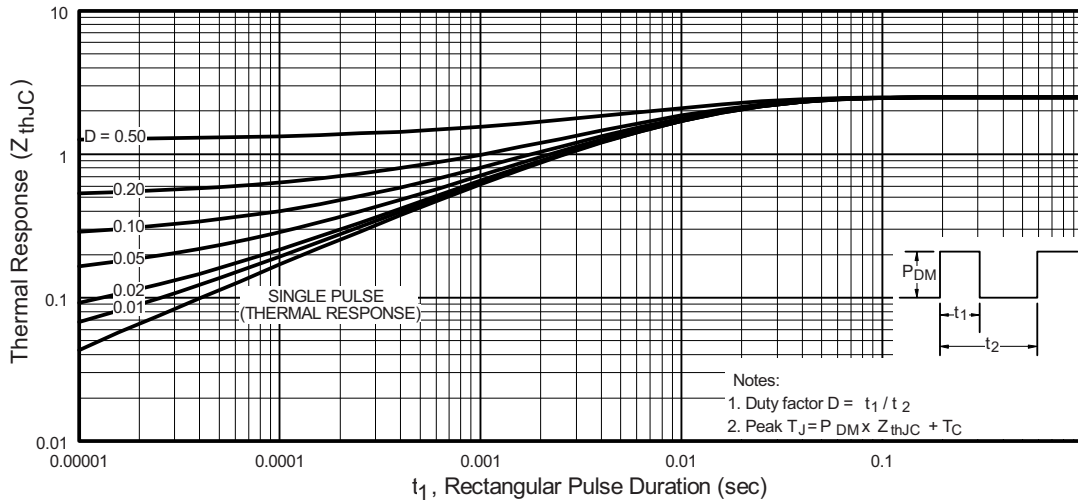


Fig. 11 - Maximum Effective Transient Thermal Impedance, Junction-to-Case

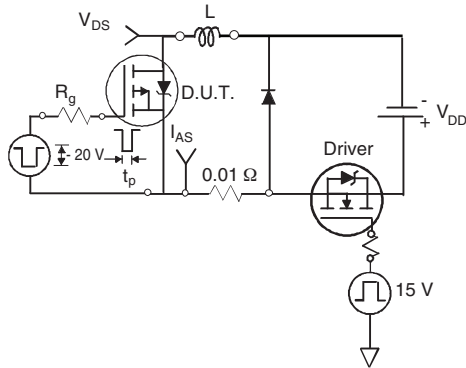


Fig. 12a - Unclamped Inductive Test Circuit

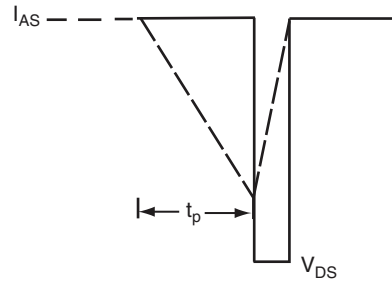


Fig. 12b - Unclamped Inductive Waveforms

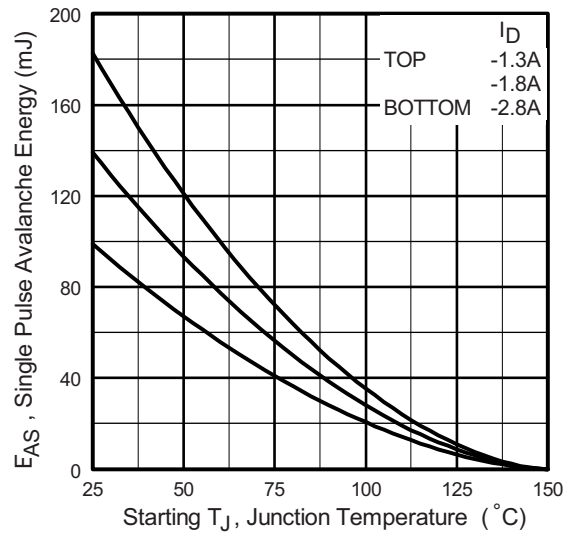


Fig. 12c - Maximum Avalanche Energy vs. Drain Current

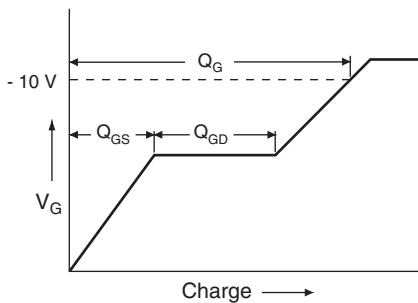


Fig. 13a - Basic Gate Charge Waveform

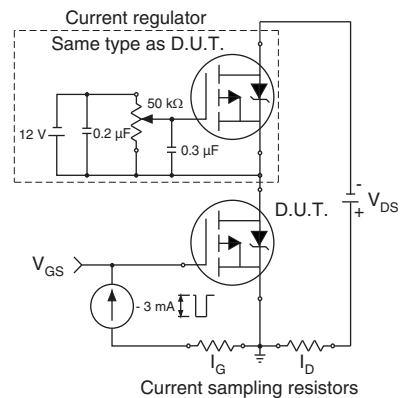
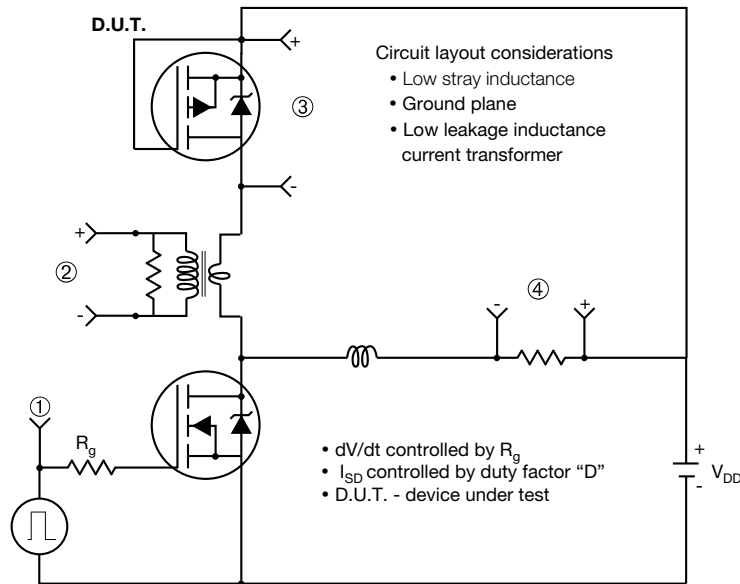


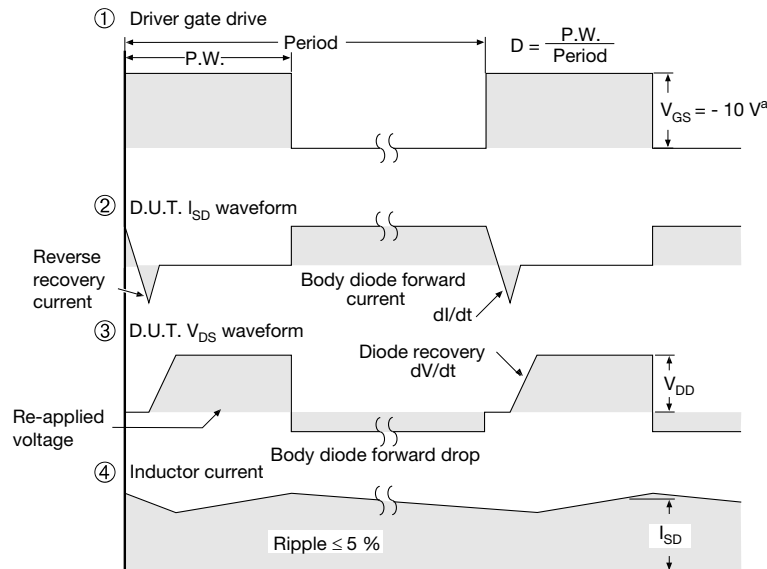
Fig. 13b - Gate Charge Test Circuit

### Peak Diode Recovery dV/dt Test Circuit



**Note**

- Compliment N-Channel of D.U.T. for driver



**Note**

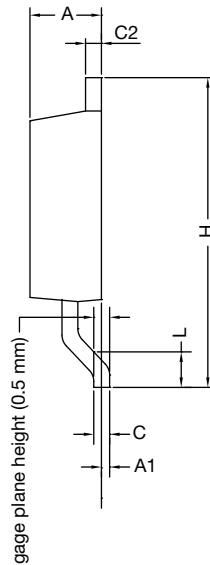
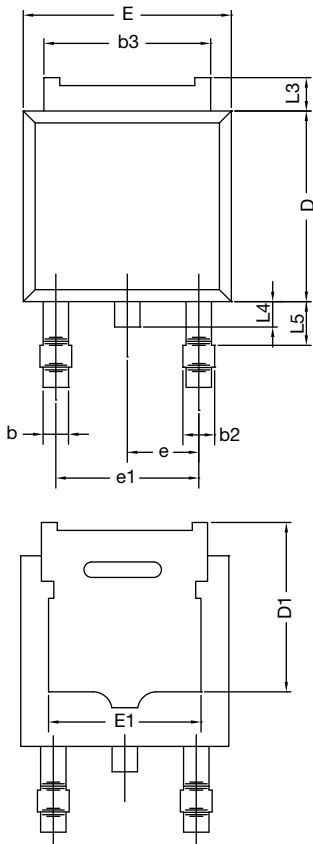
a.  $V_{GS} = -5V$  for logic level and  $-3V$  drive devices

**Fig. 14 - For P-Channel**

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see [www.vishay.com/ppg?91282](http://www.vishay.com/ppg?91282).



### TO-252AA Case Outline



DIM.	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	2.18	2.38	0.086	0.094
A1	-	0.127	-	0.005
b	0.64	0.88	0.025	0.035
b2	0.76	1.14	0.030	0.045
b3	4.95	5.46	0.195	0.215
C	0.46	0.61	0.018	0.024
C2	0.46	0.89	0.018	0.035
D	5.97	6.22	0.235	0.245
D1	4.10	-	0.161	-
E	6.35	6.73	0.250	0.265
E1	4.32	-	0.170	-
H	9.40	10.41	0.370	0.410
e	2.28 BSC		0.090 BSC	
e1	4.56 BSC		0.180 BSC	
L	1.40	1.78	0.055	0.070
L3	0.89	1.27	0.035	0.050
L4	-	1.02	-	0.040
L5	1.01	1.52	0.040	0.060
ECN: T16-0236-Rev. P, 16-May-16 DWG: 5347				

**Notes**

- Dimension L3 is for reference only.



### TO-251AA (HIGH VOLTAGE)



DIM.	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	2.18	2.39	0.086	0.094
A1	0.89	1.14	0.035	0.045
b	0.64	0.89	0.025	0.035
b1	0.65	0.79	0.026	0.031
b2	0.76	1.14	0.030	0.045
b3	0.76	1.04	0.030	0.041
b4	4.95	5.46	0.195	0.215
c	0.46	0.61	0.018	0.024
c1	0.41	0.56	0.016	0.022
c2	0.46	0.86	0.018	0.034
D	5.97	6.22	0.235	0.245

DIM.	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
D1	5.21	-	0.205	-
E	6.35	6.73	0.250	0.265
E1	4.32	-	0.170	-
e	2.29 BSC		2.29 BSC	
L	8.89	9.65	0.350	0.380
L1	1.91	2.29	0.075	0.090
L2	0.89	1.27	0.035	0.050
L3	1.14	1.52	0.045	0.060
theta1	0'	15'	0'	15'
theta2	25'	35'	25'	35'

ECN: S-82111-Rev. A, 15-Sep-08  
 DWG: 5968

#### Notes

1. Dimensioning and tolerancing per ASME Y14.5M-1994.
2. Dimension are shown in inches and millimeters.
3. Dimension D and E do not include mold flash. Mold flash shall not exceed 0.13 mm (0.005") per side. These dimensions are measured at the outermost extremes of the plastic body.
4. Thermal pad contour optional with dimensions b4, L2, E1 and D1.
5. Lead dimension uncontrolled in L3.
6. Dimension b1, b3 and c1 apply to base metal only.
7. Outline conforms to JEDEC outline TO-251AA.

## RECOMMENDED MINIMUM PADS FOR DPAK (TO-252)



Recommended Minimum Pads  
Dimensions in Inches/(mm)

[Return to Index](#)



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