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December 2015

FDMS86300

N-Channel PowerTrench® MOSFET

80 V, 122 A, 3.9 mΩ

Features

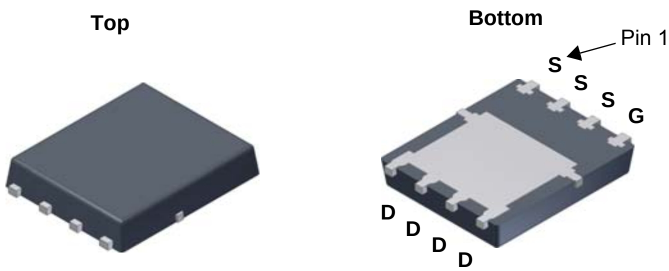
- Max $r_{DS(on)}$ = 3.9 mΩ at V_{GS} = 10 V, I_D = 19 A
- Max $r_{DS(on)}$ = 5.5 mΩ at V_{GS} = 8 V, I_D = 15.5 A
- Advanced Package and Silicon combination for low $r_{DS(on)}$ and high efficiency
- Next generation enhanced body diode technology, engineered for soft recovery
- MSL1 robust package design
- 100% UIL tested
- RoHS Compliant

General Description

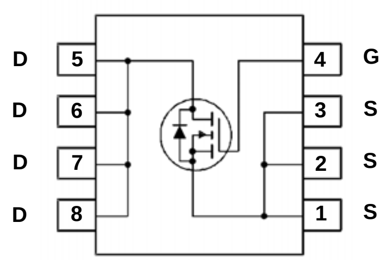
This N-Channel MOSFET has been designed specifically to improve the overall efficiency and to minimize switch node ringing of DC/DC converters using either synchronous or conventional switching PWM controllers.It has been optimized for low gate charge, low $r_{DS(on)}$, fast switching speed and body diode reverse recovery performance.

Applications

- OringFET / Load Switching
- DC-DC Conversion



Power 56



MOSFET Maximum Ratings T_A = 25 °C unless otherwise noted

Symbol	Parameter			Ratings	Units
V_{DS}	Drain to Source Voltage			80	V
V_{GS}	Gate to Source Voltage			±20	V
I_D	Drain Current -Continuous	T_C = 25 °C		122	A
	-Continuous	T_C = 100 °C		78	
	-Continuous	T_A = 25 °C	(Note 1a)	19	
	-Pulsed		(Note 4)	556	
E_{AS}	Single Pulse Avalanche Energy		(Note 3)	252	mJ
P_D	Power Dissipation	T_C = 25 °C		104	W
	Power Dissipation	T_A = 25 °C	(Note 1a)	2.5	
T_J, T_{STG}	Operating and Storage Junction Temperature Range			-55 to +150	°C

Thermal Characteristics

$R_{\theta JC}$	Thermal Resistance, Junction to Case		1.2	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	(Note 1a)	50	

Package Marking and Ordering Information

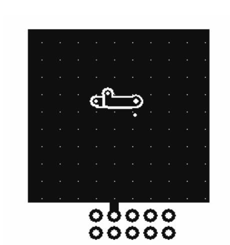
Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FDMS86300	FDMS86300	Power 56	13 ”	12 mm	3000 units

Electrical Characteristics T_J = 25 °C unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
Off Characteristics						
BV_{DSS}	Drain to Source Breakdown Voltage	I_D = 250 μA, V_{GS} = 0 V	80			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	I_D = 250 μA, referenced to 25 °C		39		mV/°C
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 64 V, V_{GS} = 0 V			1	μA
I_{GSS}	Gate to Source Leakage Current	V_{GS} = ±20 V, V_{DS} = 0 V			±100	nA
On Characteristics						
$V_{GS(th)}$	Gate to Source Threshold Voltage	V_{GS} = V_{DS}, I_D = 250 μA	2.5	3.4	4.5	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	I_D = 250 μA, referenced to 25 °C		-11		mV/°C
$r_{DS(on)}$	Static Drain to Source On Resistance	V_{GS} = 10 V, I_D = 19 A		3.2	3.9	mΩ
		V_{GS} = 8 V, I_D = 15.5 A		3.8	5.5	
		V_{GS} = 10 V, I_D = 19 A, T_J = 125 °C		5.0	5.8	
g_{FS}	Forward Transconductance	V_{DS} = 10 V, I_D = 19 A		60		S
Dynamic Characteristics						
C_{iss}	Input Capacitance	V_{DS} = 40 V, V_{GS} = 0 V, f = 1 MHz		5325	7082	pF
C_{oss}	Output Capacitance			957	1272	pF
C_{rss}	Reverse Transfer Capacitance			26	63	pF
R_g	Gate Resistance			1.2		Ω
Switching Characteristics						
$t_{d(on)}$	Turn-On Delay Time	V_{DD} = 40 V, I_D = 19 A, V_{GS} = 10 V, R_{GEN} = 6 Ω		31	50	ns
t_r	Rise Time			26	43	ns
$t_{d(off)}$	Turn-Off Delay Time			36	58	ns
t_f	Fall Time			9	18	ns
Q_g	Total Gate Charge	V_{GS} = 0 V to 10 V; V_{DD} = 40 V, I_D = 19 A		72	86	nC
Q_g	Total Gate Charge	V_{GS} = 0 V to 8 V; V_{DD} = 40 V, I_D = 19 A		59	71	nC
Q_{gs}	Gate to Source Charge	V_{DD} = 40 V, I_D = 19 A		28.2		nC
Q_{gd}	Gate to Drain “Miller” Charge	V_{DD} = 40 V, I_D = 19 A		14.9		nC
Drain-Source Diode Characteristics						
V_{SD}	Source to Drain Diode Forward Voltage	V_{GS} = 0 V, I_S = 2.1 A (Note 2)		0.71	1.2	V
		V_{GS} = 0 V, I_S = 19 A (Note 2)		0.81	1.3	
t_{rr}	Reverse Recovery Time	I_F = 19 A, di/dt = 100 A/μs		57	90	ns
Q_{rr}	Reverse Recovery Charge			50	80	nC
t_{rr}	Reverse Recovery Time	I_F = 19 A, di/dt = 300 A/μs		48	77	ns
Q_{rr}	Reverse Recovery Charge			103	165	nC

Notes:

1. $R_{\theta JA}$ is determined with the device mounted on a 1 in^2 pad 2 oz copper pad on a 1.5 x 1.5 in. board of FR-4 material. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.



a) 50 °C/W when mounted on a 1 in^2 pad of 2 oz copper

b) 125 °C/W when mounted on a minimum pad of 2 oz copper.

2. Pulse Test: Pulse Width < 300 μs, Duty cycle < 2.0%.
3. E_{AS} of 252 mJ is based on starting T_J = 25 °C, L = 0.3 mH, I_{AS} = 41 A, V_{DD} = 72 V, V_{GS} = 10 V.
4. Pulse Id limited by junction temperature, td ≤ 100 μs, please refer to SOA curve for more details.

Typical Characteristics T_J = 25 °C unless otherwise noted

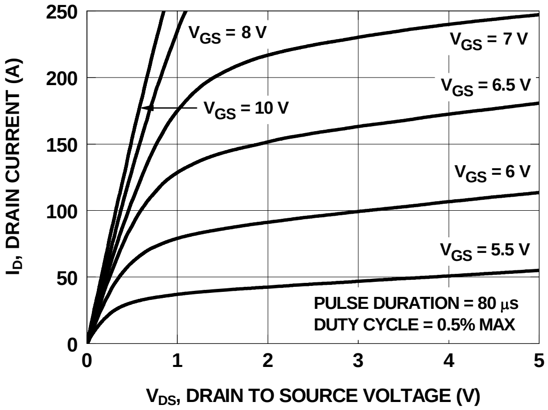


Figure 1. On-Region Characteristics

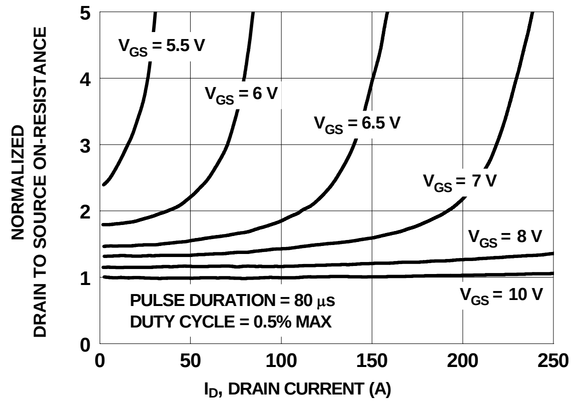


Figure 2. Normalized On-Resistance vs Drain Current and Gate Voltage

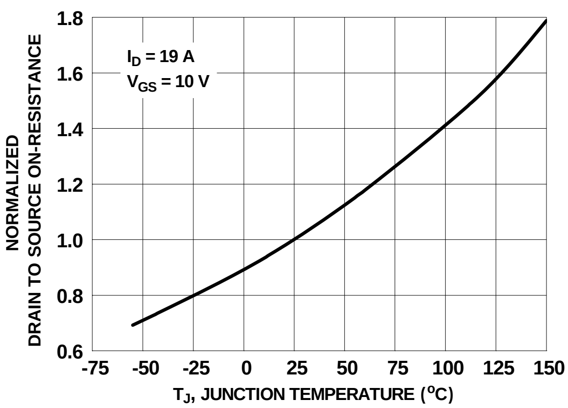


Figure 3. Normalized On-Resistance vs Junction Temperature

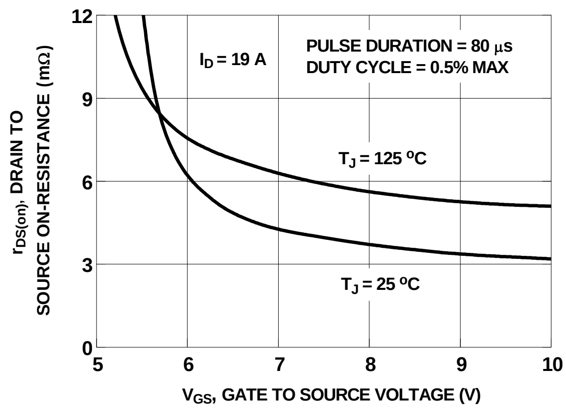


Figure 4. On-Resistance vs Gate to Source Voltage

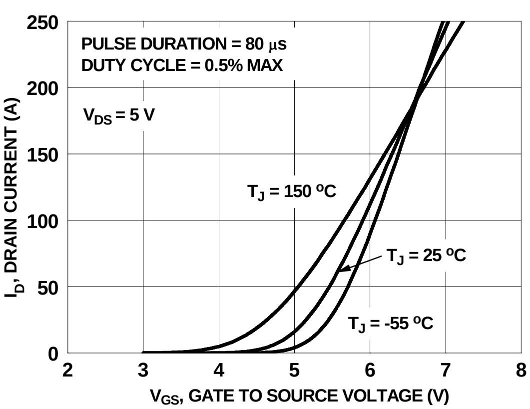


Figure 5. Transfer Characteristics

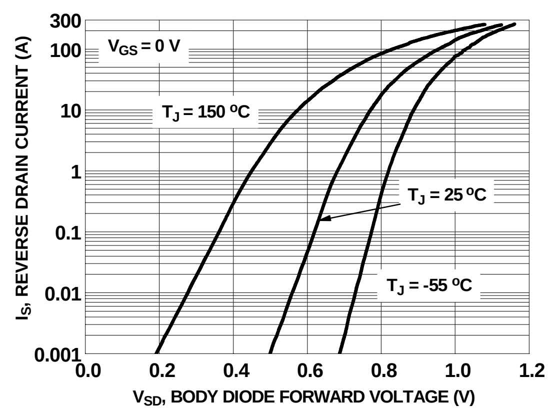


Figure 6. Source to Drain Diode Forward Voltage vs Source Current

Typical Characteristics T_J = 25 °C unless otherwise noted

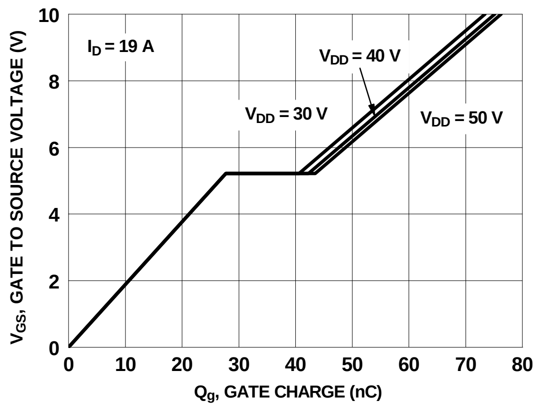


Figure 7. Gate Charge Characteristics

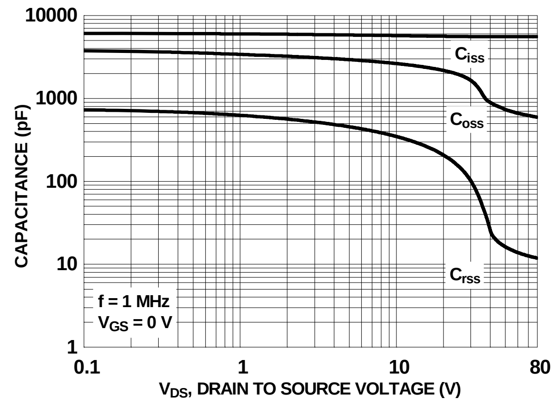


Figure 8. Capacitance vs Drain to Source Voltage

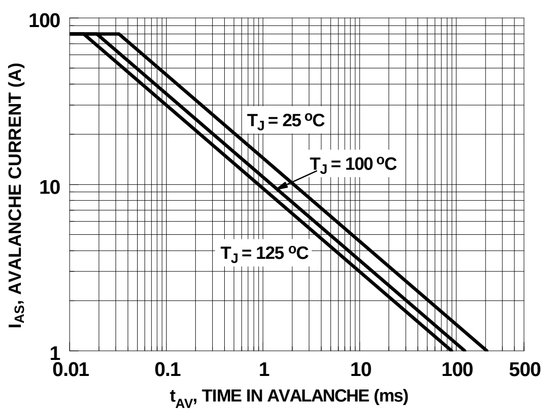


Figure 9. Unclamped Inductive Switching Capability

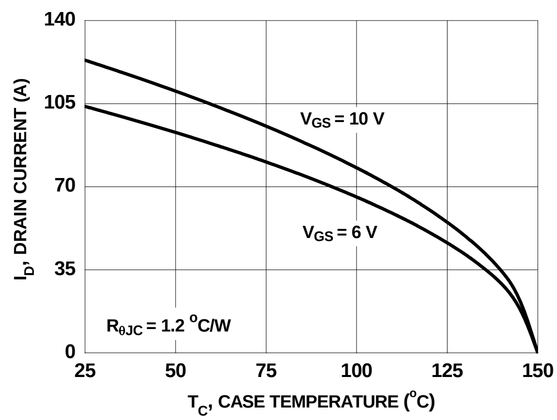


Figure 10. Maximum Continuous Drain Current vs Case Temperature

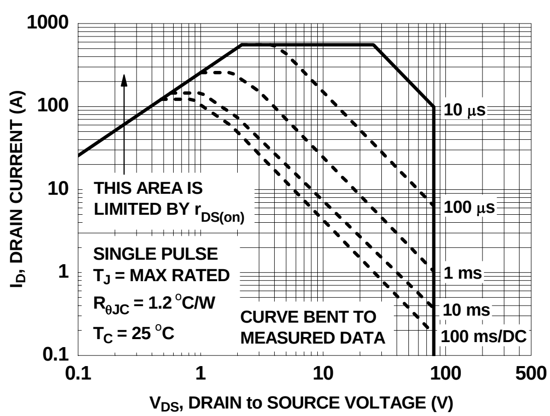


Figure 11. Forward Bias Safe Operating Area

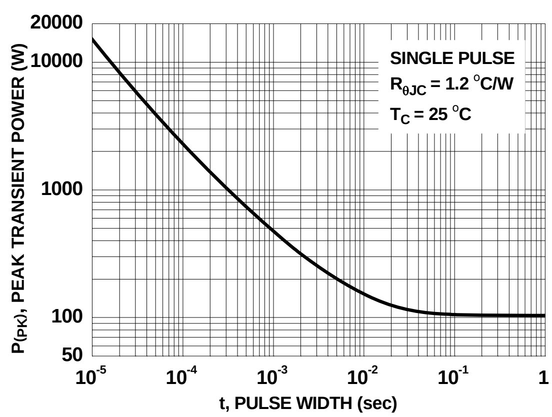


Figure 12. Single Pulse Maximum Power Dissipation

Typical Characteristics T_J = 25 °C unless otherwise noted

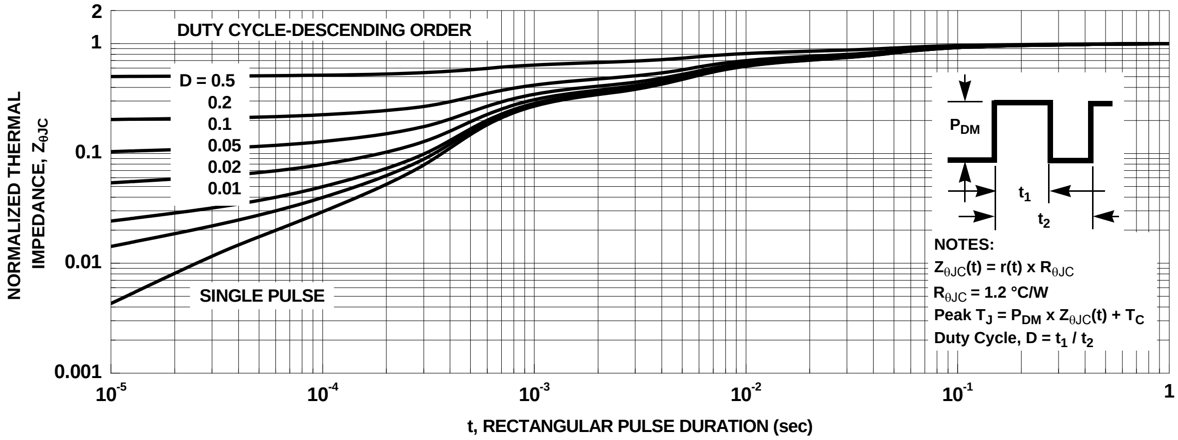
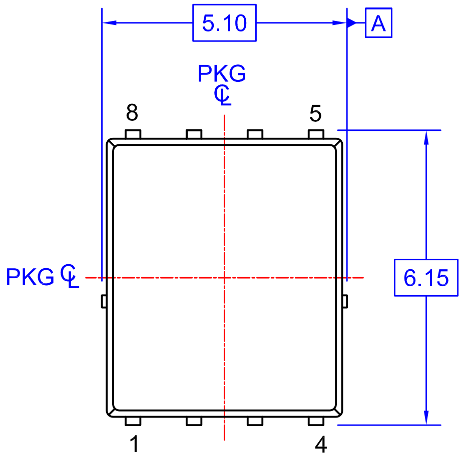
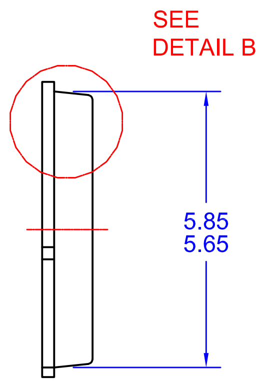
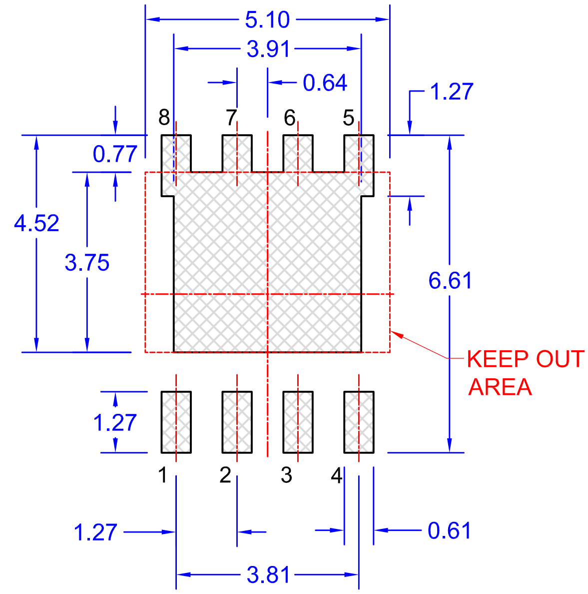


Figure 13. Junction-to-Case Transient Thermal Response Curve

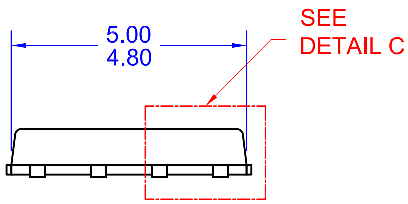


TOP VIEW

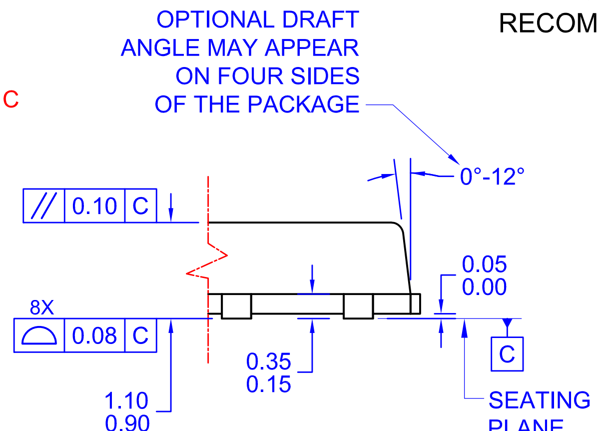




LAND PATTERN
RECOMMENDATION

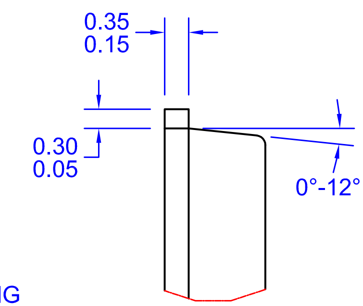


SIDE VIEW



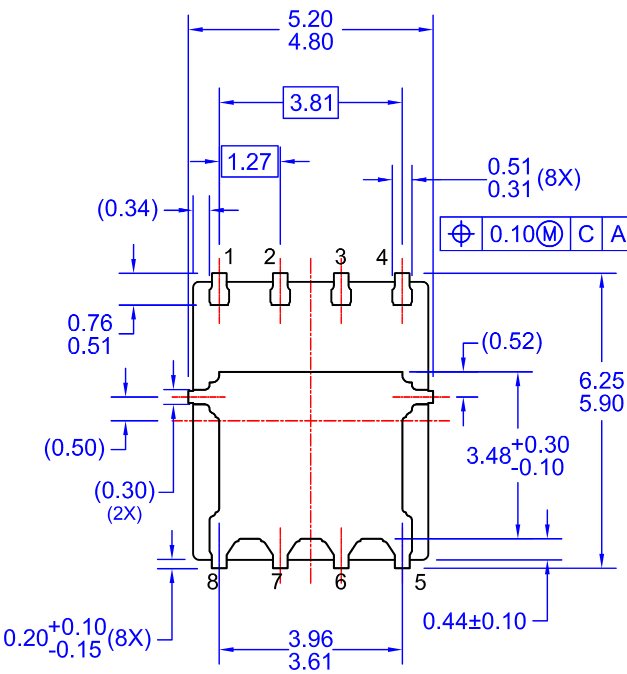
DETAIL C

SCALE: 2:1



DETAIL B

SCALE: 2:1



BOTTOM VIEW

NOTES: UNLESS OTHERWISE SPECIFIED

A. PACKAGE STANDARD REFERENCE: JEDEC MO-240, ISSUE A, VAR. AA, DATED OCTOBER 2002.

B. DIMENSIONS DO NOT INCLUDE BURRS OR MOLD FLASH. MOLD FLASH OR BURRS DOES NOT EXCEED 0.10MM.

C. ALL DIMENSIONS ARE IN MILLIMETERS.

D. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-2009.

E. IT IS RECOMMENDED TO HAVE NO TRACES OR VIAS WITHIN THE KEEP OUT AREA.

F. DRAWING FILE NAME: PQFN08AREV10

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