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FAIRCHILD SEMICONDUCTOR®

April 2009

FDS4435BZ

P-Channel PowerTrench® MOSFET

-30V, -8.8A, 20mΩ

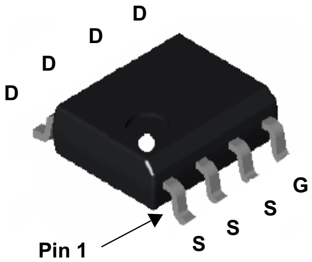
Features

- Max $r_{DS(on)}$ = 20mΩ at V_{GS} = -10V, I_D = -8.8A
- Max $r_{DS(on)}$ = 35mΩ at V_{GS} = -4.5V, I_D = -6.7A
- Extended V_{GSS} range (-25V) for battery applications
- HBM ESD protection level of ±3.8KV typical (note 3)
- High performance trench technology for extremely low $r_{DS(on)}$
- High power and current handling capability
- Termination is Lead-free and RoHS compliant

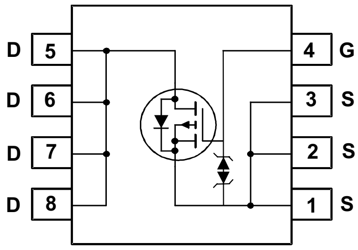
General Description

This P-Channel MOSFET is produced using Fairchild Semiconductor's advanced PowerTrench® process that has been especially tailored to minimize the on-state resistance.

This device is well suited for Power Management and load switching applications common in Notebook Computers and Portable Battery Packs.



SO-8



MOSFET Maximum Ratings T_A = 25°C unless otherwise noted

Symbol	Parameter			Ratings	Units
V_{DS}	Drain to Source Voltage			-30	V
V_{GS}	Gate to Source Voltage			±25	V
I_D	Drain Current -Continuous	T_A = 25°C	(Note 1a)	-8.8	A
	-Pulsed			-50	
P_D	Power Dissipation	T_A = 25°C	(Note 1a)	2.5	W
	Power Dissipation	T_A = 25°C	(Note 1b)	1.0	
E_{AS}	Single Pulse Avalanche Energy		(Note 4)	24	mJ
T_J, T_{STG}	Operating and Storage Junction Temperature Range			-55 to +150	°C

Thermal Characteristics

$R_{\theta JC}$	Thermal Resistance, Junction to Case		25	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	(Note 1a)	50	

Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FDS4435BZ	FDS4435BZ	SO-8	13''	12mm	2500units

Electrical Characteristics T_J = 25°C unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units

Off Characteristics

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
BV_{DSS}	Drain to Source Breakdown Voltage	I_D = -250μA, V_{GS} = 0V	-30			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	I_D = -250μA, referenced to 25°C		-21		mV/°C
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = -24V, V_{GS} = 0V			1	μA
I_{GSS}	Gate to Source Leakage Current	V_{GS} = ±25V, V_{DS} = 0V			±10	μA

On Characteristics

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
$V_{GS(th)}$	Gate to Source Threshold Voltage	V_{GS} = V_{DS}, I_D = -250μA	-1	-2.1	-3	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	I_D = -250μA, referenced to 25°C		6		mV/°C
$r_{DS(on)}$	Static Drain to Source On Resistance	V_{GS} = -10V, I_D = -8.8A		16	20	mΩ
		V_{GS} = -4.5V, I_D = -6.7A		26	35	
		V_{GS} = -10V, I_D = -8.8A, T_J = 125°C		22	28	
g_{FS}	Forward Transconductance	V_{DS} = -5V, I_D = -8.8A		24		S

Dynamic Characteristics

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
C_{iss}	Input Capacitance	V_{DS} = -15V, V_{GS} = 0V, f = 1MHz		1385	1845	pF
C_{oss}	Output Capacitance			275	365	pF
C_{rss}	Reverse Transfer Capacitance			230	345	pF
R_g	Gate Resistance	f = 1MHz		4.5		Ω

Switching Characteristics

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
$t_{d(on)}$	Turn-On Delay Time	V_{DD} = -15V, I_D = -8.8A, V_{GS} = -10V, R_{GEN} = 6Ω		10	20	ns
t_r	Rise Time			6	12	ns
$t_{d(off)}$	Turn-Off Delay Time			30	48	ns
t_f	Fall Time			12	22	ns
Q_g	Total Gate Charge	V_{GS} = 0V to -10V; V_{DD} = -15V, I_D = -8.8A		28	40	nC
Q_g	Total Gate Charge	V_{GS} = 0V to -5V		16	23	nC
Q_{gs}	Gate to Source Charge			5.2		nC
Q_{gd}	Gate to Drain "Miller" Charge			7.4		nC

Drain-Source Diode Characteristics

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
V_{SD}	Source to Drain Diode Forward Voltage	V_{GS} = 0V, I_S = -8.8A (Note 2)		-0.9	-1.2	V
t_{rr}	Reverse Recovery Time	I_F = -8.8A, di/dt = 100A/μs		29	44	ns
Q_{rr}	Reverse Recovery Charge			23	35	nC

NOTES:
1. $R_{\theta JA}$ is determined with the device mounted on a 1in^2 pad 2 oz copper pad on a 1.5 x 1.5 in. board of FR-4 material. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.

a. 50°C/W when mounted on a 1 in^2 pad of 2 oz copper.

b. 125°C/W when mounted on a minimum pad of 2 oz copper.

2. Pulse Test: Pulse Width < 300μs, Duty cycle < 2.0%.

3. The diode connected between the gate and source serves only as protection against ESD. No gate overvoltage rating is implied.

4. Starting T_J = 25°C, L = 1mH, I_{AS} = -7A, V_{DD} = -30V, V_{GS} = -10V

Typical Characteristics T_J = 25°C unless otherwise noted

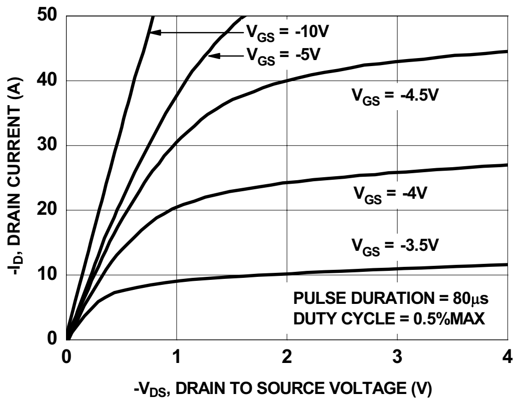


Figure 1. On-Region Characteristics

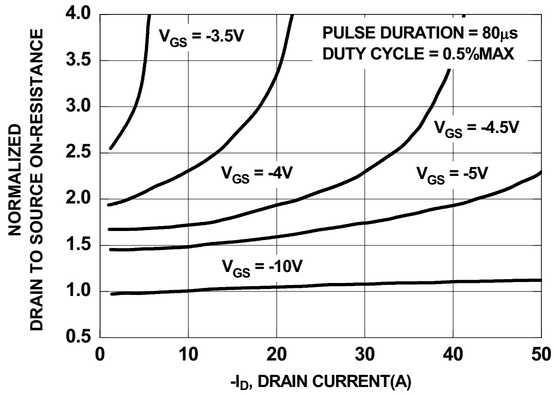


Figure 2. Normalized On-Resistance vs Drain Current and Gate Voltage

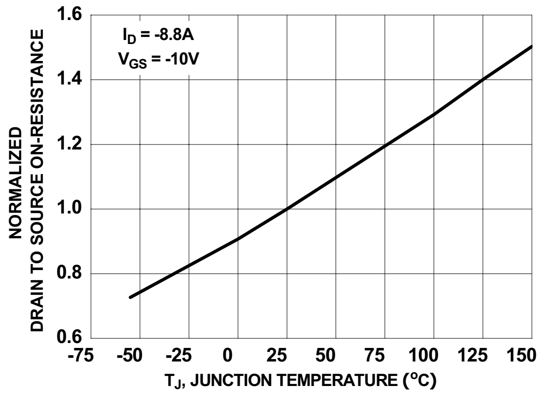


Figure 3. Normalized On-Resistance vs Junction Temperature

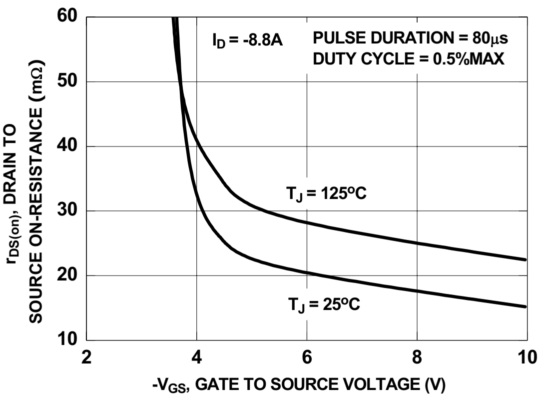


Figure 4. On-Resistance vs Gate to Source Voltage

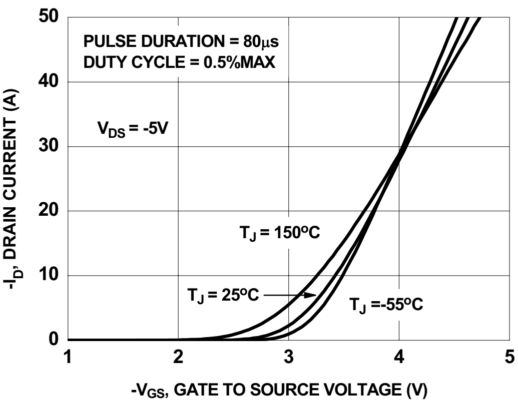


Figure 5. Transfer Characteristics

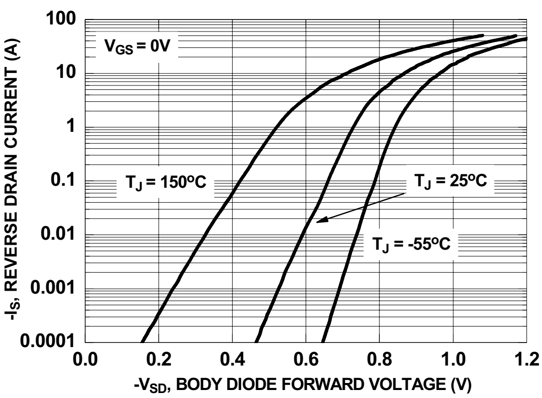


Figure 6. Source to Drain Diode Forward Voltage vs Source Current

Typical Characteristics T_J = 25°C unless otherwise noted

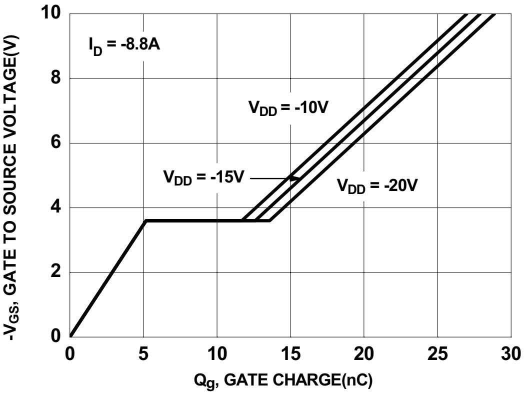


Figure 7. Gate Charge Characteristics

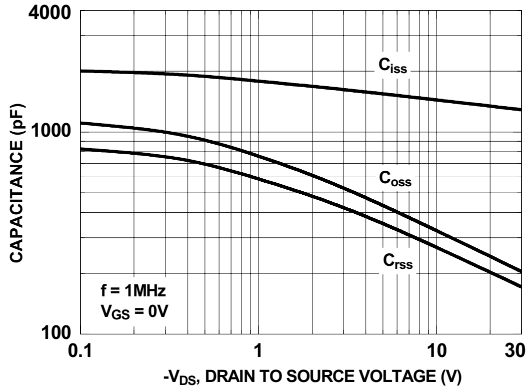


Figure 8. Capacitance vs Drain to Source Voltage

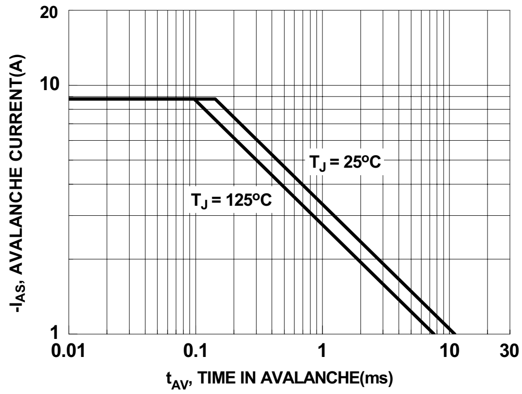


Figure 9. Unclamped Inductive Switching Capability

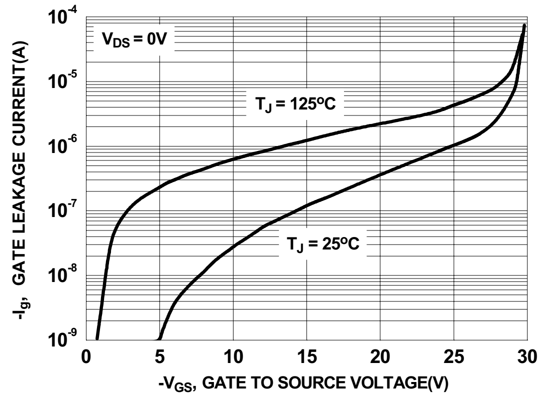


Figure 10. Gate Leakage Current vs Gate to Source Voltage

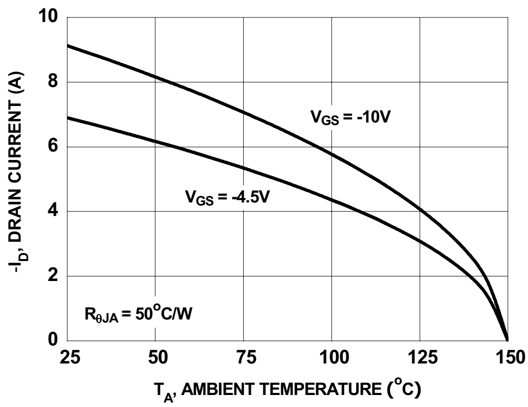


Figure 11. Maximum Continuous Drain Current vs Ambient Temperature

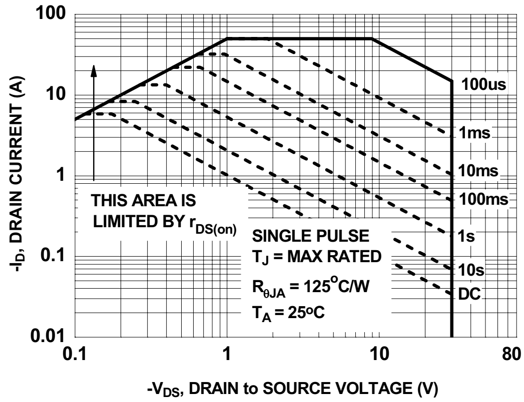


Figure 12. Forward Bias Safe Operating Area

Typical Characteristics T_J = 25°C unless otherwise noted

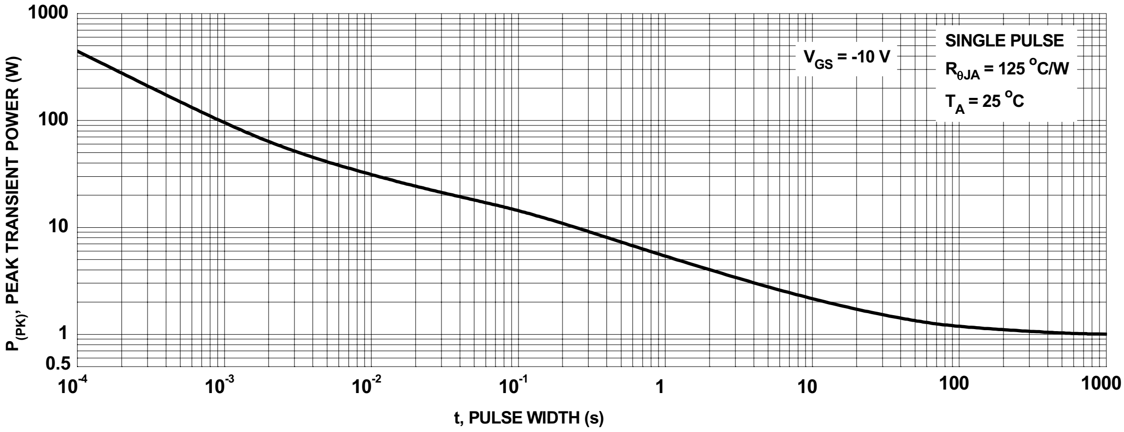


Figure 13. Single Pulse Maximum Power Dissipation

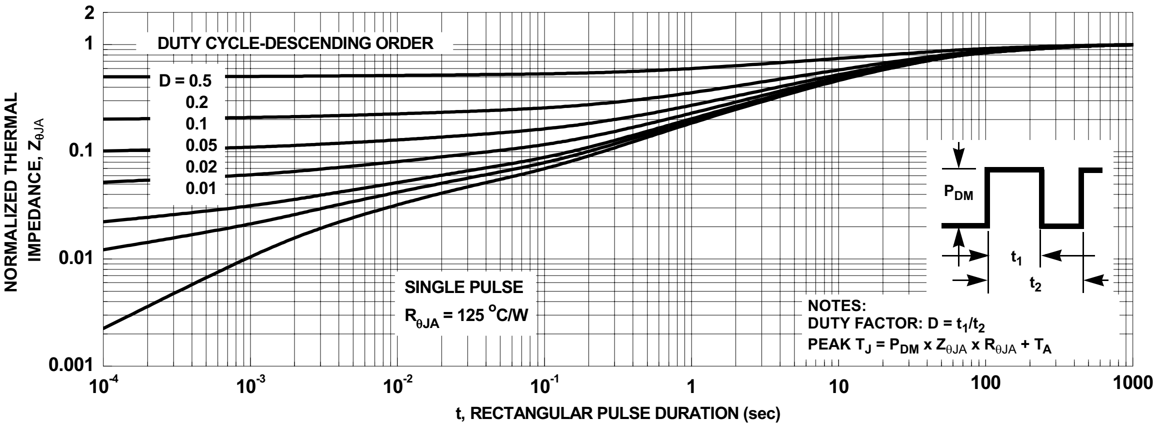


Figure 14. Transient Thermal Response Curve

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Preliminary	First Production	Datasheet contains preliminary data; supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve design.
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