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## FDN359AN N-Channel Logic Level PowerTrench™ MOSFET

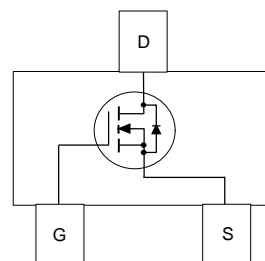
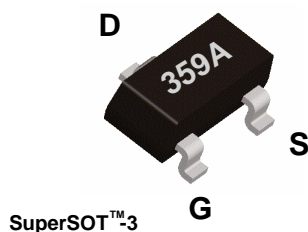
### General Description

This N-Channel Logic Level MOSFET is produced using Fairchild Semiconductor's advanced PowerTrench process that has been especially tailored to minimize on-state resistance and yet maintain superior switching performance.

These devices are well suited for low voltage and battery powered applications where low in-line power loss and fast switching are required.

### Features

- 2.7 A, 30 V.  $R_{DS(ON)} = 0.046 \Omega @ V_{GS} = 10 \text{ V}$   
 $R_{DS(ON)} = 0.060 \Omega @ V_{GS} = 4.5 \text{ V}$ .
- Very fast switching.
- Low gate charge (5nC typical).
- High power version of industry standard SOT-23 package. Identical pin out to SOT-23 with 30% higher power handling capability.



### Absolute Maximum Ratings $T_A = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Ratings	Units
$V_{DSS}$	Drain-Source Voltage	30	V
$V_{GSS}$	Gate-Source Voltage	$\pm 20$	V
$I_D$	Maximum Drain Current - Continuous (Note 1a)	2.7	A
	- Pulsed	15	
$P_D$	Maximum Power Dissipation (Note 1a) (Note 1b)	0.5	W
		0.46	
$T_J, T_{STG}$	Operating and Storage Temperature Range	-55 to 150	$^\circ\text{C}$

### THERMAL CHARACTERISTICS

$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient (Note 1a)	250	$^\circ\text{C/W}$
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case (Note 1)	75	$^\circ\text{C/W}$

## Electrical Characteristics ( $T_A = 25\text{ }^\circ\text{C}$ unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
<b>OFF CHARACTERISTICS</b>						
$BV_{DSS}$	Drain-Source Breakdown Voltage	$V_{GS} = 0\text{ V}, I_D = 250\text{ }\mu\text{A}$	30			V
$\Delta BV_{DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	$I_D = 250\text{ }\mu\text{A}$ , Referenced to $25\text{ }^\circ\text{C}$		23		mV/ $^\circ\text{C}$
$I_{DSS}$	Zero Gate Voltage Drain Current	$V_{DS} = 24\text{ V}, V_{GS} = 0\text{ V}$ $T_J = 55\text{ }^\circ\text{C}$			1	$\mu\text{A}$
					10	$\mu\text{A}$
$I_{GSSF}$	Gate - Body Leakage, Forward	$V_{GS} = 20\text{ V}, V_{DS} = 0\text{ V}$			100	nA
$I_{GSSR}$	Gate - Body Leakage, Reverse	$V_{GS} = -20\text{ V}, V_{DS} = 0\text{ V}$			-100	nA
<b>ON CHARACTERISTICS</b> (Note)						
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$	1	1.6	3	V
$\Delta V_{GS(th)}/\Delta T_J$	Gate Threshold Voltage Temp. Coefficient	$I_D = 250\text{ }\mu\text{A}$ , Referenced to $25\text{ }^\circ\text{C}$		-4		mV/ $^\circ\text{C}$
$R_{DS(on)}$	Static Drain-Source On-Resistance	$V_{GS} = 10\text{ V}, I_D = 2.7\text{ A}$ $T_J = 125\text{ }^\circ\text{C}$		0.037	0.046	$\Omega$
				0.055	0.075	
			$V_{GS} = 4.5\text{ V}, I_D = 2.4\text{ A}$	0.049	0.06	
$I_{D(on)}$	On-State Drain Current	$V_{GS} = 10\text{ V}, V_{DS} = 5\text{ V}$	15			A
$g_{FS}$	Forward Transconductance	$V_{DS} = 5\text{ V}, I_D = 2.7\text{ A}$		9.5		S
<b>DYNAMIC CHARACTERISTICS</b>						
$C_{iss}$	Input Capacitance	$V_{DS} = 10\text{ V}, V_{GS} = 0\text{ V},$ $f = 1.0\text{ MHz}$		480		pF
$C_{oss}$	Output Capacitance			120		pF
$C_{rss}$	Reverse Transfer Capacitance			45		pF
<b>SWITCHING CHARACTERISTICS</b> (Note)						
$t_{D(on)}$	Turn - On Delay Time	$V_{DD} = 5\text{ V}, I_D = 1\text{ A},$ $V_{GS} = 4.5\text{ V}, R_{GEN} = 6\text{ }\Omega$		6	12	ns
$t_r$	Turn - On Rise Time			13	24	ns
$t_{D(off)}$	Turn - Off Delay Time			15	27	ns
$t_f$	Turn - Off Fall Time			4	10	ns
$Q_g$	Total Gate Charge	$V_{DS} = 10\text{ V}, I_D = 2.7\text{ A},$ $V_{GS} = 5\text{ V}$		5	7	nC
$Q_{gs}$	Gate-Source Charge			1.4		nC
$Q_{gd}$	Gate-Drain Charge			1.6		nC
<b>DRAIN-SOURCE DIODE CHARACTERISTICS AND MAXIMUM RATINGS</b>						
$I_S$	Maximum Continuous Drain-Source Diode Forward Current				0.42	A
$V_{SD}$	Drain-Source Diode Forward Voltage	$V_{GS} = 0\text{ V}, I_S = 0.42\text{ A}$ (Note)		0.65	1.2	V

Note:

1.  $R_{\theta JA}$  is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins.  $R_{\theta JC}$  is guaranteed by design while  $R_{\theta CA}$  is determined by the user's board design.

Typical  $R_{\theta JA}$  using the board layouts shown below on FR-4 PCB in a still air environment :



a.  $250\text{ }^\circ\text{C/W}$  when mounted on a  $0.02\text{ in}^2$  pad of 2oz Cu.



b.  $270\text{ }^\circ\text{C/W}$  when mounted on a minimum pad.

Scale 1 : 1 on letter size paper

2. Pulse Test: Pulse Width  $\leq 300\mu\text{s}$ , Duty Cycle  $\leq 2.0\%$ .

## Typical Electrical Characteristics

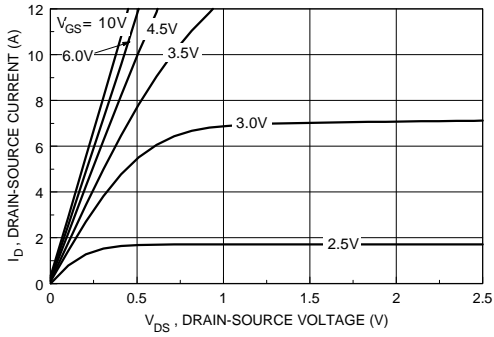


Figure 1. On-Region Characteristics.

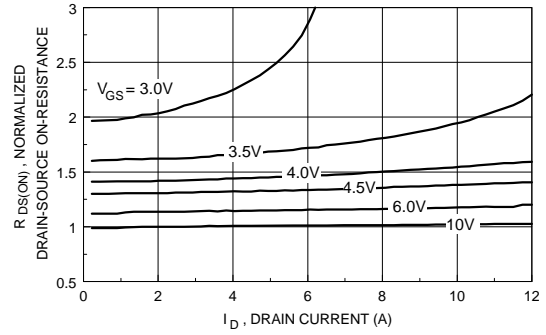


Figure 2. On-Resistance Variation with Drain Current and Gate Voltage.

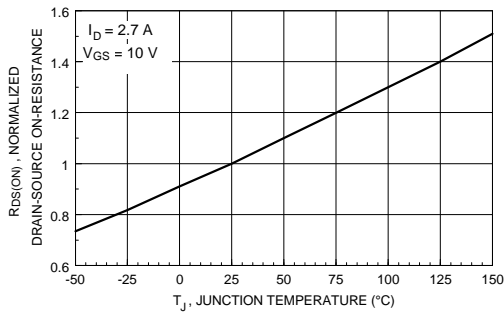


Figure 3. On-Resistance Variation with Temperature.

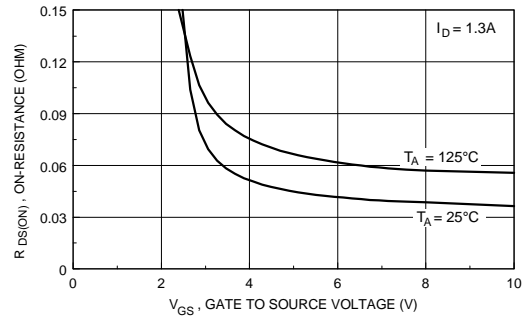


Figure 4. On-Resistance Variation with Gate-to-Source Voltage.

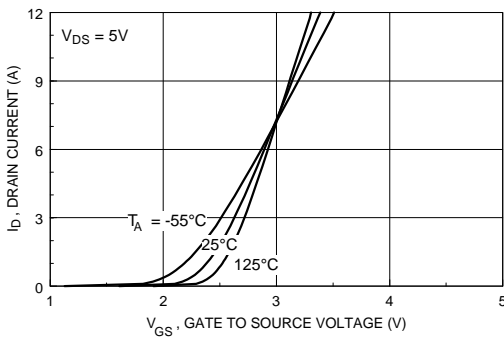


Figure 5. Transfer Characteristics.

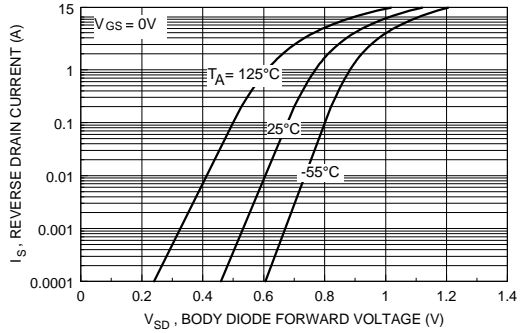


Figure 6. Body Diode Forward Voltage Variation with Source Current and Temperature.

## Typical Electrical Characteristics

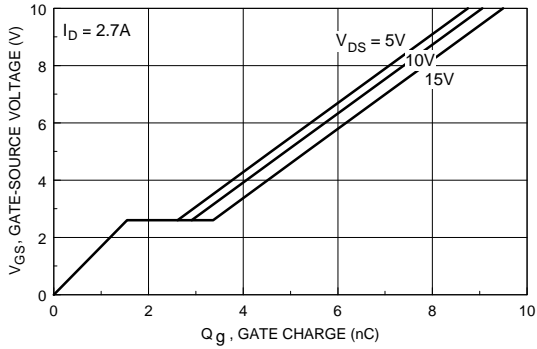


Figure 7. Gate Charge Characteristics.

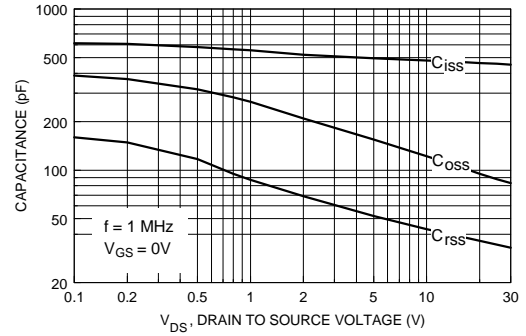


Figure 8. Capacitance Characteristics.

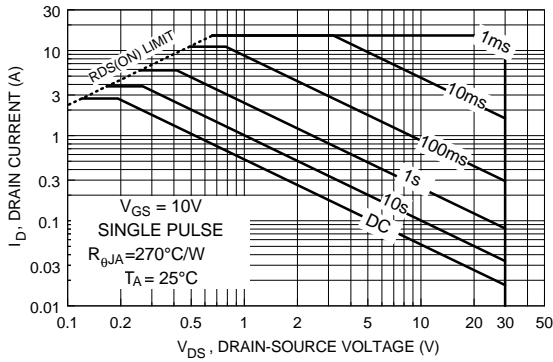


Figure 9. Maximum Safe Operating Area.

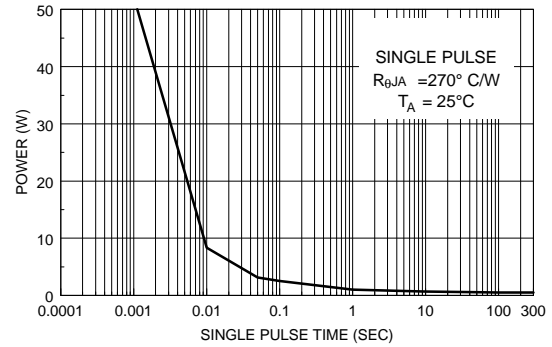


Figure 10. Single Pulse Maximum Power Dissipation.

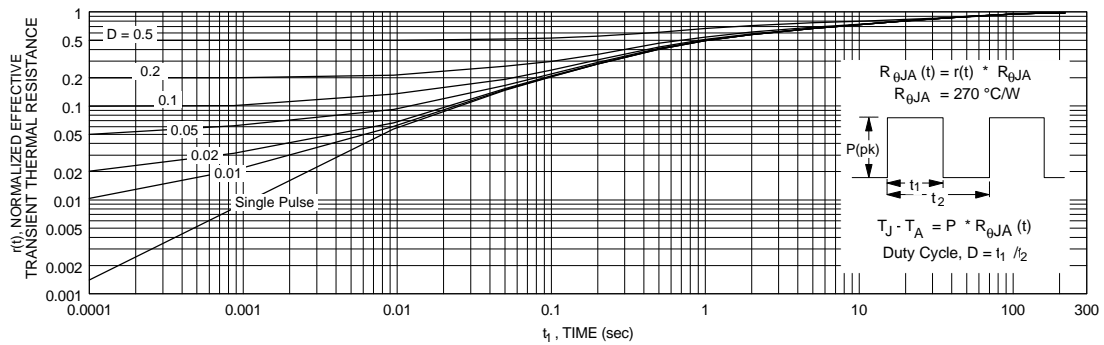


Figure 11. Transient Thermal Response Curve.

Thermal characterization performed using the conditions described in note 1b.

Transient thermal response will change depending on the circuit board design.

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