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FAIRCHILD SEMICONDUCTOR®

May 2010

FDMA507PZ

Single P-Channel PowerTrench® MOSFET

-20 V, -7.8 A, 24 mΩ

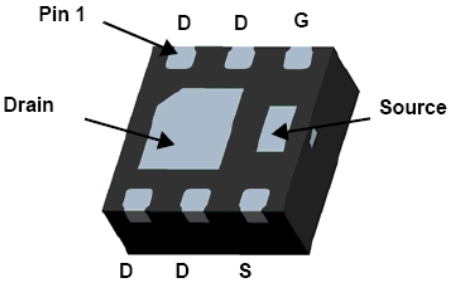
Features

- Max $r_{DS(on)}$ = 24 mΩ at V_{GS} = -5 V, I_D = -7.8 A
- Max $r_{DS(on)}$ = 25 mΩ at V_{GS} = -4.5 V, I_D = -7 A
- Max $r_{DS(on)}$ = 35 mΩ at V_{GS} = -2.5 V, I_D = -5.5 A
- Max $r_{DS(on)}$ = 45 mΩ at V_{GS} = -1.8 V, I_D = -4 A
- Low Profile - 0.8 mm maximum - in the package MicroFET 2X2 mm
- HBM ESD protection level > 3.2K V typical (Note3)
- Free from halogenated compounds and antimony oxides
- RoHS Compliant

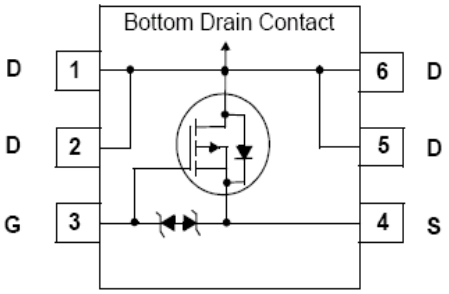
General Description

This device is designed specifically for battery charge or load switching in cellular handset and other ultraportable applications. It features a MOSFET with low on-stade resistance.

The MicroFET 2X2 package offers exceptional thermal perfomance for its physical size and is well suited to linear mode applications.



MicroFET 2X2 (Bottom View)



MOSFET Maximum Ratings T_A = 25 °C unless otherwise noted

Symbol	Parameter			Ratings	Units
V_{DS}	Drain to Source Voltage			-20	V
V_{GS}	Gate to Source Voltage			±8	V
I_D	Drain Current -Continuous	T_A = 25 °C	(Note 1a)	-7.8	A
	-Pulsed			-24	
P_D	Power Dissipation	T_A = 25 °C	(Note 1a)	2.4	W
	Power Dissipation	T_A = 25 °C	(Note 1b)	0.9	
T_J, T_{STG}	Operating and Storage Junction Temperature Range			-55 to +150	°C

Thermal Characteristics

$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	(Note 1a)	52	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	(Note 1b)	145	

Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
507	FDMA507PZ	MicroFET 2X2	7 ”	12 mm	3000 units

Electrical Characteristics T_J = 25 °C unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
Off Characteristics						
BV_{DSS}	Drain to Source Breakdown Voltage	I_D = -250 μA, V_{GS} = 0 V	-20			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	I_D = -250 μA, referenced to 25 °C		-12		mV/°C
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = -16 V, V_{GS} = 0 V			-1	μA
I_{GSS}	Gate to Source Leakage Current	V_{GS} = ±8 V, V_{DS} = 0 V			±10	μA
On Characteristics						
$V_{GS(th)}$	Gate to Source Threshold Voltage	V_{GS} = V_{DS}, I_D = -250 μA	-0.4	-0.5	-1.5	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	I_D = -250 μA, referenced to 25 °C		3		mV/°C
$r_{DS(on)}$	Drain to Source On Resistance	V_{GS} = -5 V, I_D = -7.8 A		19	24	mΩ
		V_{GS} = -4.5 V, I_D = -7 A		20	25	
		V_{GS} = -2.5 V, I_D = -5.5 A		24	35	
		V_{GS} = -1.8 V, I_D = -4 A		29	45	
		V_{GS} = -5 V, I_D = -7.8 A, T_J = 125 °C		26	34	
g_{FS}	Forward Transconductance	V_{DS} = -5 V, I_D = -7.8 A		33		S
Dynamic Characteristics						
C_{iss}	Input Capacitance	V_{DS} = -10 V, V_{GS} = 0 V, f = 1 MHz		1515	2015	pF
C_{oss}	Output Capacitance			265	355	pF
C_{rss}	Reverse Transfer Capacitance			240	360	pF
Switching Characteristics						
$t_{d(on)}$	Turn-On Delay Time	V_{DD} = -10 V, I_D = -7.8 A, V_{GS} = -5 V, R_{GEN} = 6 Ω		6.4	13	ns
t_r	Rise Time			14	25	ns
$t_{d(off)}$	Turn-Off Delay Time			192	307	ns
t_f	Fall Time			96	154	ns
$Q_{g(TOT)}$	Total Gate Charge	V_{DD} = -10 V, I_D = -7.8 A, V_{GS} = -5 V		30	42	nC
Q_{gs}	Gate to Source Gate Charge			2		nC
Q_{gd}	Gate to Drain “Miller” Charge			7.5		nC
Drain-Source Diode Characteristics						
V_{SD}	Source to Drain Diode Forward Voltage	V_{GS} = 0 V, I_S = -2.0 A (Note 2)		-0.6	-1.2	V
t_{rr}	Reverse Recovery Time	I_F = -7.8 A, di/dt = 100 A/μs		66	106	ns
Q_{rr}	Reverse Recovery Charge			44	70	nC

Notes:

1. $R_{\theta JA}$ is determined with the device mounted on a 1 in^2 pad 2 oz copper pad on a 1.5 x 1.5 in. board of FR-4 material. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.

a. 52 °C/W when mounted on a 1 in^2 pad of 2 oz copper.

b. 145 °C/W when mounted on a minimum pad of 2 oz copper.

2. Pulse Test: Pulse Width < 300μs, Duty cycle < 2.0%.

3. The diode connected between the gate and source serves only as protection against ESD. No gate overvoltage rating is implied.

Typical Characteristics T_J = 25 °C unless otherwise noted

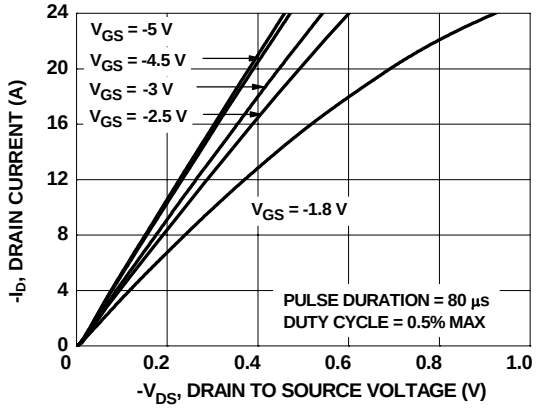


Figure 1. On Region Characteristics

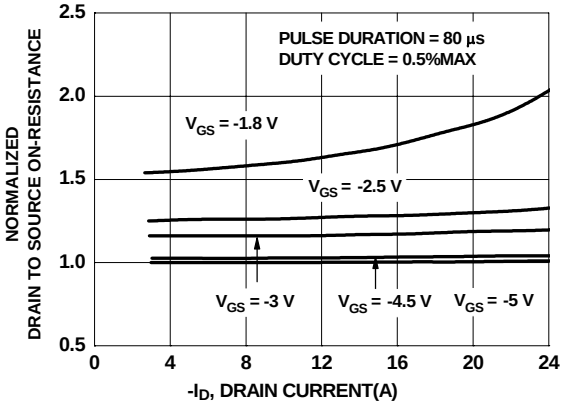


Figure 2. Normalized On-Resistance vs Drain Current and Gate Voltage

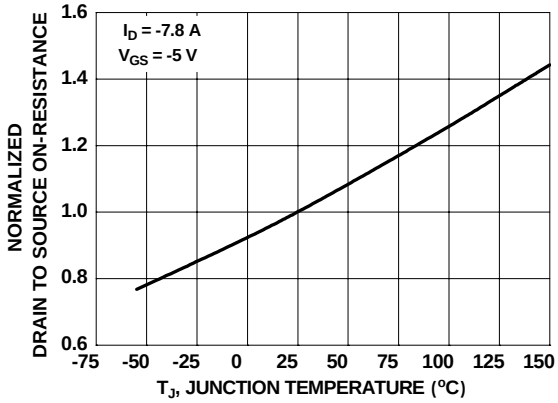


Figure 3. Normalized On Resistance vs Junction Temperature

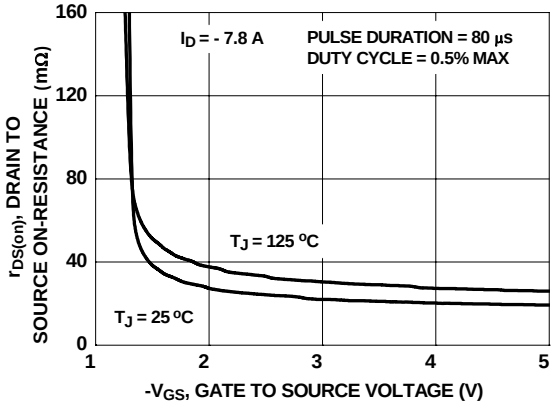


Figure 4. On-Resistance vs Gate to Source Voltage

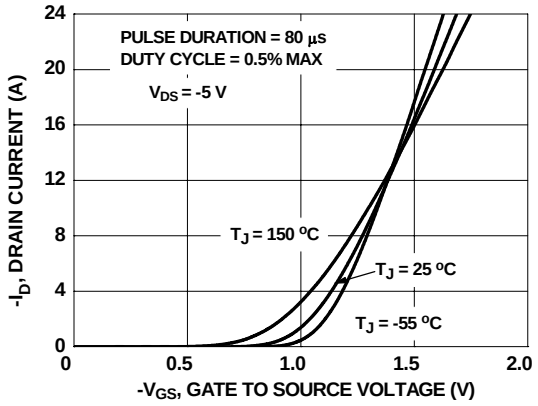


Figure 5. Transfer Characteristics

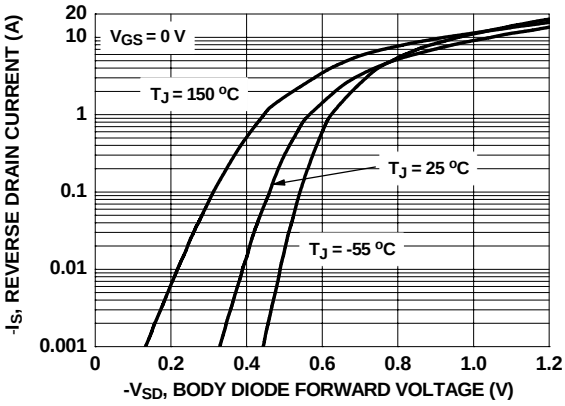


Figure 6. Source to Drain Diode Forward Voltage vs Source Current

Typical Characteristics T_J = 25 °C unless otherwise noted

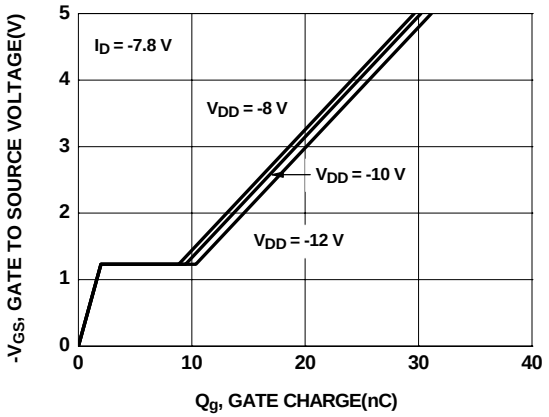


Figure 7. Gate Charge Characteristics

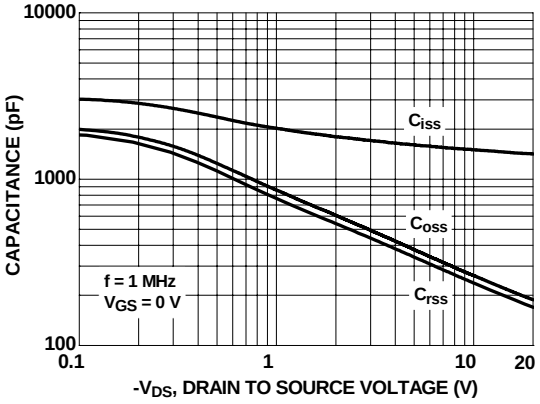


Figure 8. Capacitance vs Drain to Source Voltage

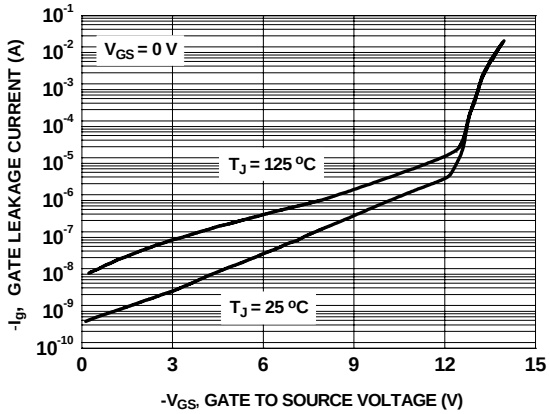


Figure 9. Gate Leakage Current vs Gate to Source Voltage

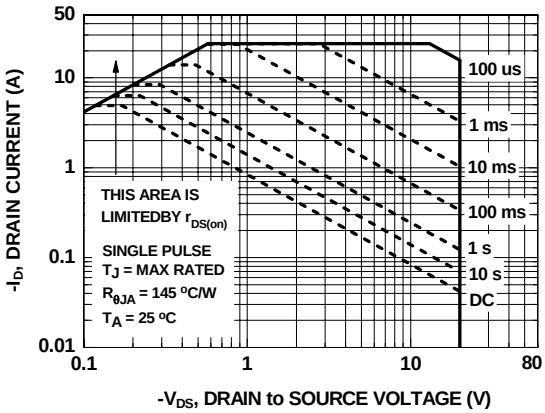


Figure 10. Forward Bias Safe Operating Area

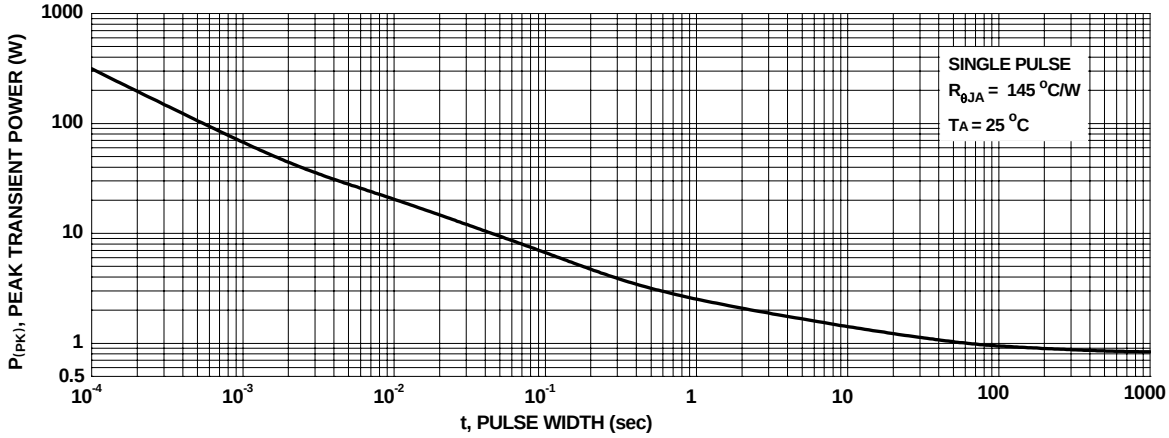


Figure 11. Single Pulse Maximum Power Dissipation

Typical Characteristics T_J = 25 °C unless otherwise noted

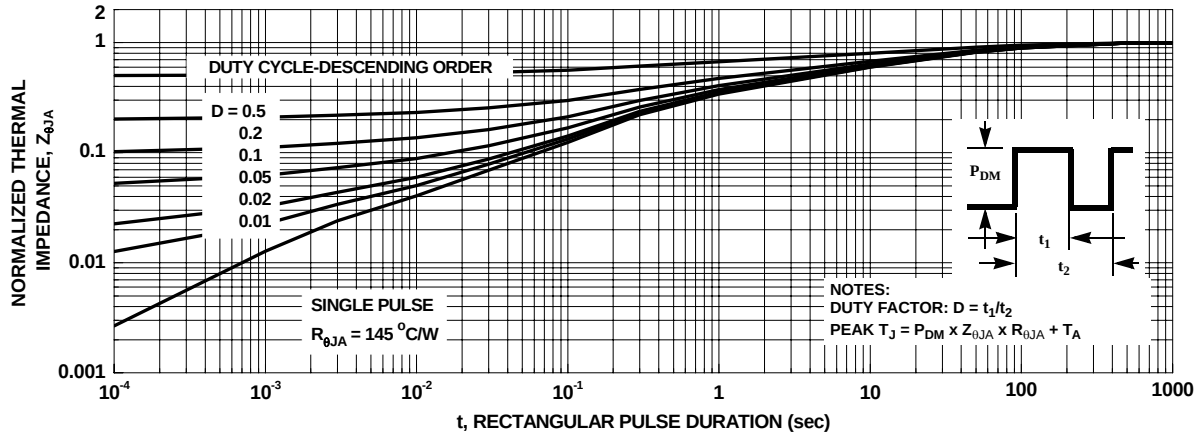
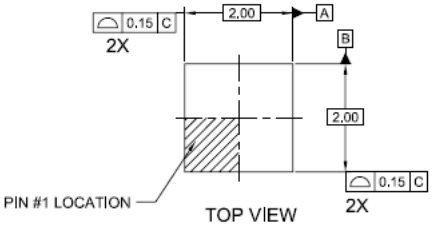
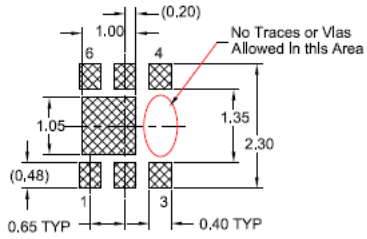


Figure 12. Junction-to-Ambient Transient Thermal Response Curve

Dimensional Outline and Pad Layout





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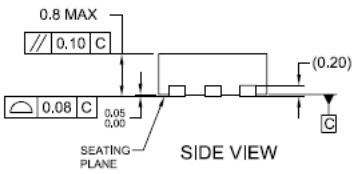

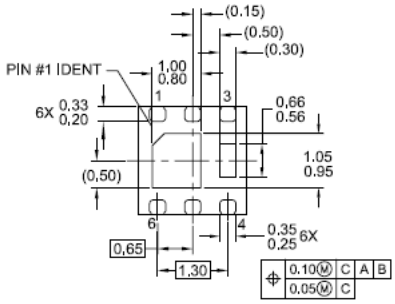

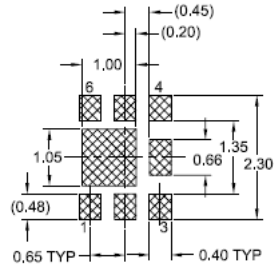

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