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# FDD3N50NZ

## N-Channel UniFET™ II MOSFET

500 V, 2.5 A, 2.5 Ω

### Features

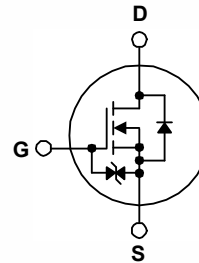
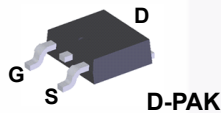
- $R_{DS(on)} = 2.1 \Omega$  (Typ.) @  $V_{GS} = 10 V$ ,  $I_D = 1.25 A$
- Low Gate Charge (Typ. 6.2 nC)
- Low  $C_{rss}$  (Typ. 2.5 pF)
- 100% Avalanche Tested
- Improved dv/dt Capability
- ESD Improved Capability
- RoHS Compliant

### Applications

- LCD/LED/PDP TV
- Lighting
- Uninterruptible Power Supply

### Description

UniFET™ II MOSFET is Fairchild Semiconductor's high voltage MOSFET family based on advanced planar stripe and DMOS technology. This advanced MOSFET family has the smallest on-state resistance among the planar MOSFET, and also provides superior switching performance and higher avalanche energy strength. In addition, internal gate-source ESD diode allows UniFET II MOSFET to withstand over 2kV HBM surge stress. This device family is suitable for switching power converter applications such as power factor correction (PFC), flat panel display (FPD) TV power, ATX and electronic lamp ballasts.



### Absolute Maximum Ratings $T_C = 25^\circ C$ unless otherwise noted.

Symbol	Parameter	FDD3N50NZTM	Unit
$V_{DSS}$	Drain to Source Voltage	500	V
$V_{GSS}$	Gate to Source Voltage	$\pm 25$	V
$I_D$	Drain Current	- Continuous ( $T_C = 25^\circ C$ )	2.5
		- Continuous ( $T_C = 100^\circ C$ )	1.5
$I_{DM}$	Drain Current	- Pulsed (Note 1)	10
$E_{AS}$	Single Pulsed Avalanche Energy	(Note 2)	114
$I_{AR}$	Avalanche Current	(Note 1)	2.5
$E_{AR}$	Repetitive Avalanche Energy	(Note 1)	4
dv/dt	Peak Diode Recovery dv/dt	(Note 3)	10
$P_D$	Power Dissipation	( $T_C = 25^\circ C$ )	40
		- Derate Above $25^\circ C$	0.3
$T_J, T_{STG}$	Operating and Storage Temperature Range	-55 to +150	$^\circ C$
$T_L$	Maximum Lead Temperature for Soldering, 1/8" from Case for 5 Seconds	300	$^\circ C$

### Thermal Characteristics

Symbol	Parameter	FDD3N50NZTM	Unit
$R_{\theta JC}$	Thermal Resistance, Junction to Case, Max.	3.1	$^\circ C/W$
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient, Max.	90	

## Package Marking and Ordering Information

Part Number	Top Mark	Package	Packing Method	Reel Size	Tape Width	Quantity
FDD3N50NZTM	FDD3N50NZ	DPAK	Tape and Reel	330 mm	16 mm	2500 units

## Electrical Characteristics $T_C = 25^\circ\text{C}$ unless otherwise noted.

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
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### Off Characteristics

$BV_{DSS}$	Drain to Source Breakdown Voltage	$I_D = 250 \mu\text{A}, V_{GS} = 0 \text{ V}, T_C = 25^\circ\text{C}$	500	-	-	V
$\Delta BV_{DSS} / \Delta T_J$	Breakdown Voltage Temperature Coefficient	$I_D = 250 \mu\text{A}$ , Referenced to $25^\circ\text{C}$	-	0.5	-	$\text{V}/^\circ\text{C}$
$I_{DSS}$	Zero Gate Voltage Drain Current	$V_{DS} = 500 \text{ V}, V_{GS} = 0 \text{ V}$ $V_{DS} = 400 \text{ V}, V_{GS} = 0 \text{ V}, T_C = 125^\circ\text{C}$	-	-	1 10	$\mu\text{A}$
$I_{GSS}$	Gate to Body Leakage Current	$V_{GS} = \pm 25 \text{ V}, V_{DS} = 0 \text{ V}$	-	-	$\pm 10$	$\mu\text{A}$

### On Characteristics

$V_{GS(th)}$	Gate Threshold Voltage	$V_{GS} = V_{DS}, I_D = 250 \mu\text{A}$	3.0	-	5.0	V
$R_{DS(on)}$	Static Drain to Source On Resistance	$V_{GS} = 10 \text{ V}, I_D = 1.25 \text{ A}$	-	2.1	2.5	$\Omega$
$g_{FS}$	Forward Transconductance	$V_{DS} = 20 \text{ V}, I_D = 1.25 \text{ A}$	-	1.9	-	S

### Dynamic Characteristics

$C_{iss}$	Input Capacitance	$V_{DS} = 25 \text{ V}, V_{GS} = 0 \text{ V},$ $f = 1 \text{ MHz}$	-	210	280	pF
$C_{oss}$	Output Capacitance		-	30	45	pF
$C_{riss}$	Reverse Transfer Capacitance		-	2.5	5	pF
$Q_{g(tot)}$	Total Gate Charge at 10V	$V_{DS} = 400 \text{ V}, I_D = 2.5 \text{ A},$ $V_{GS} = 10 \text{ V}$	-	6.2	8	nC
$Q_{gs}$	Gate to Source Gate Charge		-	1.4	-	nC
$Q_{gd}$	Gate to Drain "Miller" Charge		(Note 4)	-	3.1	-

### Switching Characteristics

$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = 250 \text{ V}, I_D = 2.5 \text{ A},$ $V_{GS} = 10 \text{ V}, R_G = 25 \Omega$	-	10	30	ns
$t_r$	Turn-On Rise Time		-	15	40	ns
$t_{d(off)}$	Turn-Off Delay Time		-	26	60	ns
$t_f$	Turn-Off Fall Time		(Note 4)	-	17	45

### Drain-Source Diode Characteristics

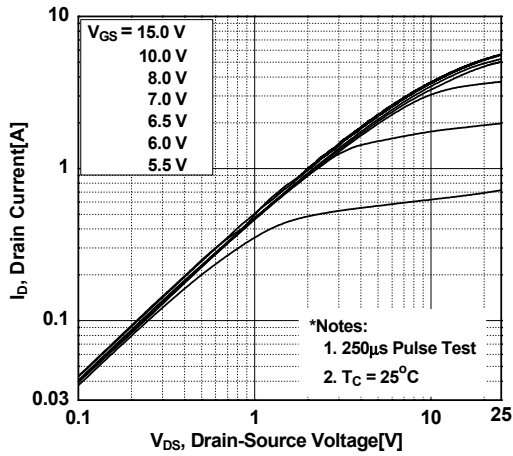
$I_S$	Maximum Continuous Drain to Source Diode Forward Current	-	-	2.5	A	
$I_{SM}$	Maximum Pulsed Drain to Source Diode Forward Current	-	-	10	A	
$V_{SD}$	Drain to Source Diode Forward Voltage	$V_{GS} = 0 \text{ V}, I_{SD} = 2.5 \text{ A}$	-	-	1.4	V
$t_{rr}$	Reverse Recovery Time	$V_{GS} = 0 \text{ V}, I_{SD} = 2.5 \text{ A},$ $di_F/dt = 100 \text{ A}/\mu\text{s}$	-	190	-	ns
$Q_{rr}$	Reverse Recovery Charge		-	0.52	-	$\mu\text{C}$

#### Notes:

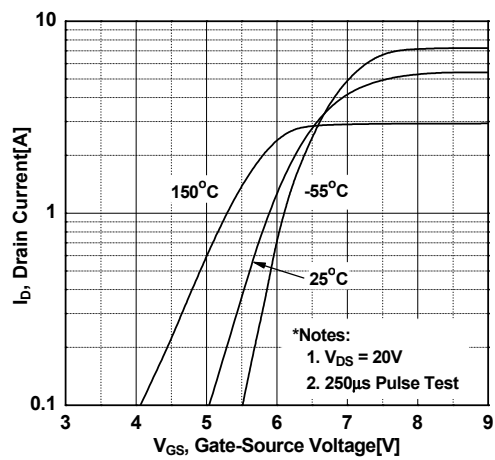
1. Repetitive rating: pulse-width limited by maximum junction temperature.
2.  $L = 36.6 \text{ mH}, I_{AS} = 2.5 \text{ A}, V_{DD} = 50 \text{ V}, R_G = 25 \Omega$ , starting  $T_J = 25^\circ\text{C}$ .
3.  $I_{SD} \leq 2.5 \text{ A}, di/dt \leq 200 \text{ A}/\mu\text{s}, V_{DD} \leq BV_{DSS}$ , starting  $T_J = 25^\circ\text{C}$ .
4. Essentially independent of operating temperature typical characteristics.

## Typical Performance Characteristics

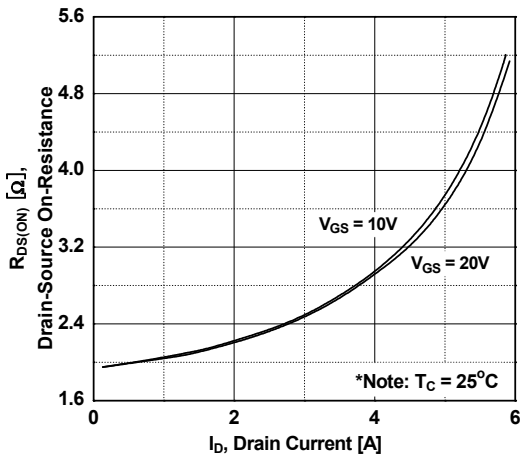
**Figure 1. On-Region Characteristics**



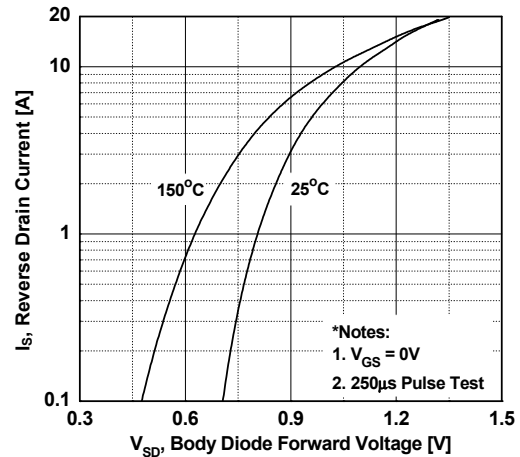
**Figure 2. Transfer Characteristics**



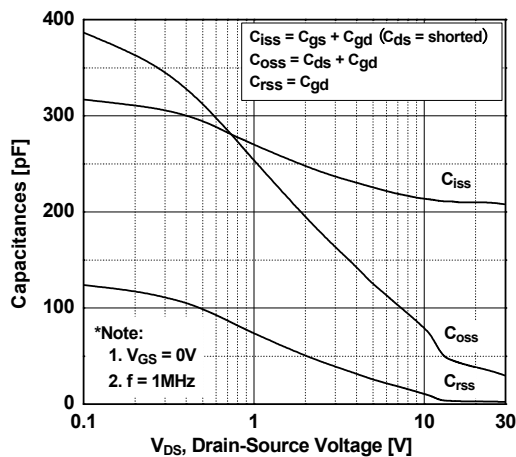
**Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage**



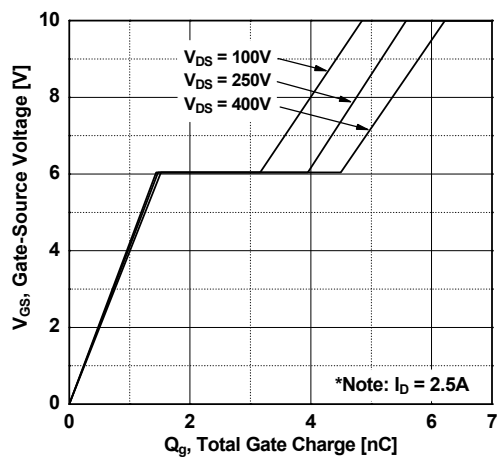
**Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature**



**Figure 5. Capacitance Characteristics**

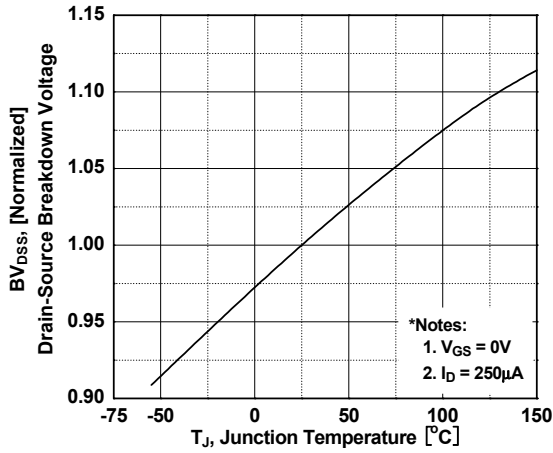


**Figure 6. Gate Charge Characteristics**

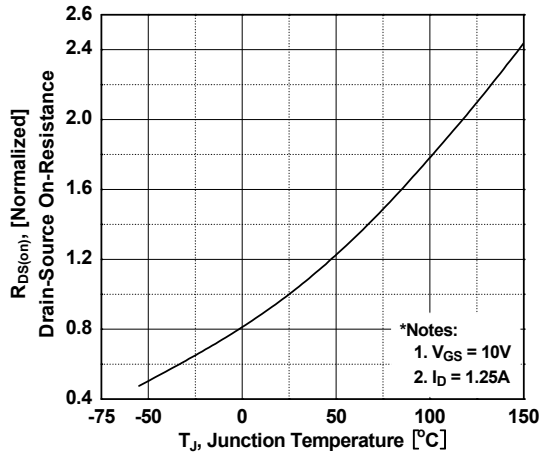


**Typical Performance Characteristics** (Continued)

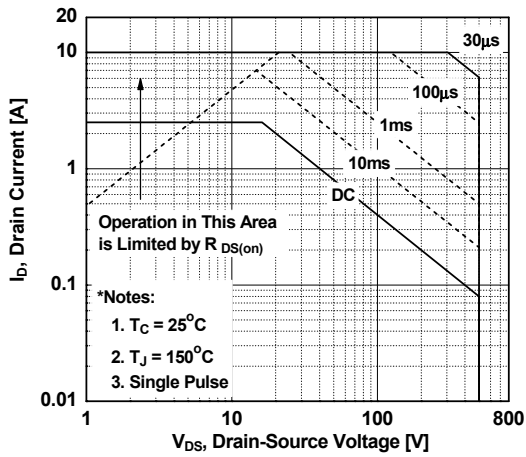
**Figure 7. Breakdown Voltage Variation vs. Temperature**



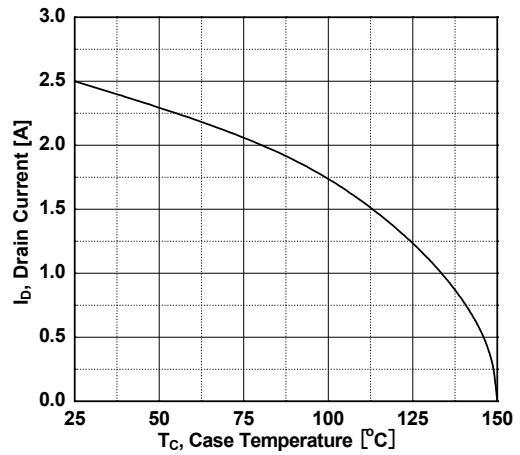
**Figure 8. On-Resistance Variation vs. Temperature**



**Figure 9. Maximum Safe Operating Area**



**Figure 10. Maximum Drain Current vs. Case Temperature**



**Figure 11. Transient Thermal Response Curve**

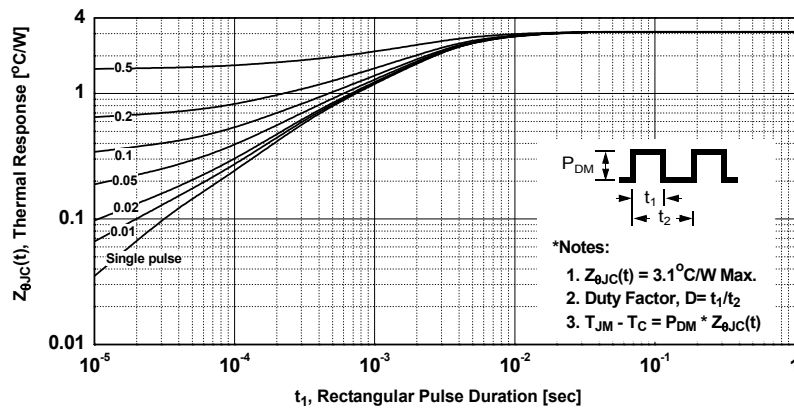




Figure 12. Gate Charge Test Circuit & Waveform



Figure 13. Resistive Switching Test Circuit & Waveforms

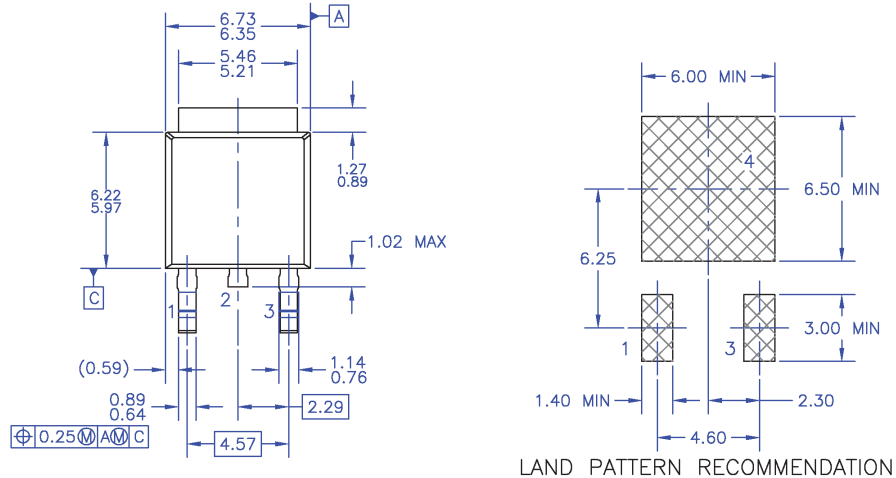


Figure 14. Unclamped Inductive Switching Test Circuit & Waveforms



Figure 15. Peak Diode Recovery  $dv/dt$  Test Circuit & Waveforms

## Mechanical Dimensions



- NOTES: UNLESS OTHERWISE SPECIFIED
- A) THIS PACKAGE CONFORMS TO JEDEC, TO-252, ISSUE C, VARIATION AA.
  - B) ALL DIMENSIONS ARE IN MILLIMETERS.
  - C) DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.
  - D) HEAT SINK TOP EDGE COULD BE IN CHAMFERED CORNERS OR EDGE PROTRUSION.
  - E) PRESENCE OF TRIMMED CENTER LEAD IS OPTIONAL.
  - F) DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH AND TIE BAR EXTRUSIONS.
  - G) LAND PATTERN RECOMMENDATION IS BASED ON IPC7351A STD TO220P1003X238-3N.
  - H) DRAWING NUMBER AND REVISION: MKT-T0252A03REV8

**Figure 16. TO252 (D-PAK), Molded, 3-Lead, Option AA&AB**

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