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# FDC610PZ

## P-Channel PowerTrench® MOSFET

-30V, -4.9A, 42mΩ

### Features

- Max  $r_{DS(on)}$  = 42mΩ at  $V_{GS} = -10V$ ,  $I_D = -4.9A$
- Max  $r_{DS(on)}$  = 75mΩ at  $V_{GS} = -4.5V$ ,  $I_D = -3.7A$
- Low gate charge (17nC typical).
- High performance trench technology for extremely low  $r_{DS(on)}$ .
- SuperSOT™ -6 package: small footprint (72% smaller than standard SO-8) low profile (1mm thick).
- RoHS Compliant

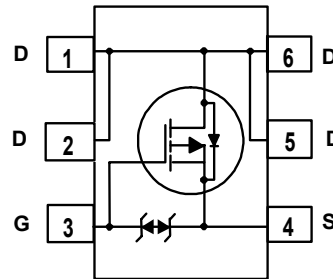
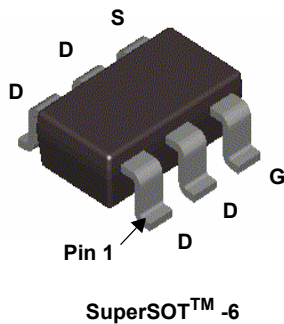


### General Description

This P-Channel MOSFET is produced using Fairchild Semiconductor's advanced PowerTrench® process that has been especially tailored to minimize the on-state resistance and yet maintain low gate charge for superior switching performance. These devices are well suited for battery power applications: load switching and power management, battery charging circuits, and DC/DC conversion.

### Application

- DC - DC Conversion



### MOSFET Maximum Ratings $T_A = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Rated Value	Units
$V_{DS}$	Drain to Source Voltage	-30	V
$V_{GS}$	Gate to Source Voltage	±25	V
$I_D$	Drain Current -Continuous (Note 1a)	-4.9	A
	-Pulsed	-20	
$P_D$	Power Dissipation (Note 1a)	1.6	W
	Power Dissipation (Note 1b)	0.8	
$T_J, T_{STG}$	Operating and Storage Junction Temperature Range	-55 to +150	°C

### Thermal Characteristics

$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1a)	78	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1b)	156	

### Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
.610Z	FDC610PZ	SSOT6	7"	8mm	3000units

## Electrical Characteristics $T_J = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
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### Off Characteristics

$BV_{DSS}$	Drain to Source Breakdown Voltage	$I_D = -250\mu\text{A}, V_{GS} = 0\text{V}$	-30			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	$I_D = -250\mu\text{A}$ , referenced to $25^\circ\text{C}$		-22		mV/ $^\circ\text{C}$
$I_{DSS}$	Zero Gate Voltage Drain Current	$V_{DS} = -24\text{V}, V_{GS} = 0\text{V}$			-1	$\mu\text{A}$
$I_{GSS}$	Gate to Source Leakage Current	$V_{GS} = \pm 25\text{V}, V_{DS} = 0\text{V}$			$\pm 10$	$\mu\text{A}$

### On Characteristics

$V_{GS(th)}$	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}, I_D = -250\mu\text{A}$	-1	-2.2	-3	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	$I_D = -250\mu\text{A}$ , referenced to $25^\circ\text{C}$		6		mV/ $^\circ\text{C}$
$r_{DS(on)}$	Static Drain to Source On Resistance	$V_{GS} = -10\text{V}, I_D = -4.9\text{A}$		36	42	m $\Omega$
		$V_{GS} = -4.5\text{V}, I_D = -3.7\text{A}$		58	75	
		$V_{GS} = -10\text{V}, I_D = -4.9\text{A}, T_J = 125^\circ\text{C}$		50	60	
$g_{FS}$	Forward Transconductance	$V_{DD} = -10\text{V}, I_D = -4.9\text{A}$		15		S

### Dynamic Characteristics

$C_{iss}$	Input Capacitance	$V_{DS} = -15\text{V}, V_{GS} = 0\text{V}, f = 1\text{MHz}$		755	1005	pF
$C_{oss}$	Output Capacitance			145	195	pF
$C_{rss}$	Reverse Transfer Capacitance			125	190	pF
$R_g$	Gate Resistance		$f = 1\text{MHz}$		13	

### Switching Characteristics

$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = -15\text{V}, I_D = -4.9\text{A}, V_{GS} = -10\text{V}, R_{GEN} = 6\Omega$		7	14	ns	
$t_r$	Rise Time			4	10	ns	
$t_{d(off)}$	Turn-Off Delay Time			33	53	ns	
$t_f$	Fall Time			23	37	ns	
$Q_g$	Total Gate Charge		$V_{GS} = 0\text{V to } -10\text{V}$		17	24	nC
$Q_g$	Total Gate Charge	$V_{GS} = 0\text{V to } -4.5\text{V}$	$V_{DD} = -15\text{V}, I_D = -4.9\text{A}$		9	13	nC
$Q_{gs}$	Gate to Source Gate Charge				2.9		nC
$Q_{gd}$	Gate to Drain "Miller" Charge				4.3		nC

### Drain-Source Diode Characteristics

$I_S$	Maximum Continuous Drain-Source Diode Forward Current			-1.3		A
$V_{SD}$	Source to Drain Diode Forward Voltage	$V_{GS} = 0\text{V}, I_S = -1.3\text{A}$ (Note 2)		-0.8	-1.2	V
$t_{rr}$	Reverse Recovery Time	$I_F = -4.9\text{A}, di/dt = 100\text{A}/\mu\text{s}$		19	35	ns
$Q_{rr}$	Reverse Recovery Charge			9	18	nC

#### Notes:

1.  $R_{\theta JA}$  is determined with the device mounted on a  $1\text{in}^2$  pad 2 oz copper pad on a  $1.5 \times 1.5\text{in.}$  board of FR-4 material.  $R_{\theta JC}$  is guaranteed by design while  $R_{\theta CA}$  is determined by the user's board design.



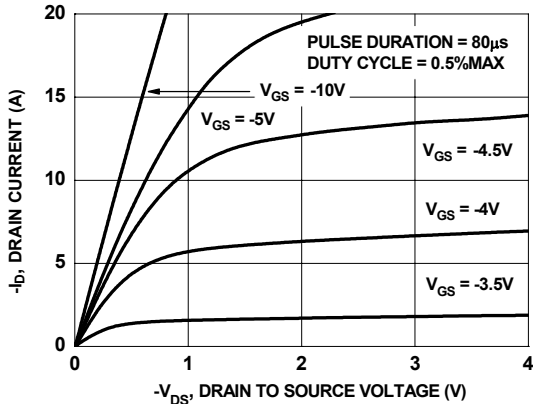
a.  $78^\circ\text{C/W}$  when mounted on a  $1\text{in}^2$  pad of 2 oz copper.



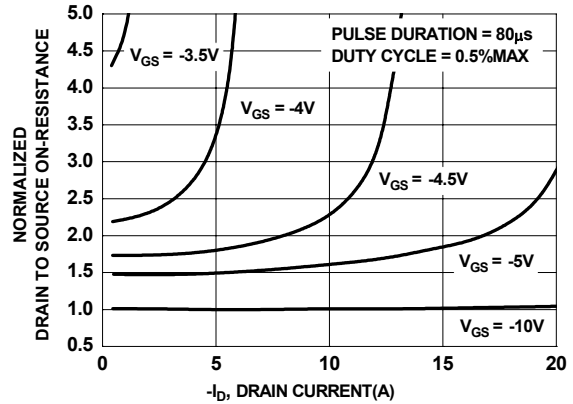
b.  $156^\circ\text{C/W}$  when mounted on a minimum pad of 2 oz copper.

2. Pulse Test: Pulse Width <  $300\mu\text{s}$ , Duty cycle < 2.0%.

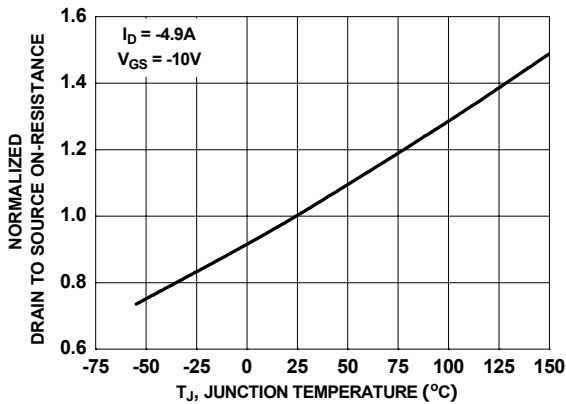
**Typical Characteristics**  $T_J = 25^\circ\text{C}$  unless otherwise noted



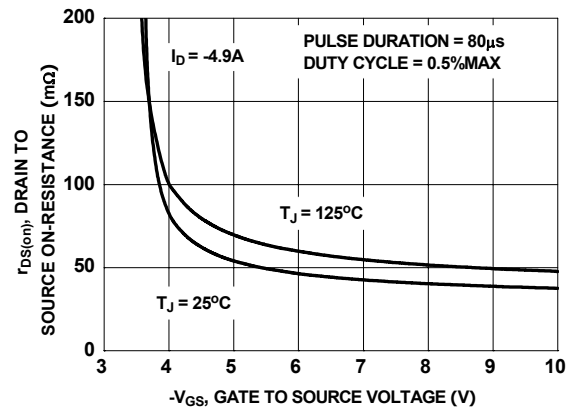
**Figure 1. On-Region Characteristics**



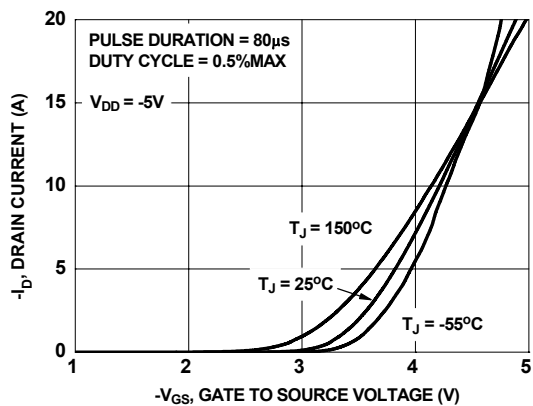
**Figure 2. Normalized On-Resistance vs Drain Current and Gate Voltage**



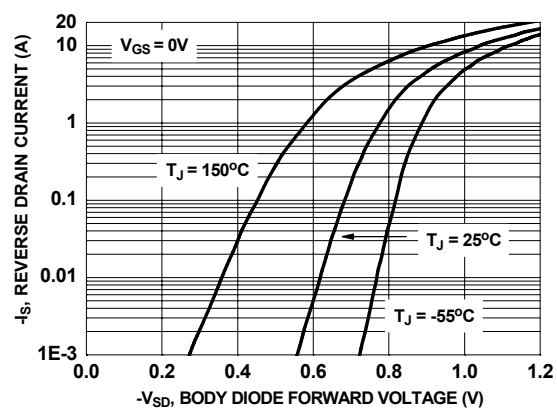
**Figure 3. Normalized On-Resistance vs Junction Temperature**



**Figure 4. On-Resistance vs Gate to Source Voltage**

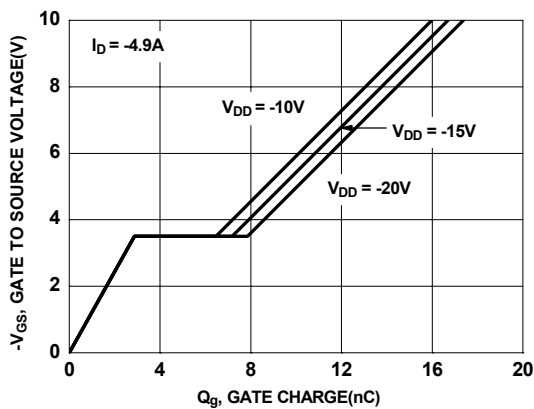


**Figure 5. Transfer Characteristics**

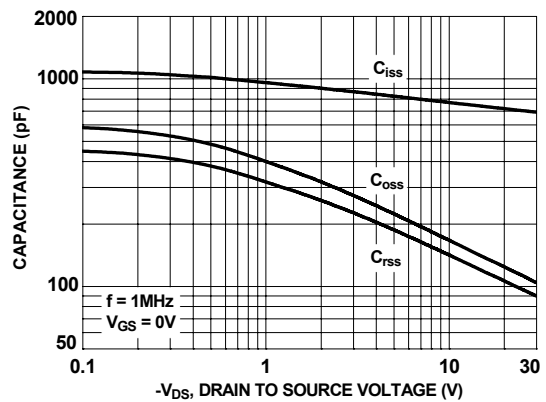


**Figure 6. Source to Drain Diode Forward Voltage vs Source Current**

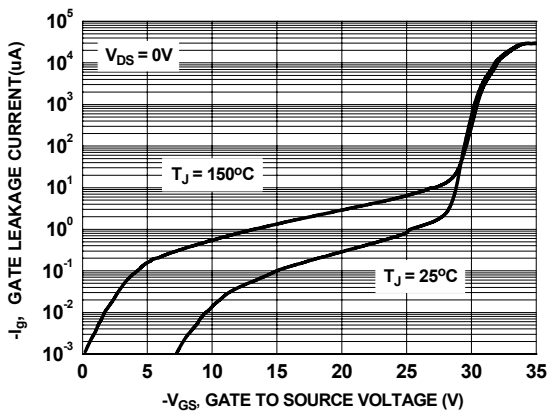
**Typical Characteristics**  $T_J = 25^\circ\text{C}$  unless otherwise noted



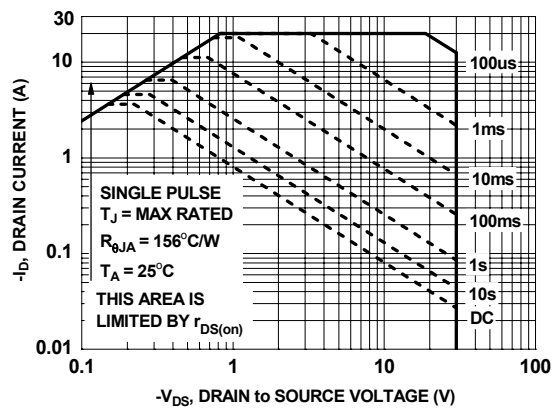
**Figure 7. Gate Charge Characteristics**



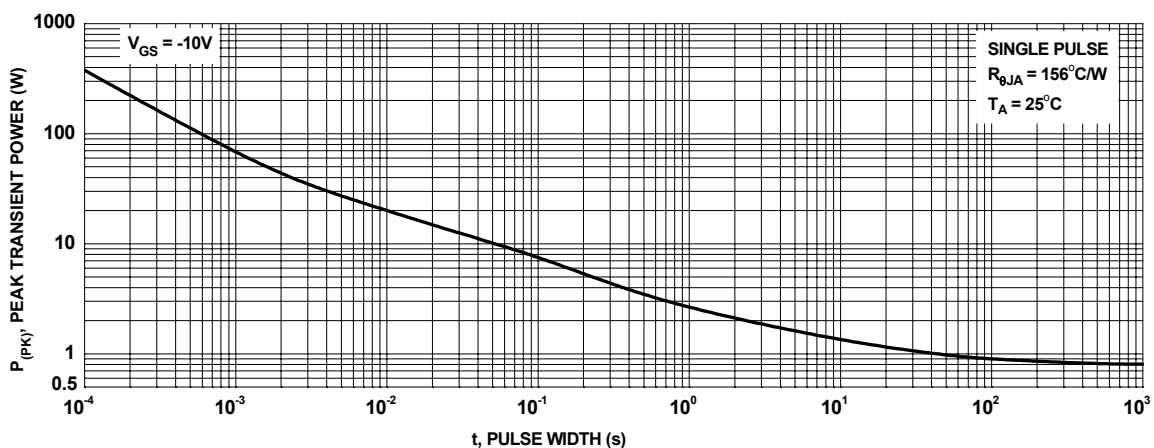
**Figure 8. Capacitance vs Drain to Source Voltage**



**Figure 9. Gate Leakage Current vs Gate to Source Voltage**

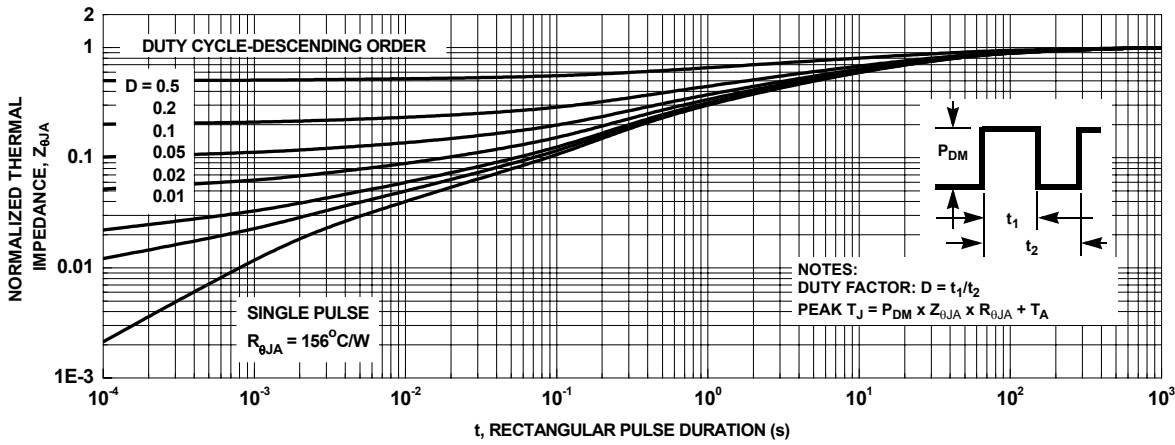


**Figure 10. Forward Bias Safe Operating Area**



**Figure 11. Single Pulse Maximum Power Dissipation**

**Typical Characteristics**  $T_J = 25^\circ\text{C}$  unless otherwise noted



**Figure 12. Transient Thermal Response Curve**



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