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Kind regards,

Team Nexperia

# PSMN1R8-40YLC

## N-channel 40 V 1.8 mΩ logic level MOSFET in LFPAK using NextPower technology

22 August 2012 Product data sheet

## 1. Product profile

### 1.1 General description

Logic level enhancement mode N-channel MOSFET in LFPAK package. This product is designed and qualified for use in a wide range of industrial, communications and domestic equipment.

### 1.2 Features and benefits

- High reliability Power SO8 package, qualified to 175°C
- Optimised for 4.5V Gate drive utilising NextPower Superjunction technology
- Ultra low QG, QGD, & QOSS for high system efficiencies at low and high loads
- Ultra low Rdson and low parasitic inductance

### 1.3 Applications

- DC-to-DC converters
- Load switching
- Power OR-ing
- Server power supplies
- Sync rectifier

### 1.4 Quick reference data

**Table 1. Quick reference data**

| Symbol | Parameter | Conditions | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| $V_{DS}$ | drain-source voltage | 25 °C ≤ $T_j$ ≤ 175 °C | | - | - | 40 | V |
| $I_D$ | drain current | $T_{mb}$ = 25 °C; $V_{GS}$ = 10 V; Fig. 1 | [1] | - | - | 100 | A |
| $P_{tot}$ | total power dissipation | $T_{mb}$ = 25 °C; Fig. 2 | | - | - | 272 | W |
| $T_j$ | junction temperature | | | -55 | - | 175 | °C |
| **Static characteristics** | | | | | | | |
| $R_{DSon}$ | drain-source on-state resistance | $V_{GS}$ = 4.5 V; $I_D$ = 25 A; $T_j$ = 25 °C; Fig. 12 | | - | 1.8 | 2.1 | mΩ |
| | | $V_{GS}$ = 10 V; $I_D$ = 25 A; $T_j$ = 25 °C; Fig. 12 | | - | 1.5 | 1.8 | mΩ |
| **Dynamic characteristics** | | | | | | | |
| $Q_{GD}$ | gate-drain charge | $V_{GS}$ = 4.5 V; $I_D$ = 25 A; $V_{DS}$ = 20 V; Fig. 15; Fig. 14 | | - | 10.9 | - | nC |

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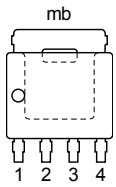
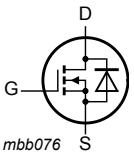
| Symbol | Parameter | Conditions | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| $Q_{G(tot)}$ | total gate charge | $V_{GS}$ = 4.5 V; $I_D$ = 25 A; $V_{DS}$ = 20 V; Fig. 15; Fig. 14 | | - | 45 | - | nC |

[1] Continuous current is limited by package.

## 2. Pinning information

**Table 2. Pinning information**

| Pin | Symbol | Description | Simplified outline | Graphic symbol |
|---|---|---|---|---|
| 1 | S | source |   **LFPAK; Power-SO8 (SOT669)** |   |
| 2 | S | source | | |
| 3 | S | source | | |
| 4 | G | gate | | |
| mb | D | mounting base; connected to drain | | |

## 3. Ordering information

**Table 3. Ordering information**

| Type number | Package | | |
|---|---|---|---|
| | Name | Description | Version |
| PSMN1R8-40YLC | LFPAK; Power-SO8 | plastic single-ended surface-mounted package; 4 leads | SOT669 |

## 4. Limiting values

**Table 4. Limiting values**

*In accordance with the Absolute Maximum Rating System (IEC 60134).*

| Symbol | Parameter | Conditions | | Min | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{DS}$ | drain-source voltage | 25 °C ≤ $T_j$ ≤ 175 °C | | - | 40 | V |
| $V_{DGR}$ | drain-gate voltage | 25 °C ≤ $T_j$ ≤ 175 °C; $R_{GS}$ = 20 kΩ | | - | 40 | V |
| $V_{GS}$ | gate-source voltage | | | -20 | 20 | V |
| $I_D$ | drain current | $V_{GS}$ = 10 V; $T_{mb}$ = 25 °C; Fig. 1 | [1] | - | 100 | A |
| | | $V_{GS}$ = 10 V; $T_{mb}$ = 100 °C; Fig. 1 | [1] | - | 100 | A |
| $I_{DM}$ | peak drain current | pulsed; $t_p$ ≤ 10 µs; $T_{mb}$ = 25 °C; Fig. 4 | | - | 1128 | A |
| $P_{tot}$ | total power dissipation | $T_{mb}$ = 25 °C; Fig. 2 | | - | 272 | W |
| $T_{stg}$ | storage temperature | | | -55 | 175 | °C |
| $T_j$ | junction temperature | | | -55 | 175 | °C |
| $T_{sld(M)}$ | peak soldering temperature | | | - | 260 | °C |

| Symbol | Parameter | Conditions | | Min | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{ESD}$ | electrostatic discharge voltage | MM (JEDEC JESD22-A115) | | 890 | - | V |
| **Source-drain diode** | | | | | | |
| $I_S$ | source current | $T_{mb}$ = 25 °C | [1] | - | 100 | A |
| $I_{SM}$ | peak source current | pulsed; $t_p \leq 10$ µs; $T_{mb}$ = 25 °C | | - | 1128 | A |
| **Avalanche ruggedness** | | | | | | |
| $E_{DS(AL)S}$ | non-repetitive drain-source avalanche energy | $V_{GS}$ = 10 V; $T_{j(init)}$ = 25 °C; $I_D$ = 100 A; $V_{sup} \leq 40$ V; $R_{GS}$ = 50 Ω; unclamped; Fig. 3 | | - | 248 | mJ |

[1] Continuous current is limited by package.

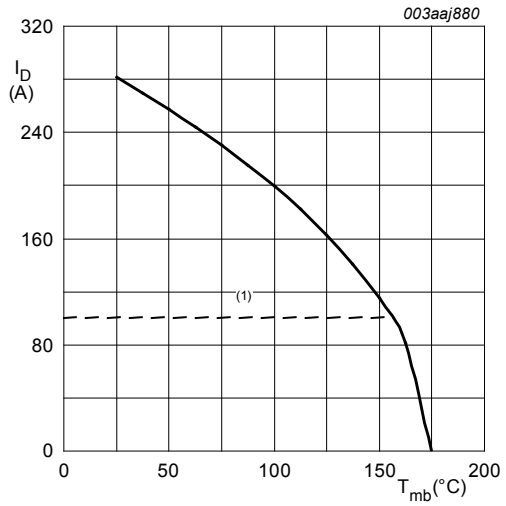



**Fig. 1. Continuous drain current as a function of mounting base temperature**

$V_{GS} \geq 10\,V$

(1) Capped at 100 A due to package.

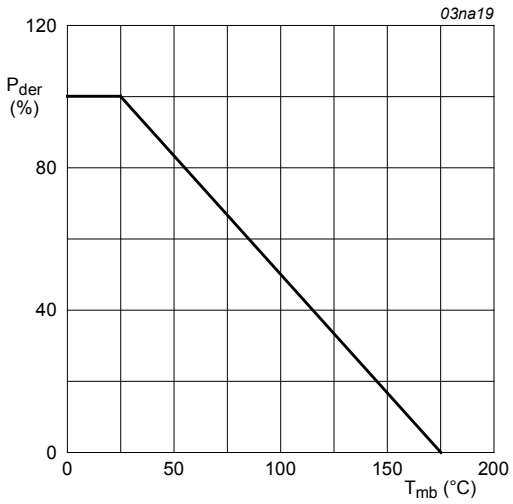



**Fig. 2. Normalized total power dissipation as a function of mounting base temperature**

$$P_{der} = \frac{P_{tot}}{P_{tot(25°C)}} \times 100\,\%$$

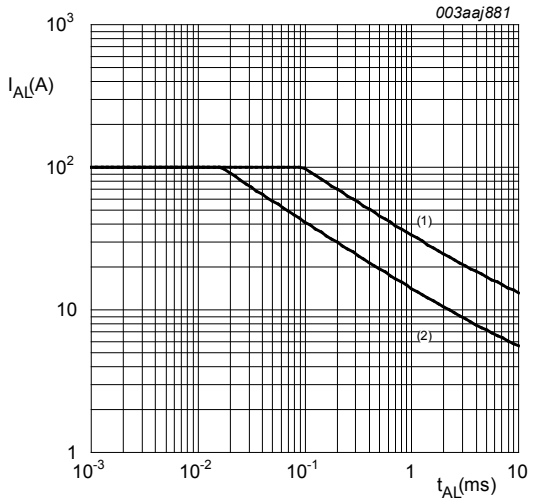



**Fig. 3. Single pulse avalanche rating; avalanche current as a function of avalanche time**

(1) $T_{j\ (init)} = 25°C$; (2) $T_{j\ (init)} = 100°C$

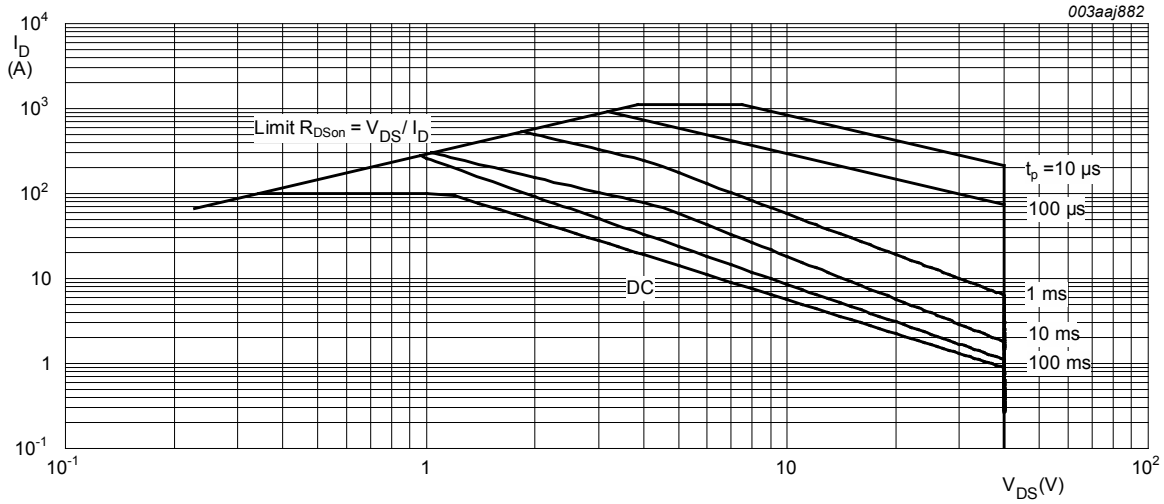



**Fig. 4. Safe operating area; continuous and peak drain currents as a function of drain-source voltage**

$T_{mb} = 25°C$; $I_{DM}$ *is a single pulse*

## 5. Thermal characteristics

**Table 5. Thermal characteristics**

| Symbol | Parameter | Conditions | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| $R_{th(j\text{-}mb)}$ | thermal resistance from junction to mounting base | Fig. 5 | | - | 0.45 | 0.55 | K/W |

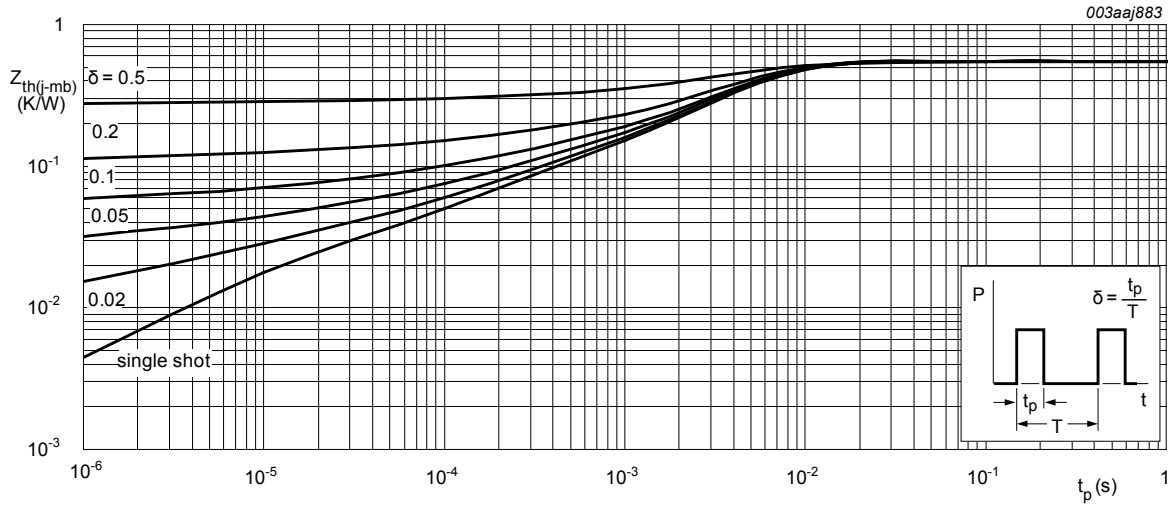



**Fig. 5. Transient thermal impedance from junction to mounting base as a function of pulse duration**

# 6. Characteristics

**Table 6. Characteristics**

| Symbol | Parameter | Conditions | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| **Static characteristics** | | | | | | | |
| $V_{(BR)DSS}$ | drain-source breakdown voltage | $I_D$ = 250 µA; $V_{GS}$ = 0 V; $T_j$ = 25 °C | | 40 | - | - | V |
| | | $I_D$ = 250 µA; $V_{GS}$ = 0 V; $T_j$ = -55 °C | | 36 | - | - | V |
| $V_{GS(th)}$ | gate-source threshold voltage | $I_D$ = 1 mA; $V_{DS}$ = $V_{GS}$; $T_j$ = 25 °C; Fig. 10 | | 1.05 | 1.45 | 1.95 | V |
| | | $I_D$ = 10 mA; $V_{DS}$ = $V_{GS}$; $T_j$ = 150 °C; Fig. 11 | | 0.5 | - | - | V |
| | | $I_D$ = 1 mA; $V_{DS}$ = $V_{GS}$; $T_j$ = -55 °C; Fig. 11 | | - | - | 2.25 | V |
| $I_{DSS}$ | drain leakage current | $V_{DS}$ = 40 V; $V_{GS}$ = 0 V; $T_j$ = 25 °C | | - | - | 1 | µA |
| | | $V_{DS}$ = 40 V; $V_{GS}$ = 0 V; $T_j$ = 150 °C | | - | - | 100 | µA |
| $I_{GSS}$ | gate leakage current | $V_{GS}$ = 16 V; $V_{DS}$ = 0 V; $T_j$ = 25 °C | | - | - | 100 | nA |
| | | $V_{GS}$ = -16 V; $V_{DS}$ = 0 V; $T_j$ = 25 °C | | - | - | 100 | nA |
| $R_{DSon}$ | drain-source on-state resistance | $V_{GS}$ = 4.5 V; $I_D$ = 25 A; $T_j$ = 25 °C; Fig. 12 | | - | 1.8 | 2.1 | mΩ |
| | | $V_{GS}$ = 4.5 V; $I_D$ = 25 A; $T_j$ = 150 °C; Fig. 12; Fig. 13 | | - | - | 3.6 | mΩ |
| | | $V_{GS}$ = 10 V; $I_D$ = 25 A; $T_j$ = 25 °C; Fig. 12 | | - | 1.5 | 1.8 | mΩ |
| | | $V_{GS}$ = 10 V; $I_D$ = 25 A; $T_j$ = 150 °C; Fig. 12; Fig. 13 | | - | - | 3.25 | mΩ |

| Symbol | Parameter | Conditions | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| $R_G$ | gate resistance | f = 1 MHz | | 0.5 | 1 | 2 | Ω |
| **Dynamic characteristics** | | | | | | | |
| $Q_{G(tot)}$ | total gate charge | $I_D$ = 25 A; $V_{DS}$ = 20 V; $V_{GS}$ = 10 V; Fig. 14; Fig. 15 | | - | 96 | - | nC |
| | | $I_D$ = 25 A; $V_{DS}$ = 20 V; $V_{GS}$ = 4.5 V; Fig. 15; Fig. 14 | | - | 45 | - | nC |
| | | $I_D$ = 0 A; $V_{DS}$ = 0 V; $V_{GS}$ = 10 V | | - | 88 | - | nC |
| $Q_{GS}$ | gate-source charge | $I_D$ = 25 A; $V_{DS}$ = 20 V; $V_{GS}$ = 4.5 V; Fig. 15; Fig. 14 | | - | 15.5 | - | nC |
| $Q_{GS(th)}$ | pre-threshold gate-source charge | | | - | 8.4 | - | nC |
| $Q_{GS(th-pl)}$ | post-threshold gate-source charge | | | - | 7.1 | - | nC |
| $Q_{GD}$ | gate-drain charge | | | - | 10.9 | - | nC |
| $V_{GS(pl)}$ | gate-source plateau voltage | $I_D$ = 25 A; $V_{DS}$ = 20 V; Fig. 15; Fig. 14 | | - | 2.7 | - | V |
| $C_{iss}$ | input capacitance | $V_{DS}$ = 20 V; $V_{GS}$ = 0 V; f = 1 MHz; $T_j$ = 25 °C; Fig. 16 | | - | 6680 | - | pF |
| $C_{oss}$ | output capacitance | | | - | 825 | - | pF |
| $C_{rss}$ | reverse transfer capacitance | | | - | 310 | - | pF |
| $t_{d(on)}$ | turn-on delay time | $V_{DS}$ = 20 V; $R_L$ = 0.8 Ω; $V_{GS}$ = 4.5 V; $R_{G(ext)}$ = 5 Ω | | - | 32.2 | - | ns |
| $t_r$ | rise time | | | - | 37 | - | ns |
| $t_{d(off)}$ | turn-off delay time | | | - | 62.5 | - | ns |
| $t_f$ | fall time | | | - | 31.7 | - | ns |
| $Q_{oss}$ | output charge | $V_{GS}$ = 0 V; $V_{DS}$ = 20 V; f = 1 MHz; $T_j$ = 25 °C | | - | 30 | - | nC |
| **Source-drain diode** | | | | | | | |
| $V_{SD}$ | source-drain voltage | $I_S$ = 25 A; $V_{GS}$ = 0 V; $T_j$ = 25 °C; Fig. 17 | | - | 0.77 | 1.1 | V |
| $t_{rr}$ | reverse recovery time | $I_S$ = 25 A; $dI_S/dt$ = -100 A/µs; $V_{GS}$ = 0 V; $V_{DS}$ = 20 V | | - | 37 | - | ns |
| $Q_r$ | recovered charge | | | - | 43 | - | nC |
| $t_a$ | reverse recovery rise time | $V_{GS}$ = 0 V; $I_S$ = 25 A; $dI_S/dt$ = -100 A/µs; $V_{DS}$ = 20 V; Fig. 18 | | - | 21 | - | ns |
| $t_b$ | reverse recovery fall time | | | - | 16 | - | ns |

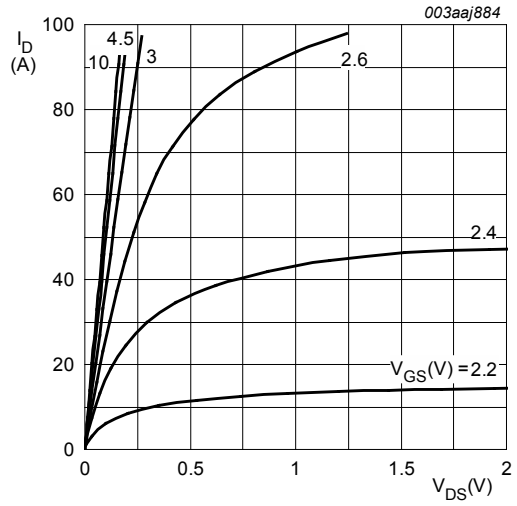



**Fig. 6. Output characteristics; drain current as a function of drain-source voltage; typical values**

$T_j = 25°C$

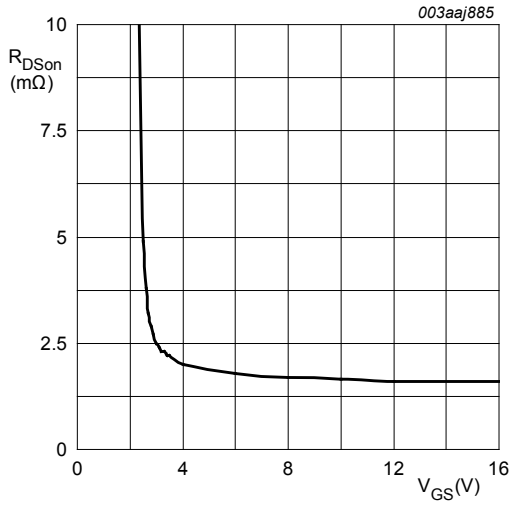



**Fig. 7. Drain-source on-state resistance as a function of gate-source voltage; typical values**

$T_j = 25°C;\ I_D = 25A$

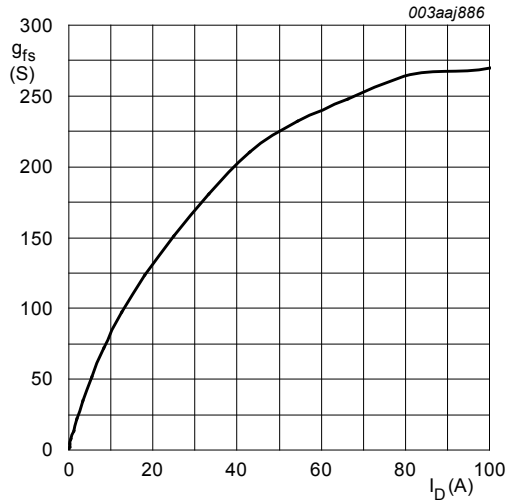



**Fig. 8. Forward transconductance as a function of drain current; typical values**

$T_j = 25°C;\ V_{DS} = 10V$

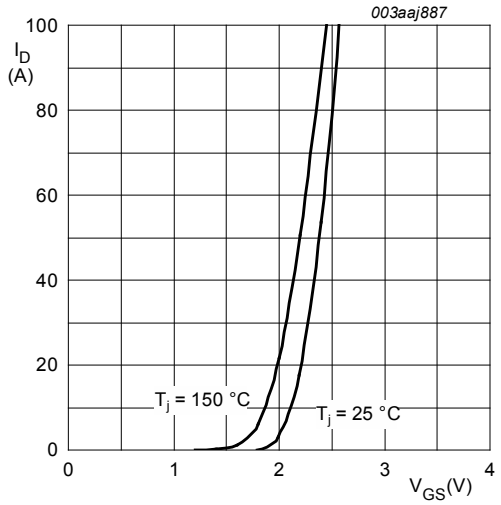



**Fig. 9. Transfer characteristics; drain current as a function of gate-source voltage; typical values**

$V_{DS} = 10V$

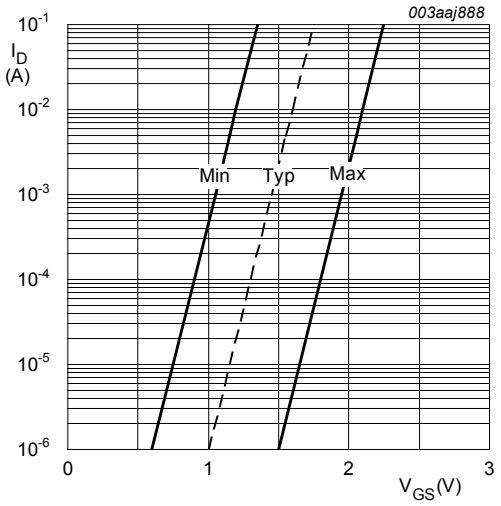



**Fig. 10. Sub-threshold drain current as a function of gate-source voltage**

$T_j = 25°C;\ V_{DS} = 5V$

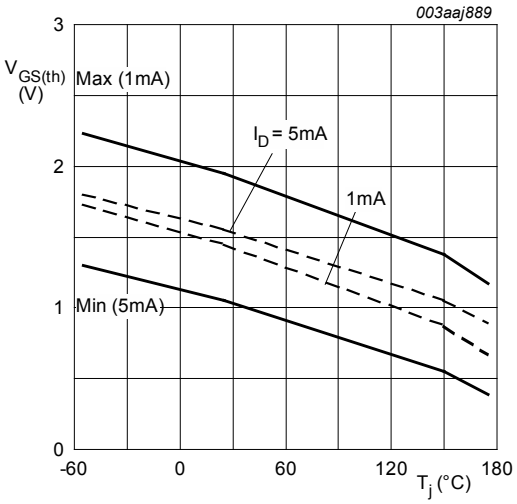



**Fig. 11. Gate-source threshold voltage as a function of junction temperature**

$V_{DS} = V_{GS}$

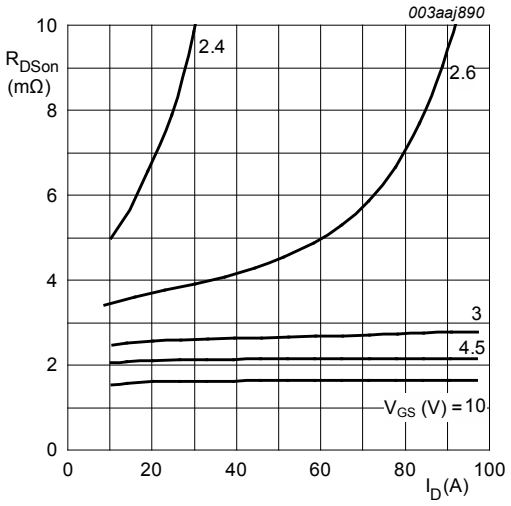



**Fig. 12. Drain-source on-state resistance as a function of drain current; typical values**

$T_j = 25°C$

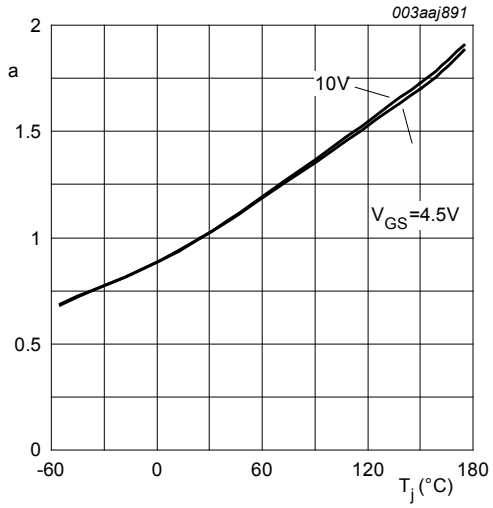



**Fig. 13. Normalized drain-source on-state resistance factor as a function of junction temperature**

$$a = \frac{R_{DSon}}{R_{DSon\,(25°C)}}$$

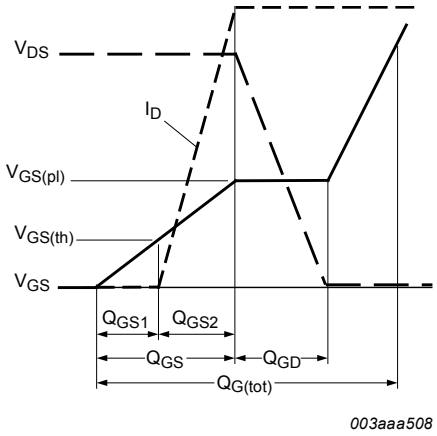



Fig. 14. Gate charge waveform definitions

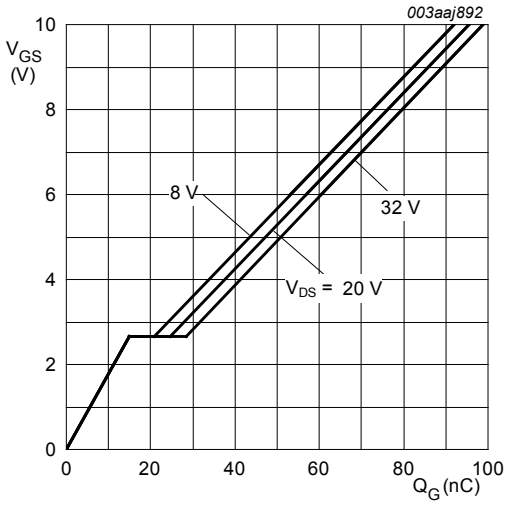



Fig. 15. Gate-source voltage as a function of gate charge; typical values

$T_j = 25°C;\ I_D = 25A$

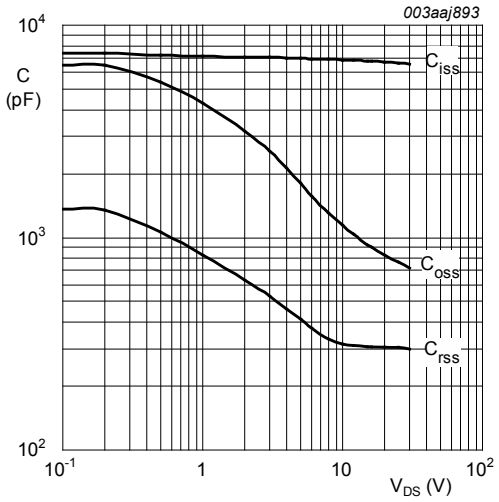



Fig. 16. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values

$V_{GS} = 0V;\ f = 1MHz$

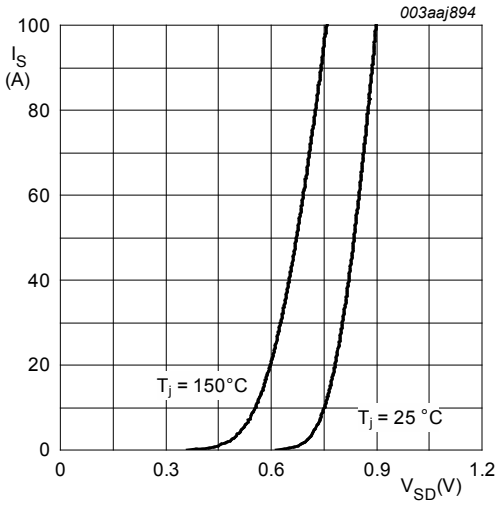



Fig. 17. Source current as a function of source-drain voltage; typical values

$V_{GS} = 0V$

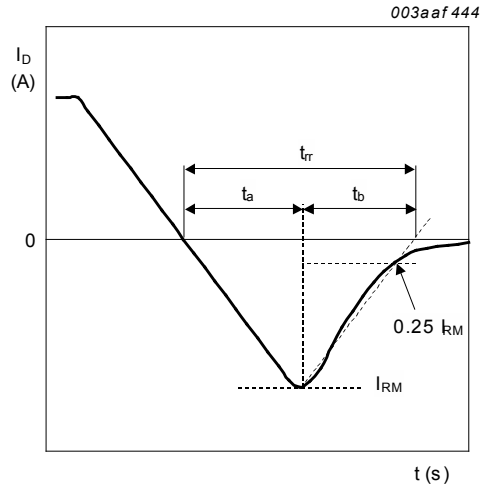
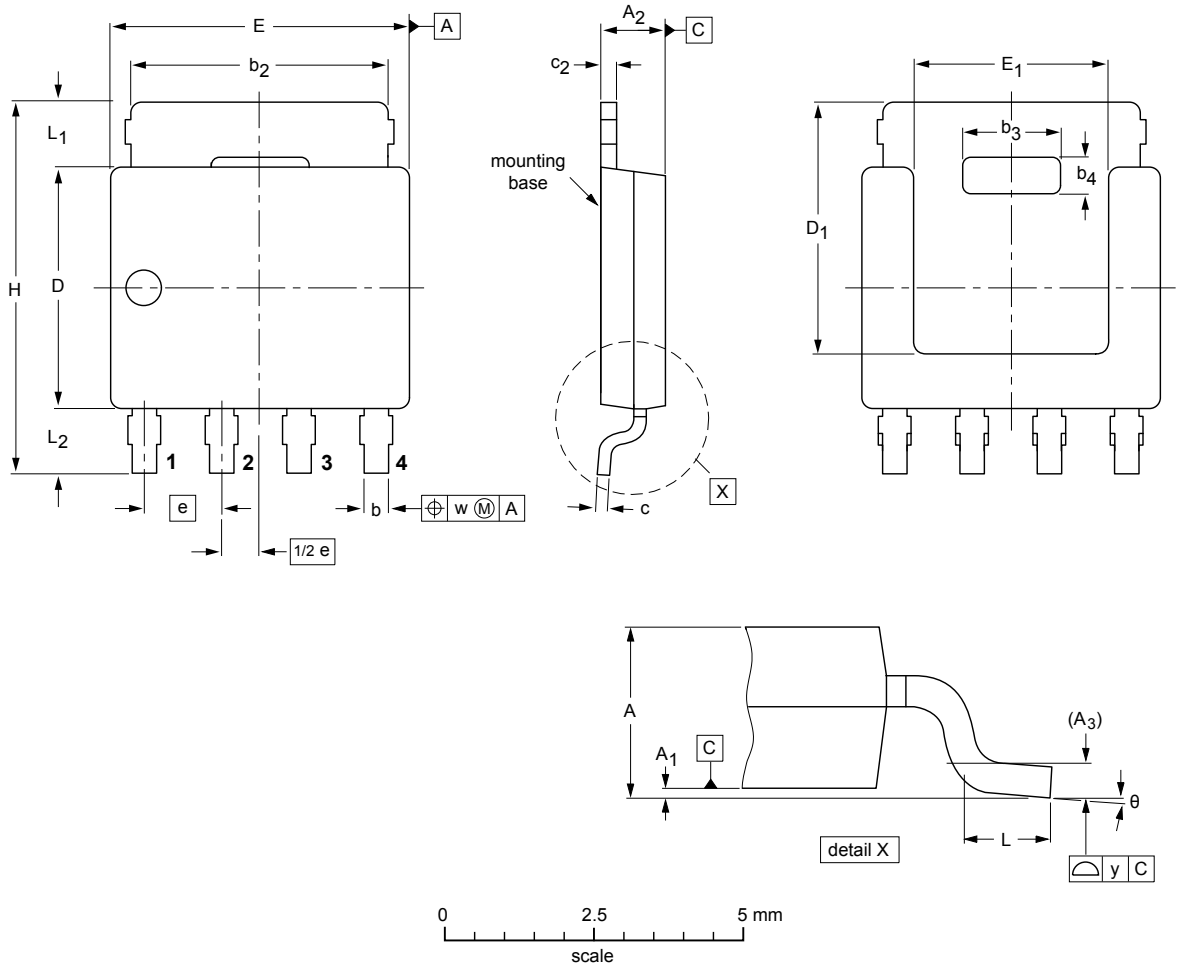



**Fig. 18. Reverse recovery timing definition**

# 7. Package outline

**Plastic single-ended surface-mounted package (LFPAK; Power-SO8); 4 leads** **SOT669**




**DIMENSIONS (mm are the original dimensions)**

| UNIT | A | $A_1$ | $A_2$ | $A_3$ | b | $b_2$ | $b_3$ | $b_4$ | c | $c_2$ | $D^{(1)}$ | $D_1^{(1)}$ max | $E^{(1)}$ | $E_1^{(1)}$ | e | H | L | $L_1$ | $L_2$ | w | y | θ |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| mm | 1.20<br>1.01 | 0.15<br>0.00 | 1.10<br>0.95 | 0.25 | 0.50<br>0.35 | 4.41<br>3.62 | 2.2<br>2.0 | 0.9<br>0.7 | 0.25<br>0.19 | 0.30<br>0.24 | 4.10<br>3.80 | 4.20 | 5.0<br>4.8 | 3.3<br>3.1 | 1.27 | 6.2<br>5.8 | 0.85<br>0.40 | 1.3<br>0.8 | 1.3<br>0.8 | 0.25 | 0.1 | 8°<br>0° |

**Note**

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

| OUTLINE VERSION | REFERENCES | | | | EUROPEAN PROJECTION | ISSUE DATE |
|---|---|---|---|---|---|---|
| | IEC | JEDEC | JEITA | | | |
| SOT669 | | MO-235 | | | | ~~06-03-16~~<br>11-03-25 |

**Fig. 19. Package outline LFPAK; Power-SO8 (SOT669)**

# 8. Legal information

## 8.1 Data sheet status

| Document status [1][2] | Product status [3] | Definition |
|---|---|---|
| Objective [short] data sheet | Development | This document contains data from the objective specification for product development. |
| Preliminary [short] data sheet | Qualification | This document contains data from the preliminary specification. |
| Product [short] data sheet | Production | This document contains the product specification. |

[1] Please consult the most recently issued document before initiating or completing a design.
[2] The term 'short data sheet' is explained in section "Definitions".
[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

## 8.2 Definitions

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