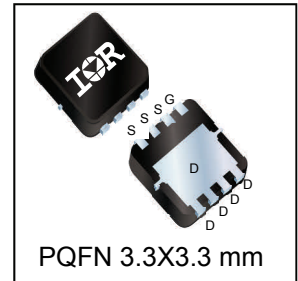
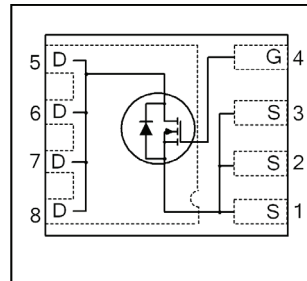


V_{DSS}	30	V
$V_{GS\ max}$	±20	V
$R_{DS(on)\ max}$ (@ $V_{GS} = 10V$)	6.1	mΩ
(@ $V_{GS} = 4.5V$)	8.8	
Q_g (typical)	13	nC
I_D (@ $T_C(Bottom) = 25°C$)	24 Ⓞ	A

HEXFET® Power MOSFET



Applications

- Charge and Discharge Switch for Notebook PC Battery Application
- System/Load Switch
- Synchronous MOSFET for Buck Converters

Features

Low Thermal Resistance to PCB (<3.8°C/W)
Low Profile (<1.05 mm)
Industry-Standard Pinout
Compatible with Existing Surface Mount Techniques
RoHS Compliant Containing no Lead, no Bromide and no Halogen
MSL1, Consumer Qualification

results in
 ⇒

Benefits

Enable better thermal dissipation
Increased Power Density
Multi-Vendor Compatibility
Easier Manufacturing
Environmentally Friendlier
Increased Reliability

Base part number	Package Type	Standard Pack		Orderable Part Number
		Form	Quantity	
IRFHM8329PbF	PQFN 3.3 mm x 3.3 mm	Tape and Reel	4000	IRFHM8329TRPbF

Absolute Maximum Ratings

	Parameter	Max.	Units
V_{GS}	Gate-to-Source Voltage	± 20	V
$I_D @ T_A = 25°C$	Continuous Drain Current, $V_{GS} @ 10V$	16	A
$I_D @ T_A = 70°C$	Continuous Drain Current, $V_{GS} @ 10V$	13	
$I_D @ T_C(Bottom) = 25°C$	Continuous Drain Current, $V_{GS} @ 10V$	57 [Ⓞ] [Ⓡ]	
$I_D @ T_C(Bottom) = 100°C$	Continuous Drain Current, $V_{GS} @ 10V$	36 [Ⓞ] [Ⓡ]	
$I_D @ T_C = 25°C$	Continuous Drain Current, $V_{GS} @ 10V$ (Source Bonding Technology Limited)	24 [Ⓡ]	
I_{DM}	Pulsed Drain Current ^①	230	
$P_D @ T_A = 25°C$	Power Dissipation ^⑤	2.6	W
$P_D @ T_C(Bottom) = 25°C$	Power Dissipation ^⑤	33	
	Linear Derating Factor ^⑤	0.021	W/°C
T_J T_{STG}	Operating Junction and Storage Temperature Range	-55 to + 150	°C

Notes ^① through [Ⓡ] are on page 9

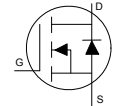
Static @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
BV _{DSS}	Drain-to-Source Breakdown Voltage	30	—	—	V	V _{GS} = 0V, I _D = 250μA
ΔBV _{DSS} /ΔT _J	Breakdown Voltage Temp. Coefficient	—	21	—	mV/°C	Reference to 25°C, I _D = 1mA
R _{DS(on)}	Static Drain-to-Source On-Resistance	—	4.8	6.1	mΩ	V _{GS} = 10V, I _D = 20A ③
		—	6.8	8.8		V _{GS} = 4.5V, I _D = 16A ③
V _{GS(th)}	Gate Threshold Voltage	1.2	1.7	2.2	V	V _{DS} = V _{GS} , I _D = 25μA
ΔV _{GS(th)}	Gate Threshold Voltage Coefficient	—	-6.0	—	mV/°C	
I _{DSS}	Drain-to-Source Leakage Current	—	—	1.0	μA	V _{DS} = 24V, V _{GS} = 0V
		—	—	150		V _{DS} = 24V, V _{GS} = 0V, T _J = 125°C
I _{GSS}	Gate-to-Source Forward Leakage	—	—	100	nA	V _{GS} = 20V
	Gate-to-Source Reverse Leakage	—	—	-100		V _{GS} = -20V
g _{fs}	Forward Transconductance	56	—	—	S	V _{DS} = 10V, I _D = 20A
Q _g	Total Gate Charge	—	26	—	nC	V _{GS} = 10V, V _{DS} = 15V, I _D = 20A
Q _g	Total Gate Charge	—	13	20	nC	V _{DS} = 15V V _{GS} = 4.5V I _D = 20A
Q _{gs1}	Pre-V _{th} Gate-to-Source Charge	—	2.9	—		
Q _{gs2}	Post-V _{th} Gate-to-Source Charge	—	2.0	—		
Q _{gd}	Gate-to-Drain Charge	—	4.6	—		
Q _{godr}	Gate Charge Overdrive	—	3.5	—		
Q _{sw}	Switch Charge (Q _{gs2} + Q _{gd})	—	6.6	—		
Q _{oss}	Output Charge	—	7.8	—	nC	V _{DS} = 16V, V _{GS} = 0V
R _G	Gate Resistance	—	1.4	—	Ω	
t _{d(on)}	Turn-On Delay Time	—	14	—	ns	V _{DD} = 15V, V _{GS} = 4.5V I _D = 20A R _G = 1.8Ω
t _r	Rise Time	—	74	—		
t _{d(off)}	Turn-Off Delay Time	—	14	—		
t _f	Fall Time	—	14	—		
C _{iss}	Input Capacitance	—	1710	—	pF	V _{GS} = 0V V _{DS} = 10V f = 1.0MHz
C _{oss}	Output Capacitance	—	360	—		
C _{rss}	Reverse Transfer Capacitance	—	180	—		

Avalanche Characteristics

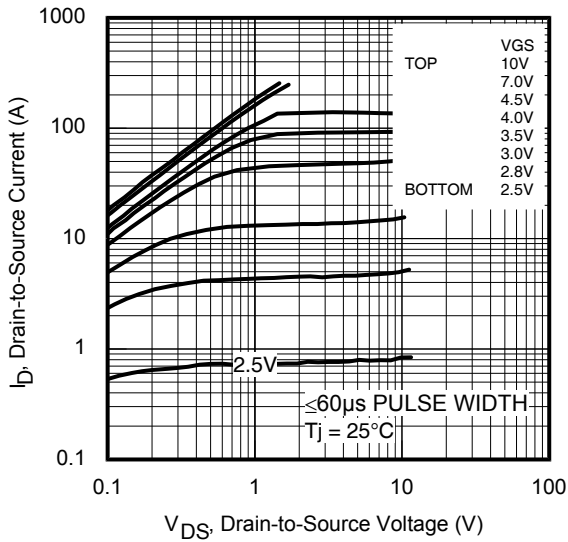
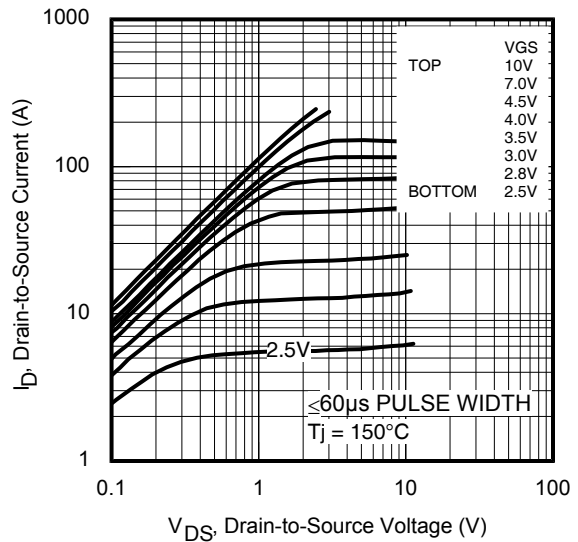
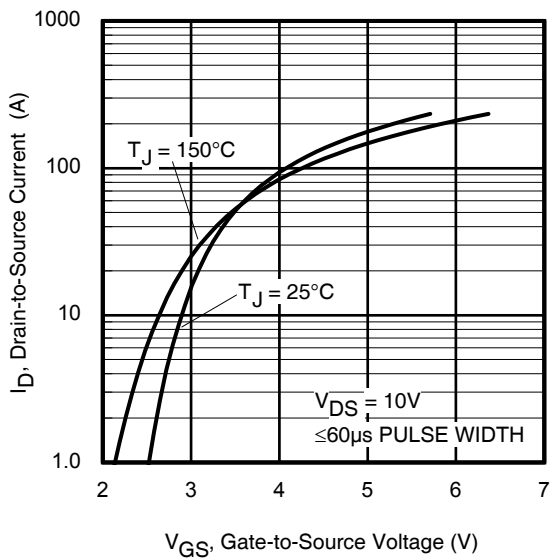
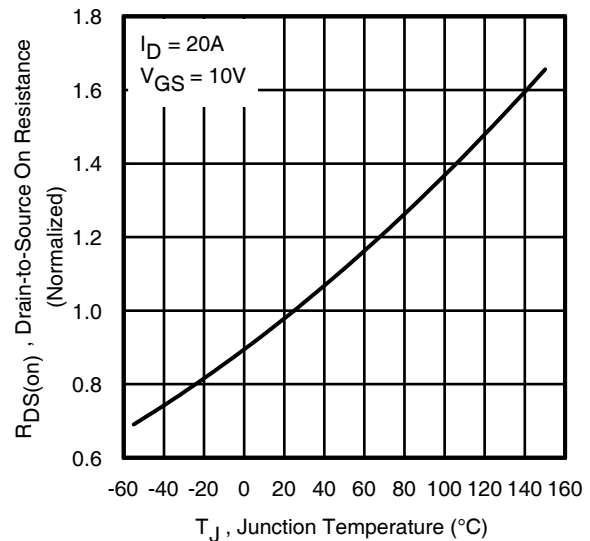
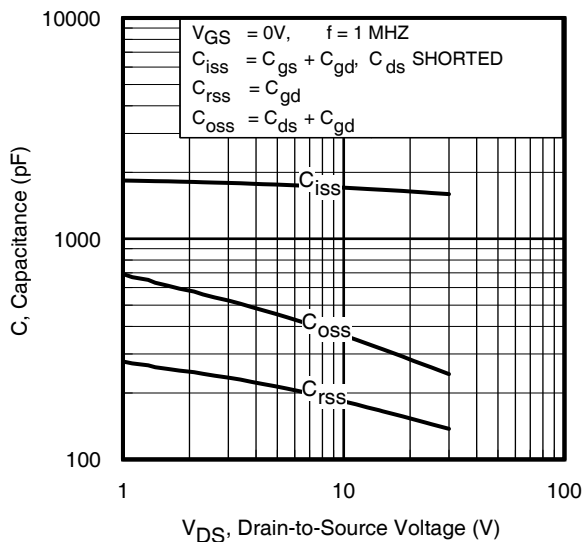
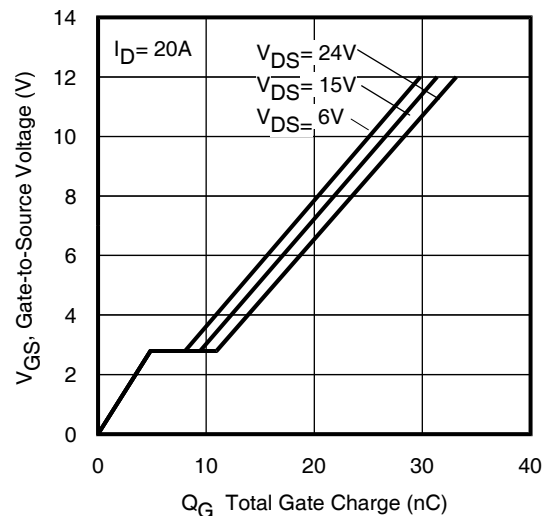
	Parameter	Typ.	Max.	Units
E _{AS}	Single Pulse Avalanche Energy ②	—	43	mJ
I _{AR}	Avalanche Current ①	—	20	A

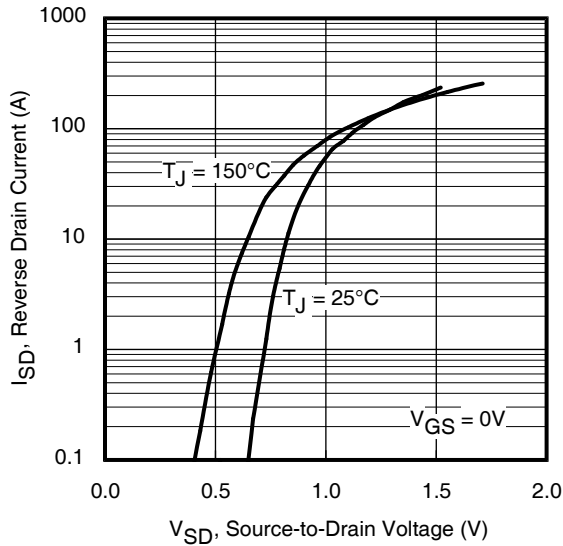
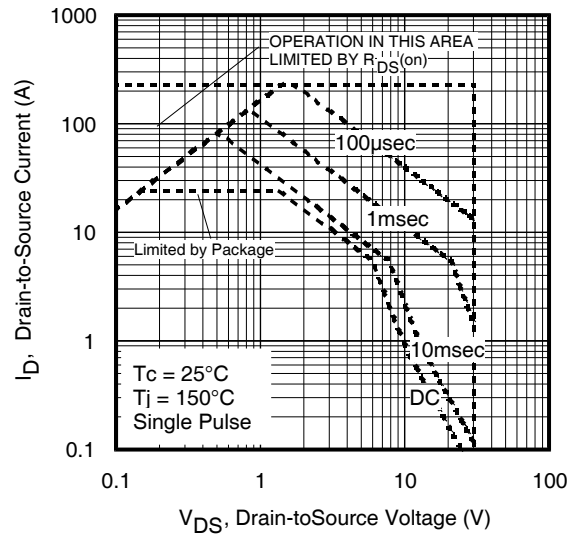
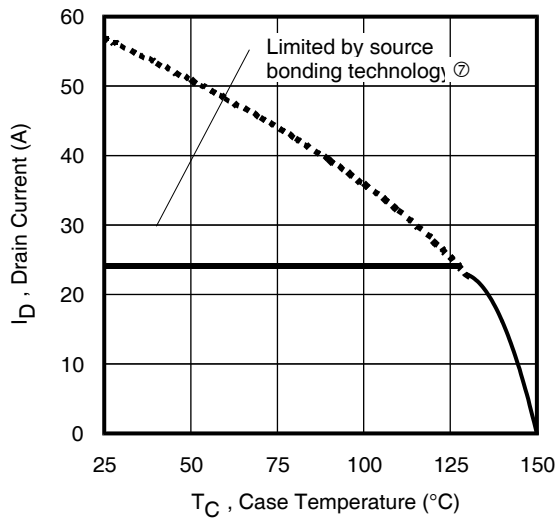
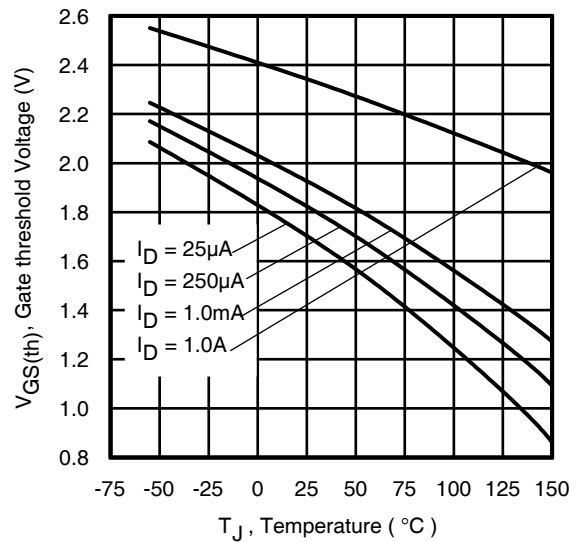
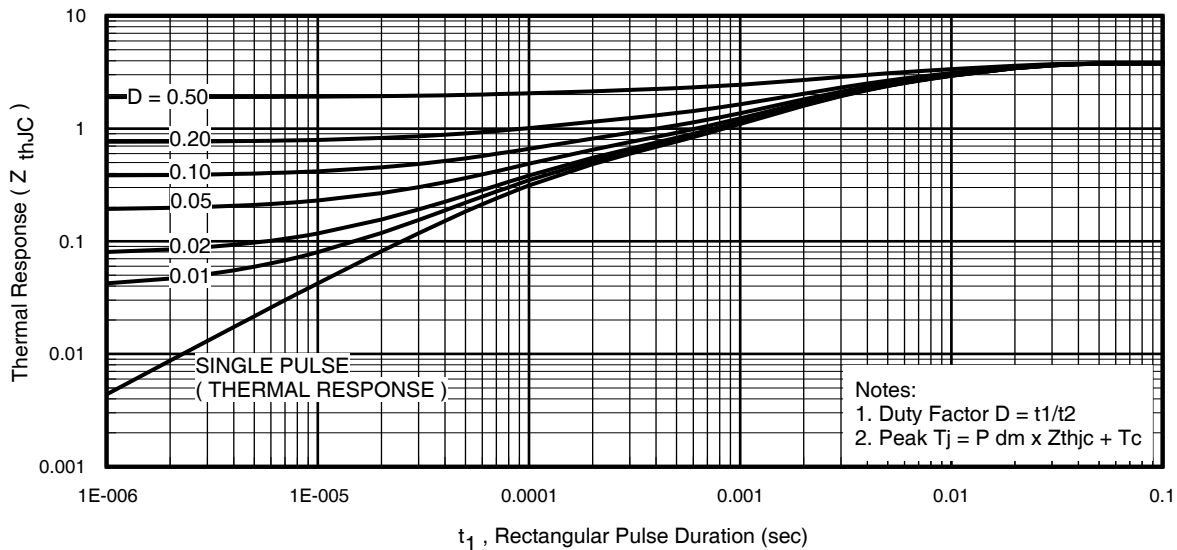
Diode Characteristics

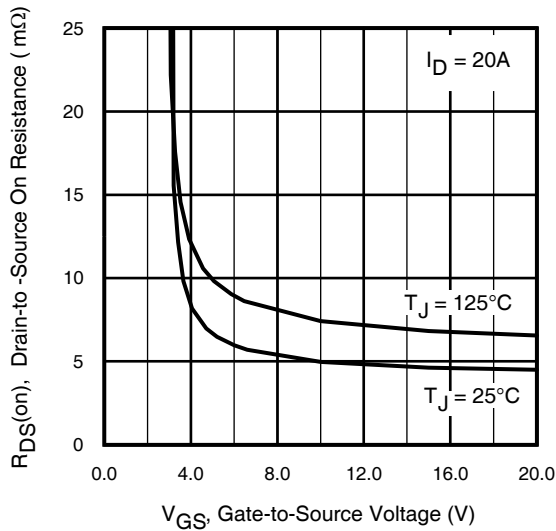
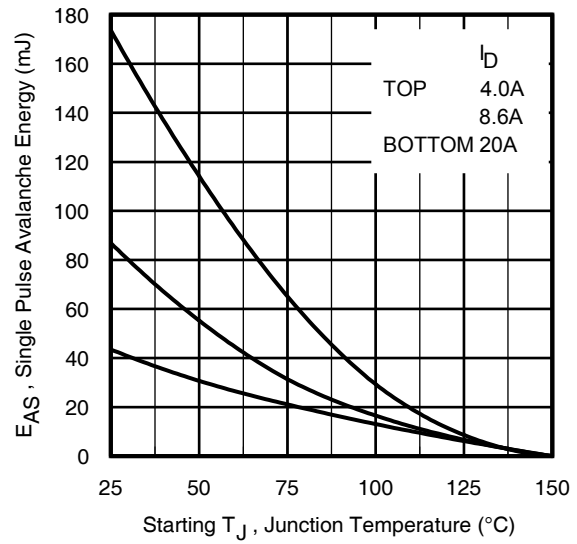
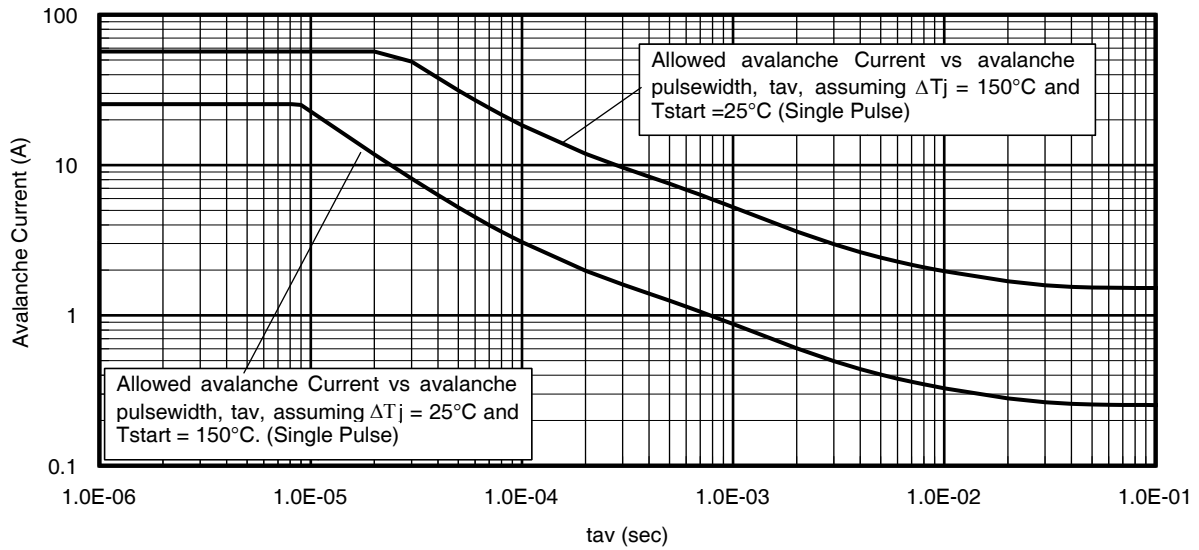
	Parameter	Min.	Typ.	Max.	Units	Conditions
I _S	Continuous Source Current (Body Diode)	—	—	24 ^⑦	A	MOSFET symbol showing the integral reverse p-n junction diode. 
I _{SM}	Pulsed Source Current (Body Diode) ①	—	—	230		
V _{SD}	Diode Forward Voltage	—	—	1.0	V	T _J = 25°C, I _S = 20A, V _{GS} = 0V ③
t _{rr}	Reverse Recovery Time	—	13	20	ns	T _J = 25°C, I _F = 20A, V _{DD} = 15V
Q _{rr}	Reverse Recovery Charge	—	8.1	12	nC	di/dt = 290A/μs ③

Thermal Resistance

	Parameter	Typ.	Max.	Units
R _{θJC} (Bottom)	Junction-to-Case ④	—	3.8	°C/W
R _{θJC} (Top)	Junction-to-Case ④	—	42	
R _{θJA}	Junction-to-Ambient ⑤	—	47	
R _{θJA} (<10s)	Junction-to-Ambient ⑤	—	32	


Fig 1. Typical Output Characteristics

Fig 2. Typical Output Characteristics

Fig 3. Typical Transfer Characteristics

Fig 4. Normalized On-Resistance vs. Temperature

Fig 5. Typical Capacitance vs. Drain-to-Source Voltage

Fig 6. Typical Gate Charge vs. Gate-to-Source Voltage


Fig 7. Typical Source-Drain Diode Forward Voltage

Fig 8. Maximum Safe Operating Area

Fig 9. Maximum Drain Current vs. Case Temperature

Fig 10. Drain-to-Source Breakdown Voltage

Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case


Fig 12. On-Resistance vs. Gate Voltage

Fig 13. Maximum Avalanche Energy vs. Drain Current

Fig 14. Typical Avalanche Current vs. Pulsewidth

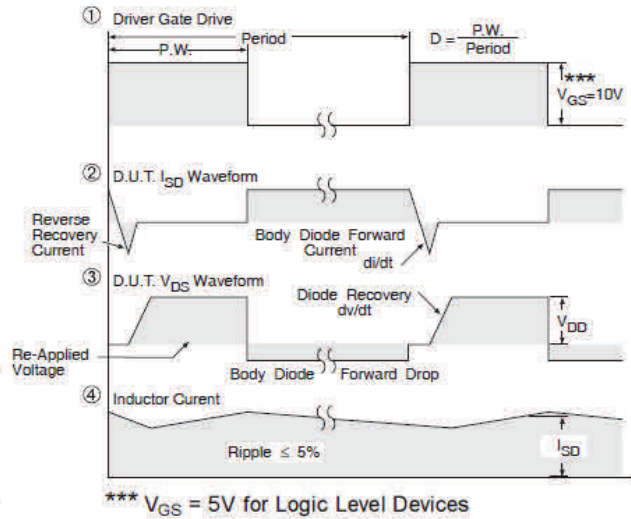
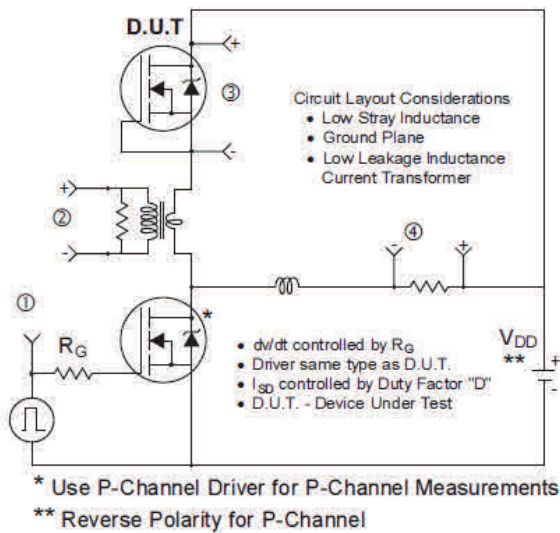


Fig 15. Peak Diode Recovery dv/dt Test Circuit for N-Channel HEXFET® Power MOSFETs

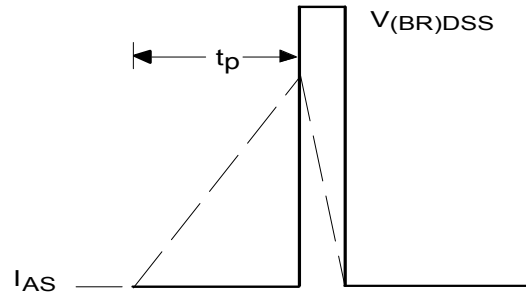
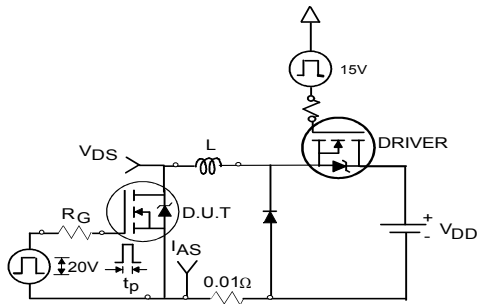


Fig 16a. Unclamped Inductive Test Circuit

Fig 16b. Unclamped Inductive Waveforms

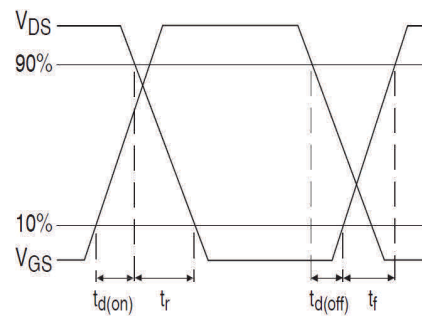
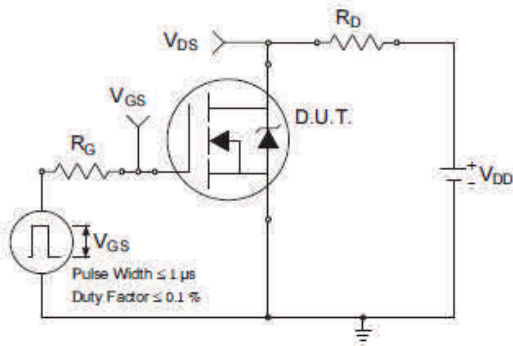


Fig 17a. Switching Time Test Circuit

Fig 17b. Switching Time Waveforms

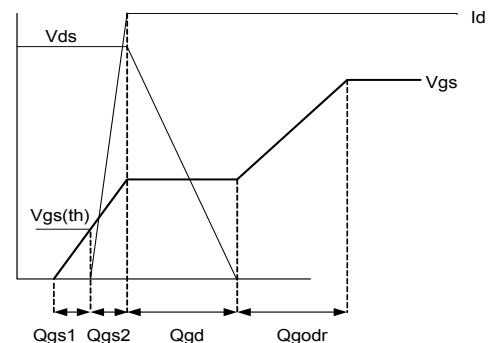
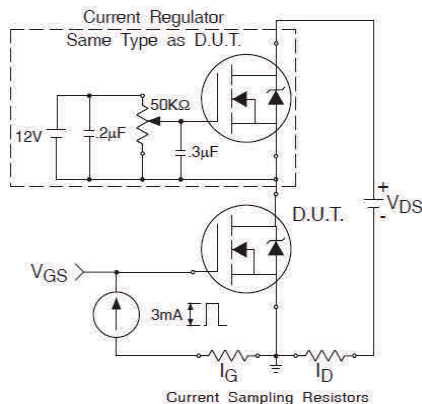
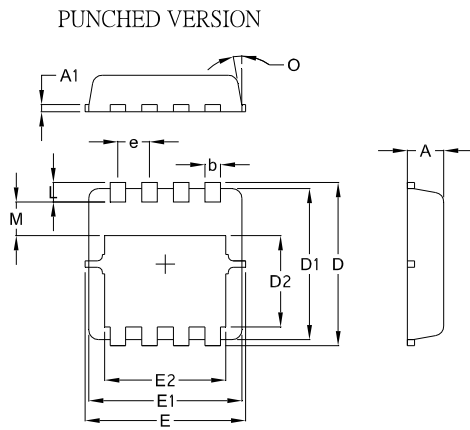


Fig 18a. Gate Charge Test Circuit

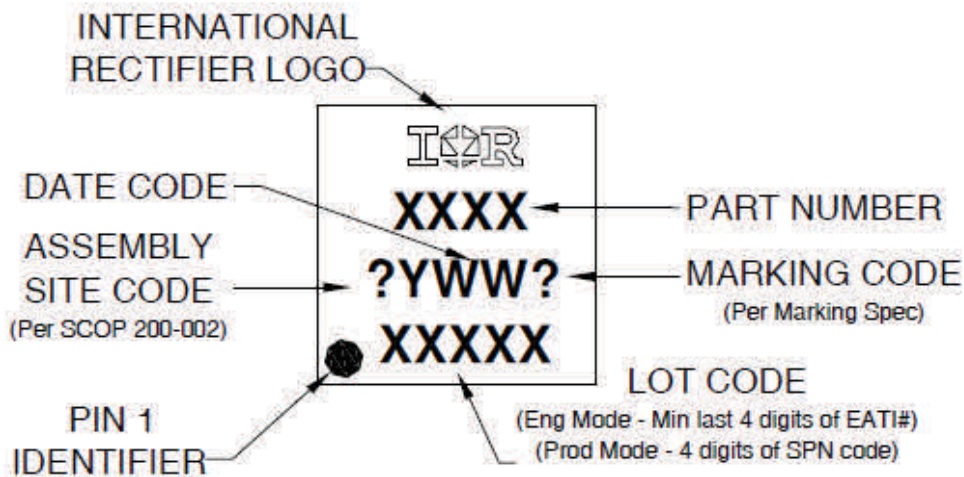
Fig 18b. Gate Charge Waveform

PQFN 3.3mm x 3.3mm Outline Package Details


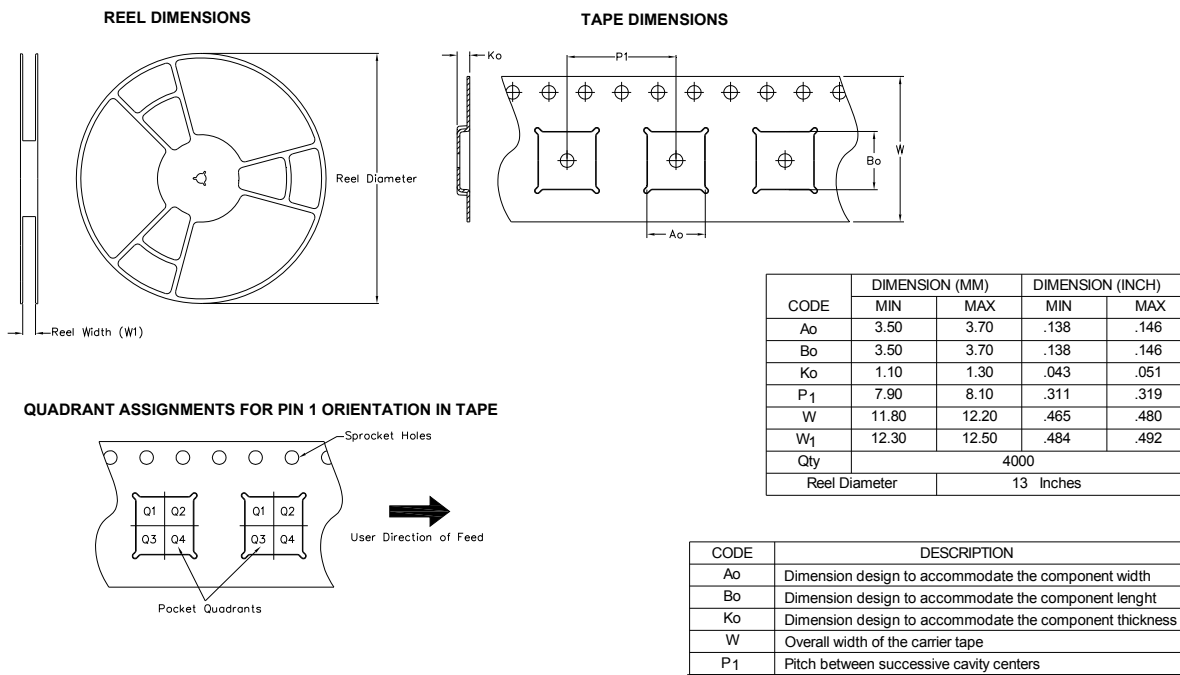
SYMBOL	COMMON			
	MM		INCH	
	MIN.	MAX.	MIN.	MAX.
A	0.70	1.05	0.0276	0.0413
A1	0.12	0.39	0.0047	0.0154
b	0.25	0.39	0.0098	0.0154
D	3.20	3.45	0.1260	0.1358
D1	3.00	3.20	0.1181	0.1417
D2	1.69	2.20	0.0665	0.0866
E	3.20	3.40	0.1260	0.1339
E1	3.00	3.20	0.1181	0.1417
E2	2.15	2.59	0.0846	0.1020
e	0.65 BSC		0.0256 BSC	
L	0.15	0.55	0.0059	0.0217
M	0.59	—	0.0232	—
O	9Deg	12Deg	9Deg	12Deg

For more information on board mounting, including footprint and stencil recommendation, please refer to application note AN-1136: <http://www.irf.com/technical-info/appnotes/an-1136.pdf>

For more information on package inspection techniques, please refer to application note AN-1154: <http://www.irf.com/technical-info/appnotes/an-1154.pdf>

PQFN 3.3mm x 3.3mm Outline Part Marking


Note: For the most current drawing please refer to IR website at <http://www.irf.com/package/>

PQFN 3.3mm x 3.3mm Outline Tape and Reel


Note: For the most current drawing please refer to IR website at <http://www.irf.com/package/>

Qualification Information[†]

Qualification Level	Consumer ^{††} (per JEDEC JESD47F ^{†††} guidelines)	
Moisture Sensitivity Level	PQFN 3.3mm x 3.3mm	MSL1 (per JEDEC J-STD-020D ^{†††})
RoHS Compliant	Yes	

† Qualification standards can be found at International Rectifier’s web site: <http://www.irf.com/product-info/reliability>

†† Higher qualification ratings may be available should the user have such requirements. Please contact your International Rectifier sales representative for further information: <http://www.irf.com/whoto-call/salesrep/>

††† Applicable version of JEDEC standard at the time of product release.

Notes:

- ① Repetitive rating; pulse width limited by max. junction temperature.
- ② Starting $T_J = 25^\circ\text{C}$, $L = 0.22\text{mH}$, $R_G = 50\Omega$, $I_{AS} = 20\text{A}$.
- ③ Pulse width $\leq 400\mu\text{s}$; duty cycle $\leq 2\%$.
- ④ R_θ is measured at T_J of approximately 90°C .
- ⑤ When mounted on 1 inch square 2 oz copper pad on 1.5x1.5 in. board of FR-4 material. Please refer to AN-994 for more details: <http://www.irf.com/technical-info/appnotes/an-994.pdf>
- ⑥ Calculated continuous current based on maximum allowable junction temperature.
- ⑦ Current is limited to 25A by source bonding technology.

Revision History

Date	Comments
6/5/14	<ul style="list-style-type: none"> • Updated schematic on page 1 • Updated package outline and part marking on page 7 • Updated tape and reel on page 8
6/30/14	<ul style="list-style-type: none"> • Remove “SAWN” package outline on page 7.