IXYS

Preliminary Technical Information

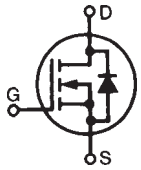
X2-Class Power MOSFET

IXTR102N65X2

V_{DSS} = 650V
I_{D25} = 54A
$R_{DS(on)}$ ≤ 33mΩ

(Electrically Isolated Tab)

N-Channel Enhancement Mode
Avalanche Rated



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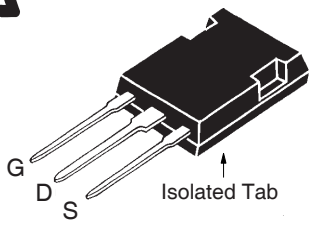


G = Gate D = Drain
S = Source

Symbol	Test Conditions	Maximum Ratings	
V_{DSS}	T_J = 25°C to 150°C	650	V
V_{DGR}	T_J = 25°C to 150°C, R_{GS} = 1MΩ	650	V
V_{GSS}	Continuous	± 30	V
V_{GSM}	Transient	± 40	V
I_{D25}	T_C = 25°C	54	A
I_{DM}	T_C = 25°C, Pulse Width Limited by T_{JM}	204	A
I_A	T_C = 25°C	25	A
E_{AS}	T_C = 25°C	3	J
P_D	T_C = 25°C	330	W
dv/dt	$I_S \le I_{DM}$, $V_{DD} \le V_{DSS}$, $T_J \le 150°C$	15	V/ns
T_J		-55 ... +150	°C
T_{JM}		150	°C
T_{stg}		-55 ... +150	°C
T_L	Maximum Lead Temperature for Soldering	300	°C
T_{SOLD}	1.6 mm (0.062in.) from Case for 10s	260	°C
V_{ISOL}	50/60 Hz, 1 Minute	2500	V~
F_C	Mounting Force	20..120/4.5..27	N/lb
Weight		5	g

Symbol	Test Conditions (T_J = 25°C Unless Otherwise Specified)	Characteristic Values Min.	Typ.	Max.	
BV_{DSS}	V_{GS} = 0V, I_D = 1mA	650			V
$V_{GS(th)}$	$V_{DS} = V_{GS}$, I_D = 250μA	3.0		5.0	V
I_{GSS}	V_{GS} = ± 30V, V_{DS} = 0V			± 100	nA
I_{DSS}	$V_{DS} = V_{DSS}$, V_{GS}= 0V			25	μA
	T_J = 125°C			500	μA
$R_{DS(on)}$	V_{GS} = 10V, I_D = 51A, Note 1			33	mΩ

Features

- Silicon Chip on Direct-Copper Bond (DCB) Substrate
- Isolated Mounting Surface
- 2500V~ Electrical Isolation
- Low Q_G
- Avalanche Rated
- Low Package Inductance

Advantages

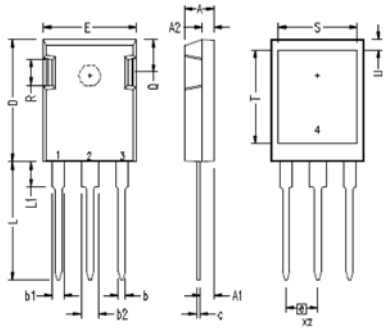
- High Power Density
- Easy to Mount
- Space Savings

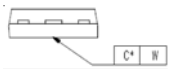
Applications

- Switch-Mode and Resonant-Mode Power Supplies
- DC-DC Converters
- PFC Circuits
- AC and DC Motor Drives
- Robotics and Servo Controls

Symbol	Test Conditions (T_J = 25°C, Unless Otherwise Specified)	Characteristic Values Min.	Typ.	Max
g_{fs}	V_{DS} = 10V, I_D = 51A, Note 1	50	82	S
R_{Gi}	Gate Input Resistance		0.7	Ω
C_{iss}	V_{GS} = 0V, V_{DS} = 25V, f = 1MHz		10.9	nF
C_{oss}			6100	pF
C_{rss}			12.6	pF
	Effective Output Capacitance			
$C_{o(er)}$	Energy related; V_{GS} = 0V		367	pF
$C_{o(tr)}$	Time related; V_{DS} = 0.8 • V_{DSS}		1420	pF
$t_{d(on)}$	**Resistive Switching Times**		37	ns
t_r	V_{GS} = 10V, V_{DS} = 0.5 • V_{DSS}, I_D = 51A		28	ns
$t_{d(off)}$	R_G = 2Ω (External)		67	ns
t_f			11	ns
$Q_{g(on)}$	V_{GS} = 10V, V_{DS} = 0.5 • V_{DSS}, I_D = 51A		152	nC
Q_{gs}			57	nC
Q_{gd}			33	nC
R_{thJC}				0.38 °C/W
R_{thCS}			0.15	°C/W

ISOPLUS247 (IXTR) Outline





1 = Gate
2,4 = Drain
3 = Source

SYM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	.190	.205	4.83	5.21
A1	.090	.100	2.29	2.54
A2	.075	.085	1.91	2.16
b	.045	.055	1.14	1.40
b1	.075	.085	1.91	2.15
b2	.115	.126	2.92	3.20
C	.024	.033	0.61	0.83
D	.819	.840	20.80	21.34
E	.620	.635	15.75	16.13
e	.215 BSC		5.45 BSC	
L	.780	.811	19.81	20.60
L1	.150	.172	3.81	4.38
Q	.220	.244	5.59	6.20
R	.170	.191	4.32	4.85
S	.520	.540	13.21	13.72
T	.620	.640	15.75	16.26
U	.065	.080	1.65	2.03
W	0	.004	0	0.10

Source-Drain Diode

Symbol	Test Conditions (T_J = 25°C, Unless Otherwise Specified)	Characteristic Values Min.	Typ.	Max.	
I_S	V_{GS} = 0V			102	A
I_{SM}	Repetitive, Pulse Width Limited by T_{JM}			408	A
V_{SD}	I_F = I_S, V_{GS} = 0V, Note 1			1.4	V
t_{rr}	I_F = 51A, -di/dt = 100A/μs		450		ns
Q_{RM}	V_R = 100V, V_{GS} = 0V		11.7		μC
I_{RM}			52		A

Note 1. Pulse test, t ≤ 300μs, duty cycle, d ≤ 2%.

PRELIMINARY TECHNICAL INFORMATION

The product presented herein is under development. The Technical Specifications offered are derived from a subjective evaluation of the design, based upon prior knowledge and experience, and constitute a "considered reflection" of the anticipated result. IXYS reserves the right to change limits, test conditions, and dimensions without notice.

Fig. 1. Output Characteristics @ T_J = 25°C

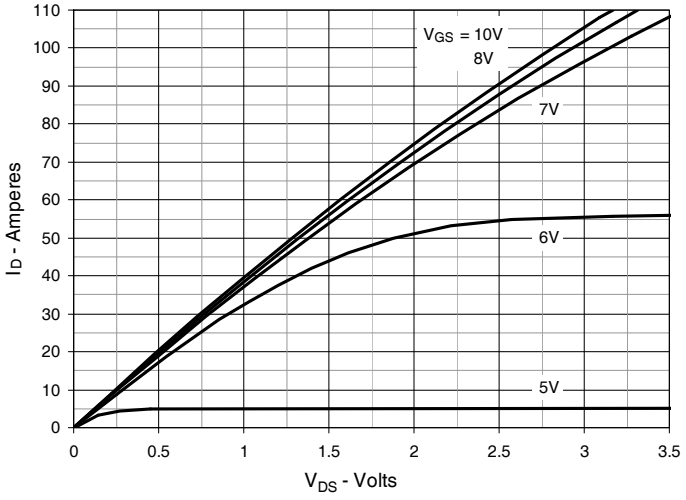


Fig. 2. Extended Output Characteristics @ T_J = 25°C

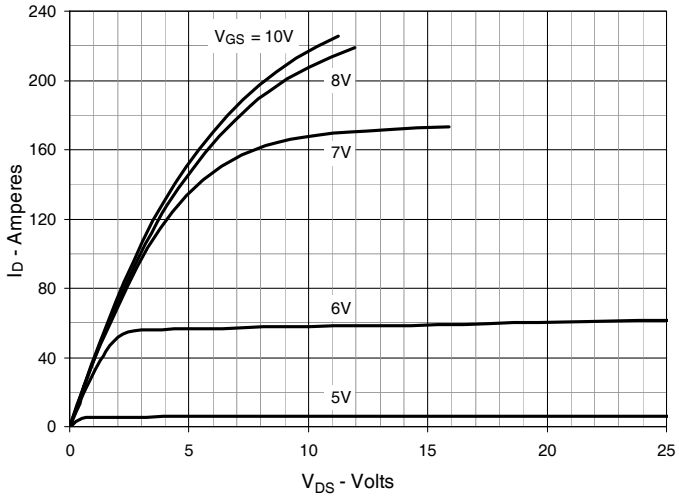


Fig. 3. Output Characteristics @ T_J = 125°C

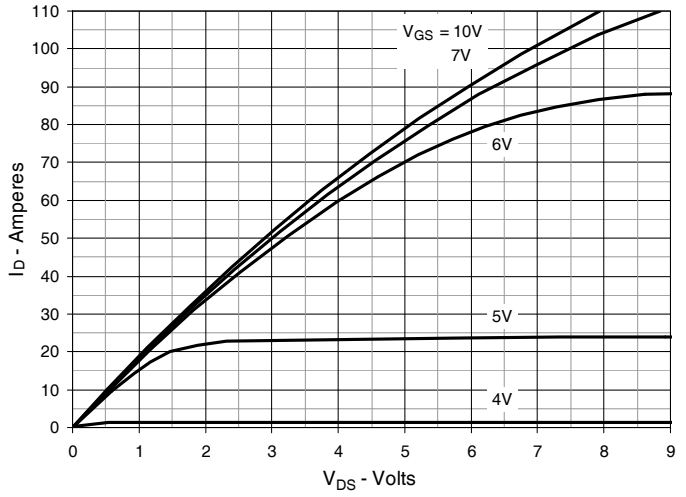


Fig. 4. $R_{DS(on)}$ Normalized to I_D = 51A Value vs. Junction Temperature

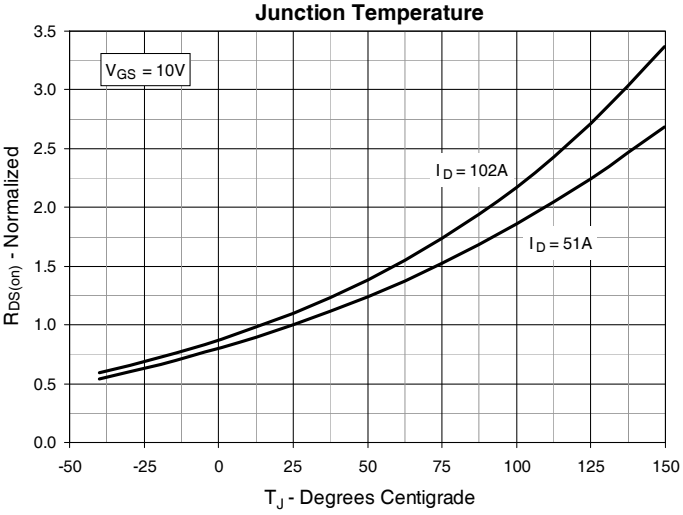


Fig. 5. $R_{DS(on)}$ Normalized to I_D = 51A Value vs. Drain Current

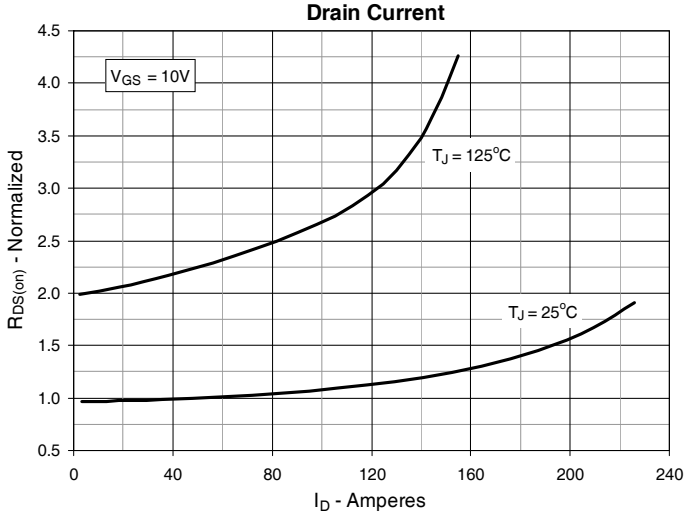


Fig. 6. Normalized Breakdown & Threshold Voltages vs. Junction Temperature

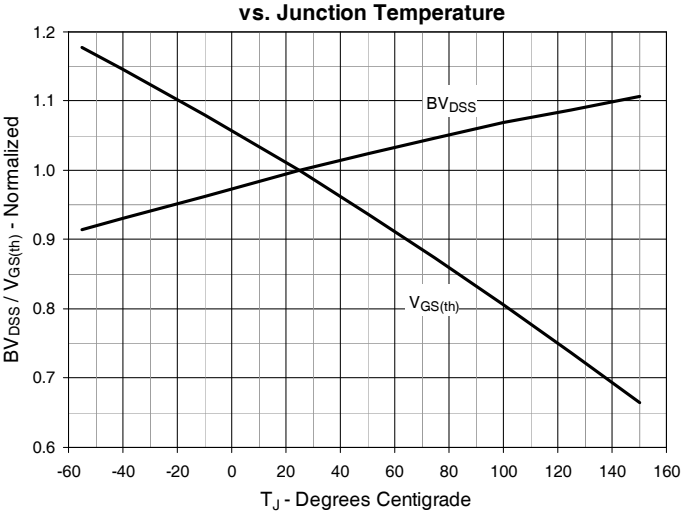


Fig. 7. Maximum Drain Current vs. Case Temperature

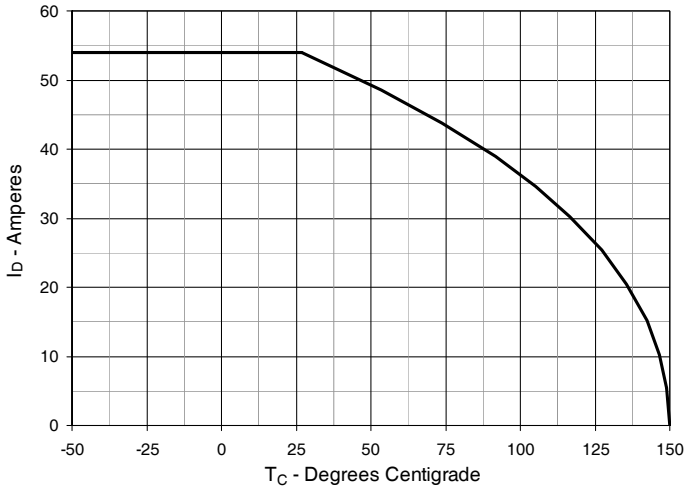


Fig. 8. Input Admittance

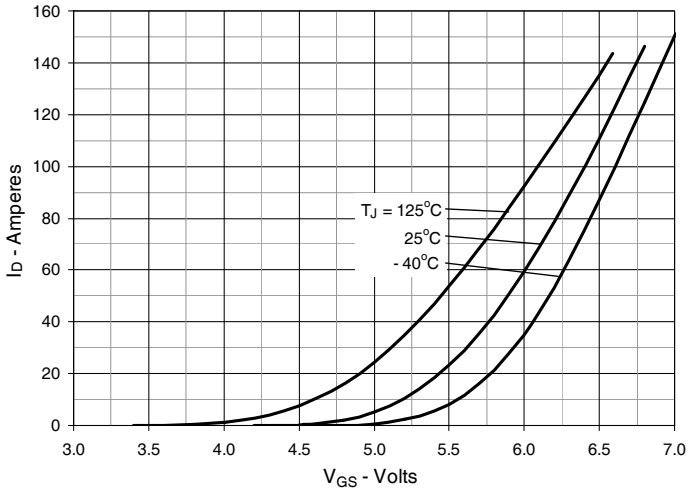


Fig. 9. Transconductance

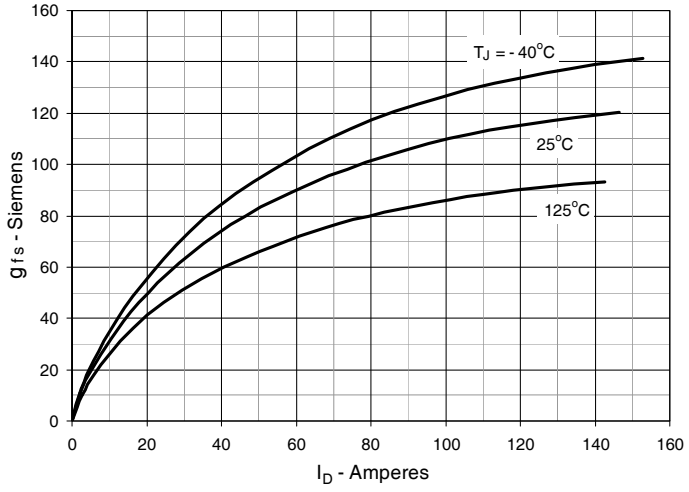


Fig. 10. Forward Voltage Drop of Intrinsic Diode

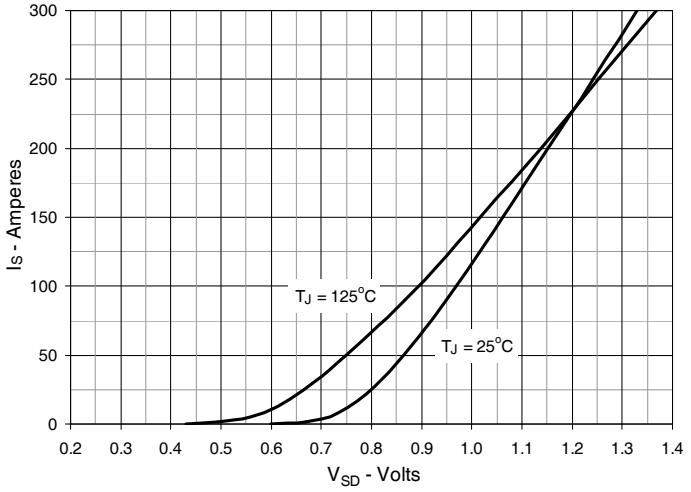


Fig. 11. Gate Charge

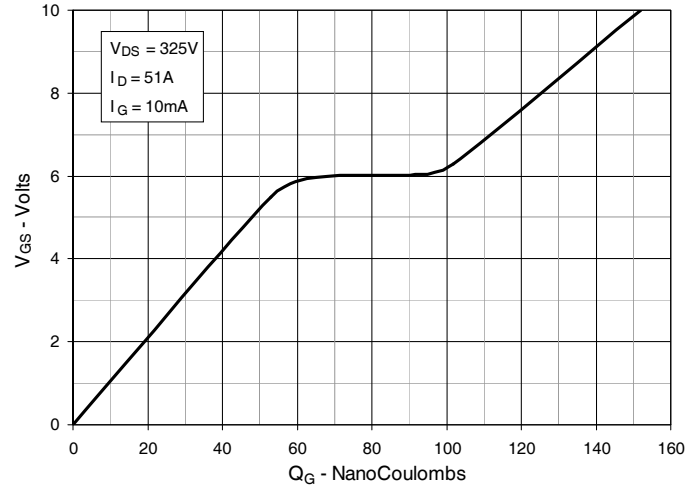


Fig. 12. Capacitance

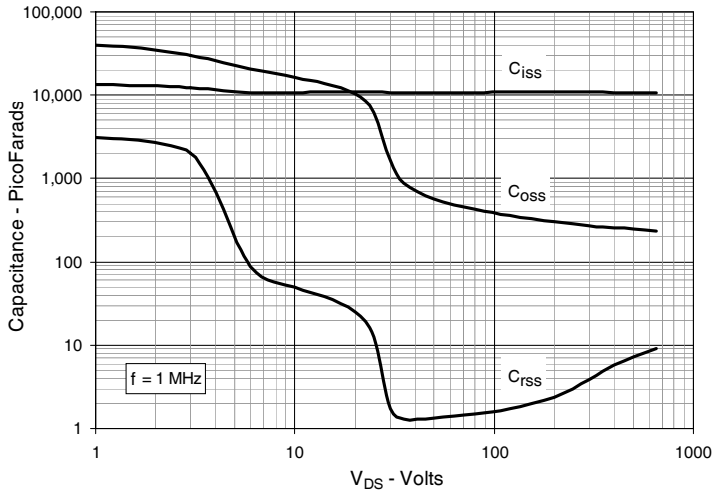


Fig. 13. Output Capacitance Stored Energy

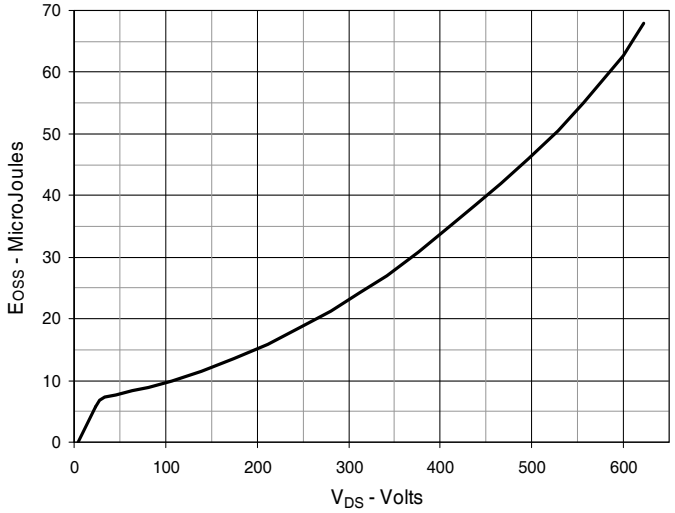


Fig. 14. Forward-Bias Safe Operating Area

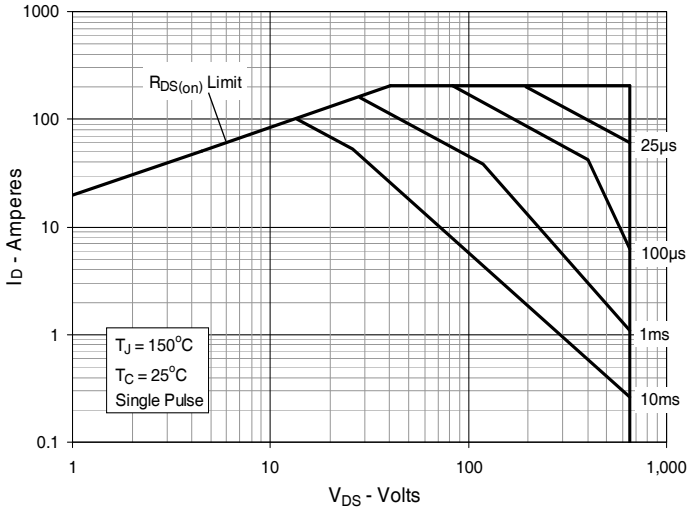


Fig. 15. Maximum Transient Thermal Impedance