

# MOSFET

Metal Oxide Semiconductor Field Effect Transistor

## CoolMOS™ C7

650V CoolMOS™ C7 Power Transistor  
IPL65R195C7

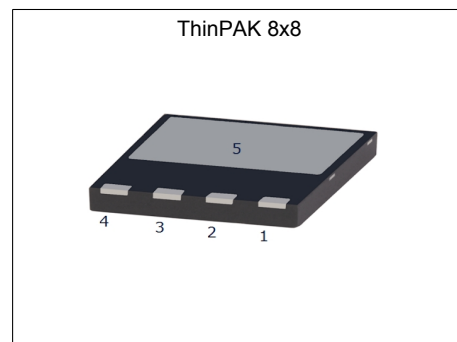
## Data Sheet

Rev. 2.0  
Final

## 1 Description

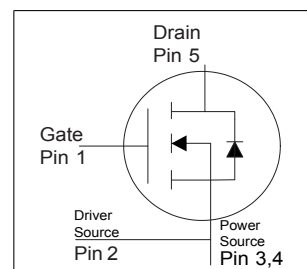
CoolMOS™ is a revolutionary technology for high voltage power MOSFETs, designed according to the superjunction (SJ) principle and pioneered by Infineon Technologies.

CoolMOS™ C7 series combines the experience of the leading SJ MOSFET supplier with high class innovation. The product portfolio provides all benefits of fast switching superjunction MOSFETs offering better efficiency, reduced gate charge, easy implementation and outstanding reliability.



## Features

- Increased MOSFET dv/dt ruggedness
- Better efficiency due to best in class FOM  $R_{DS(on)} \cdot E_{oss}$  and  $R_{DS(on)} \cdot Q_g$
- **ThinPAK** SMD Package with very low parasitic inductance to enable fast and reliable switching with minimum of size to increase power-density
- Easy to use/drive due to **driver source pin** for better control of the gate.
- Pb-free plating, halogen free mold compound
- Qualified for industrial grade applications according to JEDEC (J-STD20 and JESD22)



## Benefits

- Enabling higher system efficiency by lower switching losses
- Enabling higher frequency / increased power density solutions
- System cost / size savings due to reduced cooling requirements
- Higher system reliability due to lower operating temperatures



## Applications

PFC stages and hard switching PWM stages for e.g. Computing, Server, Telecom, UPS and Solar.

*Please note: For MOSFET paralleling the use of ferrite beads on the gate or separate totem poles is generally recommended.*

**Table 1 Key Performance Parameters**

Parameter	Value	Unit
$V_{DS} @ T_{j,max}$	700	V
$R_{DS(on),max}$	195	mΩ
$Q_{g,typ}$	23	nC
$I_{D,pulse}$	49	A
$E_{oss}@400V$	2.7	μJ
Body diode di/dt	55	A/μs

Type / Ordering Code	Package	Marking	Related Links
IPL65R195C7	PG-VSON-4	65C7195	see Appendix A

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## 2 Maximum ratings

at  $T_j = 25^\circ\text{C}$ , unless otherwise specified

**Table 2 Maximum ratings**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Continuous drain current <sup>1)</sup>	$I_D$	-	-	12 8	A	$T_C=25^\circ\text{C}$ $T_C=100^\circ\text{C}$
Pulsed drain current <sup>2)</sup>	$I_{D,pulse}$	-	-	49	A	$T_C=25^\circ\text{C}$
Avalanche energy, single pulse	$E_{AS}$	-	-	57	mJ	$I_D=5.4\text{A}$ ; $V_{DD}=50\text{V}$ ; see table 10
Avalanche energy, repetitive	$E_{AR}$	-	-	0.29	mJ	$I_D=5.4\text{A}$ ; $V_{DD}=50\text{V}$ ; see table 10
Avalanche current, single pulse	$I_{AS}$	-	-	5.4	A	-
MOSFET dv/dt ruggedness	dv/dt	-	-	100	V/ns	$V_{DS}=0\dots400\text{V}$
Gate source voltage (static)	$V_{GS}$	-20	-	20	V	static;
Gate source voltage (dynamic)	$V_{GS}$	-30	-	30	V	AC ( $f>1\text{ Hz}$ )
Power dissipation	$P_{tot}$	-	-	75	W	$T_C=25^\circ\text{C}$
Storage temperature	$T_{stg}$	-40	-	150	$^\circ\text{C}$	-
Operating junction temperature	$T_j$	-40	-	150	$^\circ\text{C}$	-
Mounting torque	-	-	-	n.a.	Ncm	-
Continuous diode forward current	$I_S$	-	-	12	A	$T_C=25^\circ\text{C}$
Diode pulse current <sup>2)</sup>	$I_{S,pulse}$	-	-	49	A	$T_C=25^\circ\text{C}$
Reverse diode dv/dt <sup>3)</sup>	dv/dt	-	-	1	V/ns	$V_{DS}=0\dots400\text{V}$ , $I_{SD}\leq I_S$ , $T_j=25^\circ\text{C}$ see table 8
Maximum diode commutation speed	di/dt	-	-	55	A/ $\mu\text{s}$	$V_{DS}=0\dots400\text{V}$ , $I_{SD}\leq I_S$ , $T_j=25^\circ\text{C}$ see table 8
Insulation withstand voltage	$V_{ISO}$	-	-	n.a.	V	$V_{rms}$ , $T_C=25^\circ\text{C}$ , $t=1\text{min}$

<sup>1)</sup> Limited by  $T_{j,max}$ .

<sup>2)</sup> Pulse width  $t_p$  limited by  $T_{j,max}$

<sup>3)</sup> Identical low side and high side switch with identical  $R_G$

### 3 Thermal characteristics

**Table 3 Thermal characteristics**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Thermal resistance, junction - case	$R_{thJC}$	-	-	1.66	°C/W	-
Thermal resistance, junction - ambient	$R_{thJA}$	-	-	62	°C/W	device on PCB, minimal footprint
Thermal resistance, junction - ambient for SMD version	$R_{thJA}$	-	35	45	°C/W	Device on 40mm*40mm*1.5mm epoxy PCB FR4 with 6cm <sup>2</sup> (one layer, 70µm thickness) copper area for drain connection and cooling. PCB is vertical without air stream cooling.
Reflow soldering temperature	$T_{sold}$	-	-	260	°C	reflow MSL3

## 4 Electrical characteristics

at  $T_j=25^\circ\text{C}$ , unless otherwise specified

**Table 4 Static characteristics**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Drain-source breakdown voltage	$V_{(BR)DSS}$	650	-	-	V	$V_{GS}=0\text{V}$ , $I_D=1\text{mA}$
Gate threshold voltage	$V_{(GS)th}$	3	3.5	4	V	$V_{DS}=V_{GS}$ , $I_D=0.29\text{mA}$
Zero gate voltage drain current	$I_{DSS}$	-	-	1	$\mu\text{A}$	$V_{DS}=650$ , $V_{GS}=0\text{V}$ , $T_j=25^\circ\text{C}$ $V_{DS}=650$ , $V_{GS}=0\text{V}$ , $T_j=150^\circ\text{C}$
Gate-source leakage current	$I_{GSS}$	-	-	100	nA	$V_{GS}=20\text{V}$ , $V_{DS}=0\text{V}$
Drain-source on-state resistance	$R_{DS(on)}$	-	0.173 0.414	0.195 -	$\Omega$	$V_{GS}=10\text{V}$ , $I_D=2.9\text{A}$ , $T_j=25^\circ\text{C}$ $V_{GS}=10\text{V}$ , $I_D=2.9\text{A}$ , $T_j=150^\circ\text{C}$
Gate resistance	$R_G$	-	1.1	-	$\Omega$	$f=1\text{MHz}$ , open drain

**Table 5 Dynamic characteristics**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input capacitance	$C_{iss}$	-	1150	-	pF	$V_{GS}=0\text{V}$ , $V_{DS}=400\text{V}$ , $f=250\text{kHz}$
Output capacitance	$C_{oss}$	-	17	-	pF	$V_{GS}=0\text{V}$ , $V_{DS}=400\text{V}$ , $f=250\text{kHz}$
Effective output capacitance, energy related <sup>1)</sup>	$C_{o(er)}$	-	34	-	pF	$V_{GS}=0\text{V}$ , $V_{DS}=0\dots400\text{V}$
Effective output capacitance, time related <sup>2)</sup>	$C_{o(tr)}$	-	374	-	pF	$I_D=\text{constant}$ , $V_{GS}=0\text{V}$ , $V_{DS}=0\dots400\text{V}$
Turn-on delay time	$t_{d(on)}$	-	9	-	ns	$V_{DD}=400\text{V}$ , $V_{GS}=13\text{V}$ , $I_D=2.9\text{A}$ , $R_G=10\Omega$ ; see table 9
Rise time	$t_r$	-	5	-	ns	$V_{DD}=400\text{V}$ , $V_{GS}=13\text{V}$ , $I_D=2.9\text{A}$ , $R_G=10\Omega$ ; see table 9
Turn-off delay time	$t_{d(off)}$	-	75	-	ns	$V_{DD}=400\text{V}$ , $V_{GS}=13\text{V}$ , $I_D=2.9\text{A}$ , $R_G=10\Omega$ ; see table 9
Fall time	$t_f$	-	16	-	ns	$V_{DD}=400\text{V}$ , $V_{GS}=13\text{V}$ , $I_D=2.9\text{A}$ , $R_G=10\Omega$ ; see table 9

**Table 6 Gate charge characteristics**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Gate to source charge	$Q_{gs}$	-	6	-	nC	$V_{DD}=400\text{V}$ , $I_D=2.9\text{A}$ , $V_{GS}=0$ to $10\text{V}$
Gate to drain charge	$Q_{gd}$	-	7	-	nC	$V_{DD}=400\text{V}$ , $I_D=2.9\text{A}$ , $V_{GS}=0$ to $10\text{V}$
Gate charge total	$Q_g$	-	23	-	nC	$V_{DD}=400\text{V}$ , $I_D=2.9\text{A}$ , $V_{GS}=0$ to $10\text{V}$
Gate plateau voltage	$V_{plateau}$	-	5.0	-	V	$V_{DD}=400\text{V}$ , $I_D=2.9\text{A}$ , $V_{GS}=0$ to $10\text{V}$

<sup>1)</sup>  $C_{o(er)}$  is a fixed capacitance that gives the same stored energy as  $C_{oss}$  while  $V_{DS}$  is rising from 0 to 400V

<sup>2)</sup>  $C_{o(tr)}$  is a fixed capacitance that gives the same charging time as  $C_{oss}$  while  $V_{DS}$  is rising from 0 to 400V

**Table 7 Reverse diode characteristics**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Diode forward voltage	$V_{SD}$	-	0.8	-	V	$V_{GS}=0V, I_F=2.9A, T_j=25^{\circ}C$
Reverse recovery time	$t_{rr}$	-	700	-	ns	$V_R=400V, I_F=12A, di_F/dt=55A/\mu s$ ; see table 8
Reverse recovery charge	$Q_{rr}$	-	5.8	-	$\mu C$	$V_R=400V, I_F=12A, di_F/dt=55A/\mu s$ ; see table 8
Peak reverse recovery current	$I_{rrm}$	-	16	-	A	$V_R=400V, I_F=12A, di_F/dt=55A/\mu s$ ; see table 8

### 5 Electrical characteristics diagrams

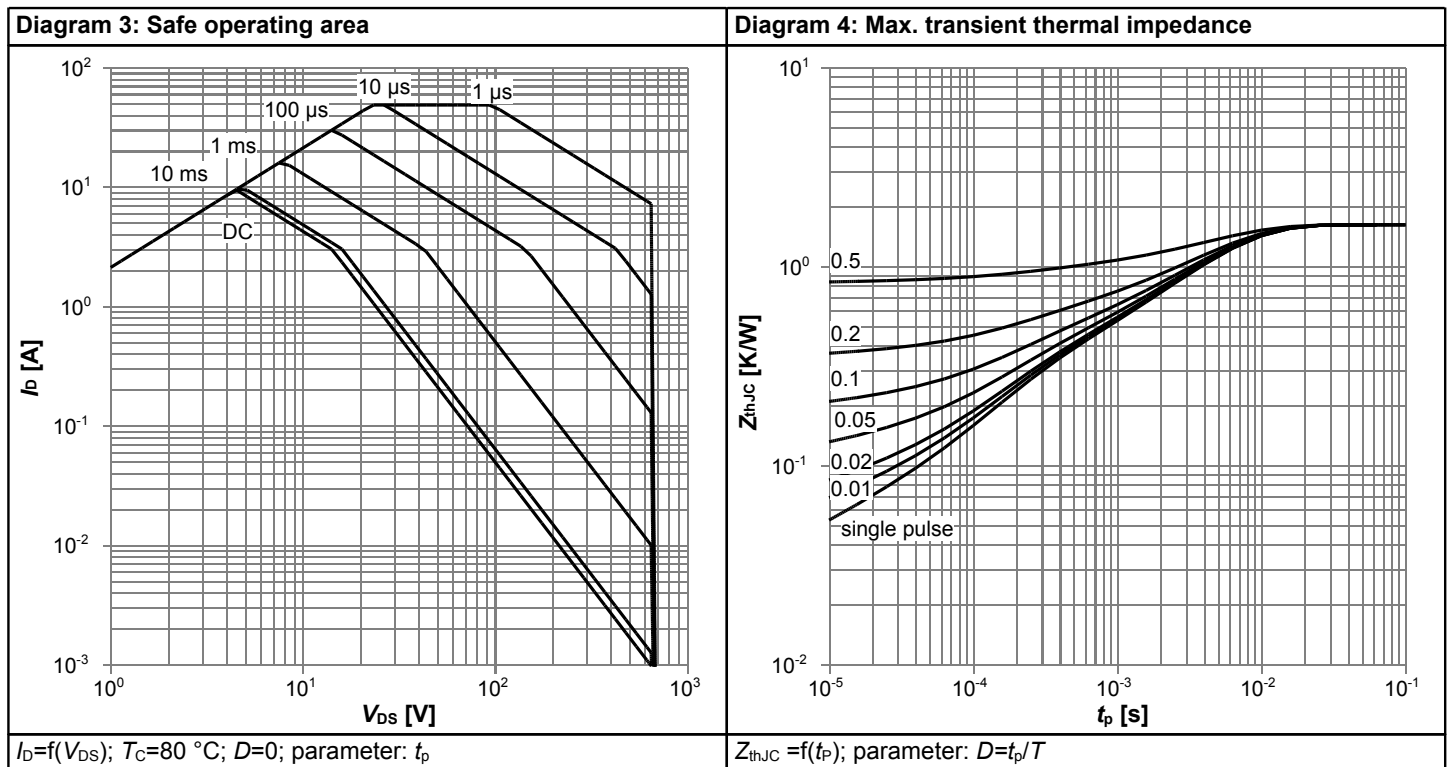
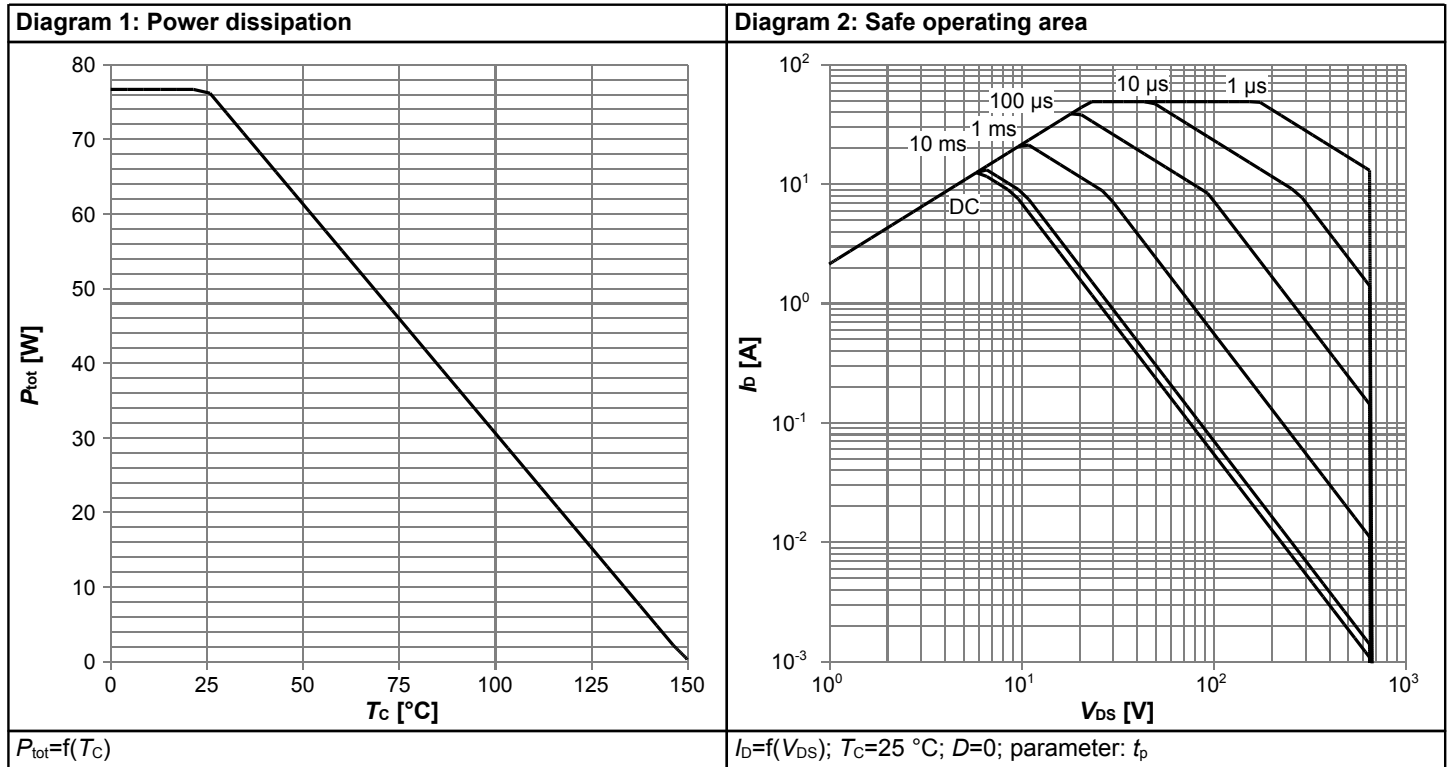
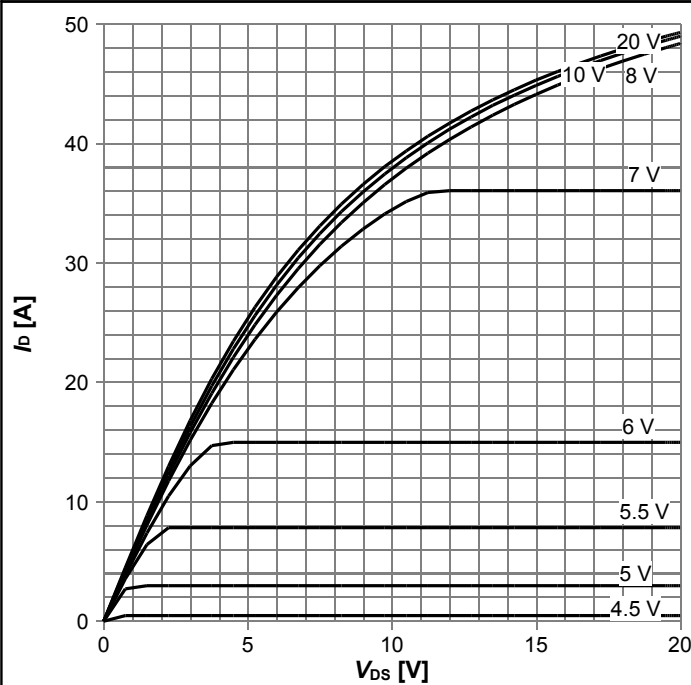


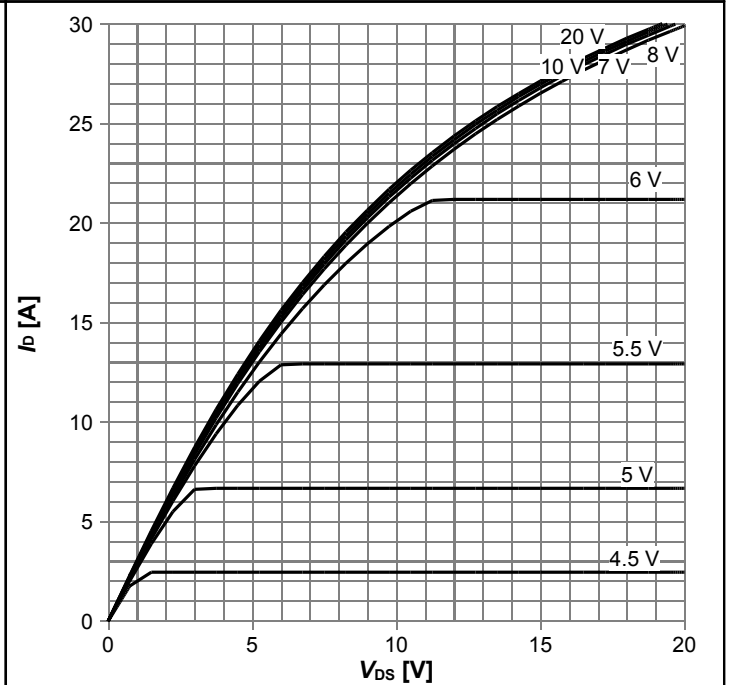


Diagram 5: Typ. output characteristics



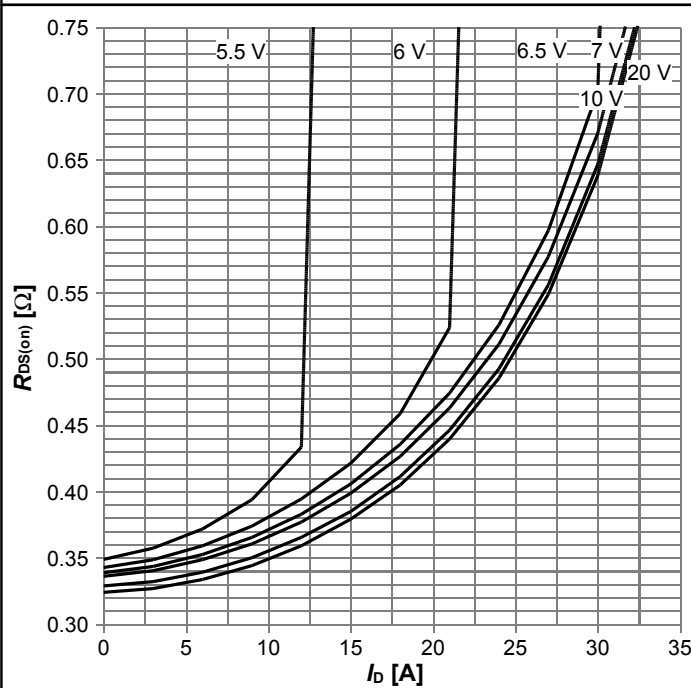
$I_D = f(V_{DS})$ ;  $T_j = 25^\circ\text{C}$ ; parameter:  $V_{GS}$

Diagram 6: Typ. output characteristics



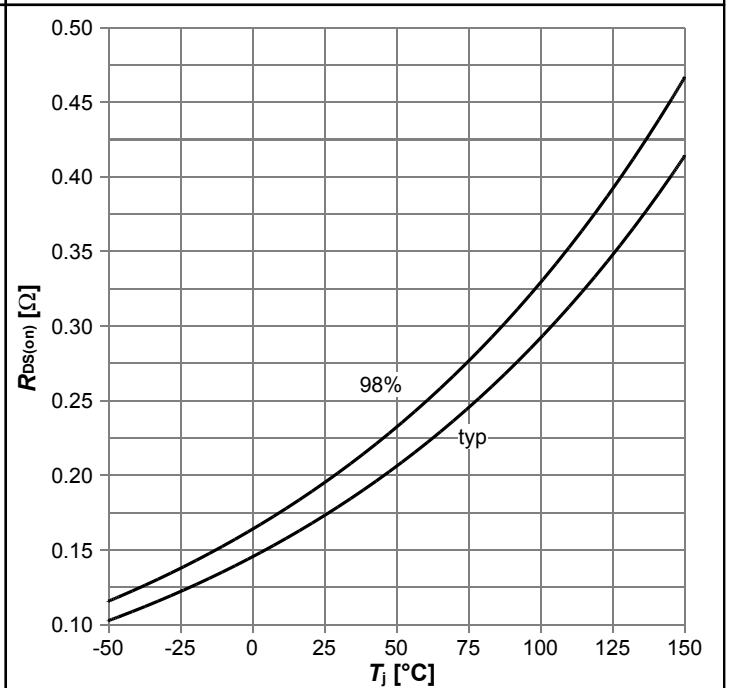
$I_D = f(V_{DS})$ ;  $T_j = 125^\circ\text{C}$ ; parameter:  $V_{GS}$

Diagram 7: Typ. drain-source on-state resistance



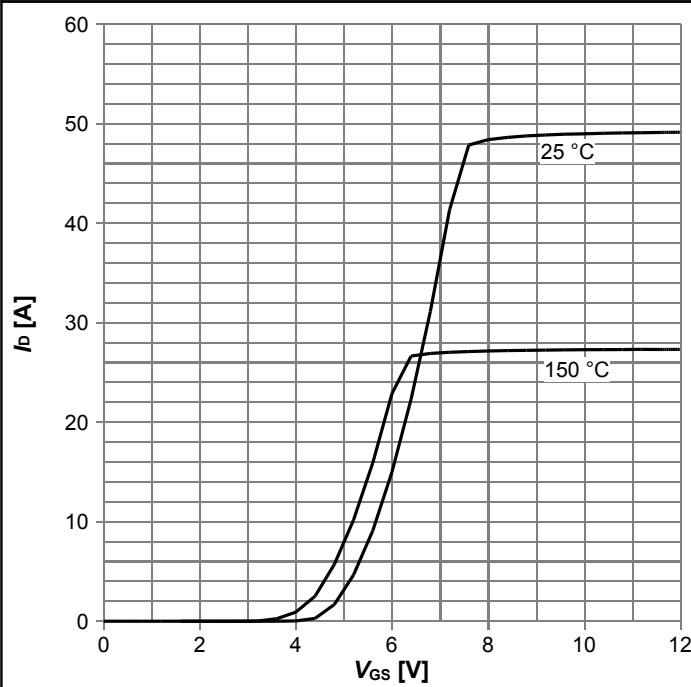
$R_{DS(on)} = f(I_D)$ ;  $T_j = 125^\circ\text{C}$ ; parameter:  $V_{GS}$

Diagram 8: Drain-source on-state resistance



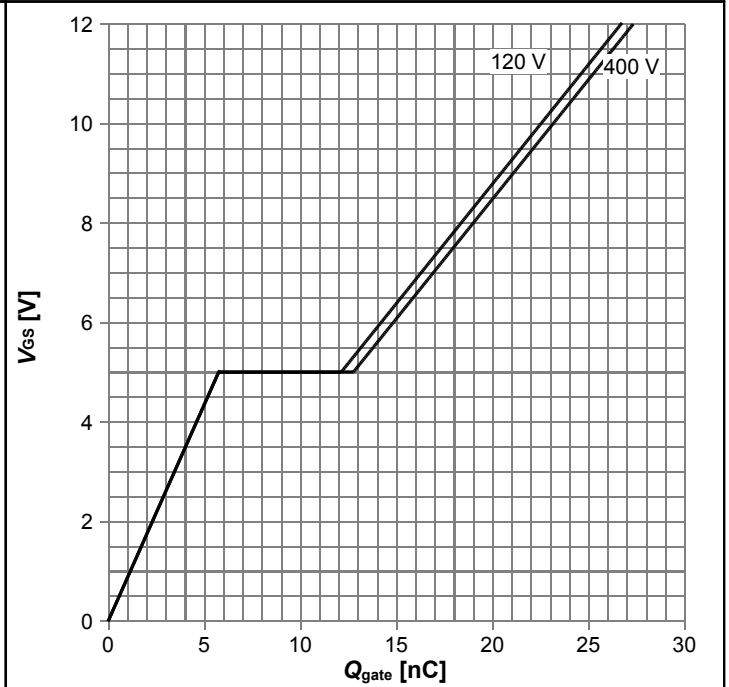
$R_{DS(on)} = f(T_j)$ ;  $I_D = 2.9\text{ A}$ ;  $V_{GS} = 10\text{ V}$

Diagram 9: Typ. transfer characteristics



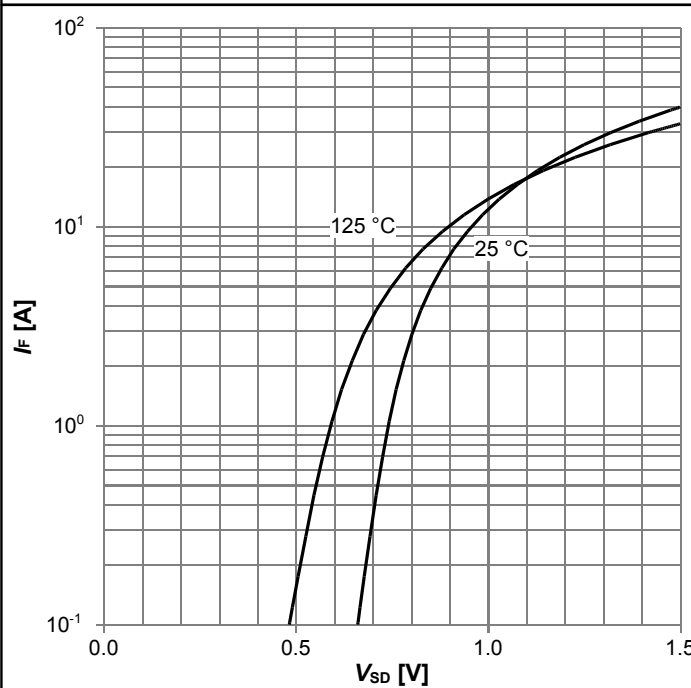
$I_D=f(V_{GS}); V_{DS}=20V; \text{parameter: } T_j$

Diagram 10: Typ. gate charge



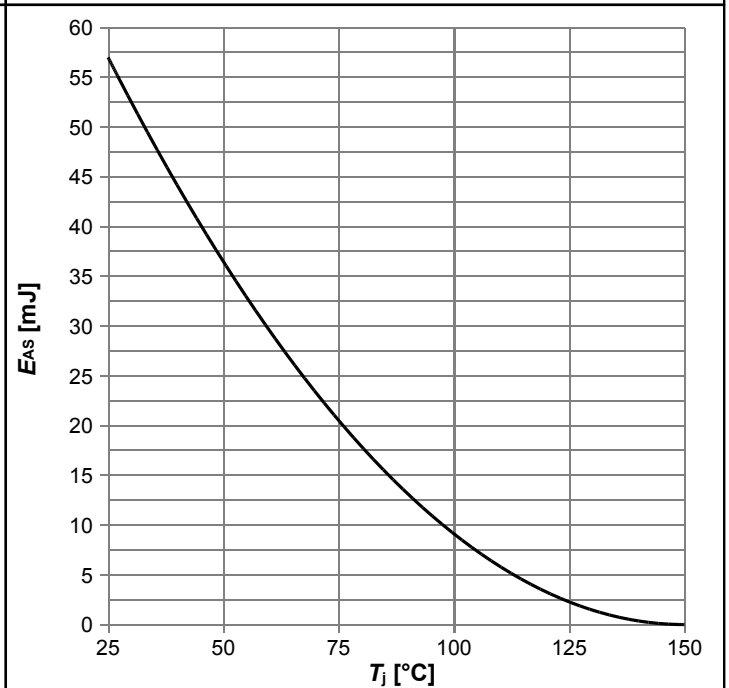
$V_{GS}=f(Q_{gate}); I_D=2.9 \text{ A pulsed}; \text{parameter: } V_{DD}$

Diagram 11: Forward characteristics of reverse diode



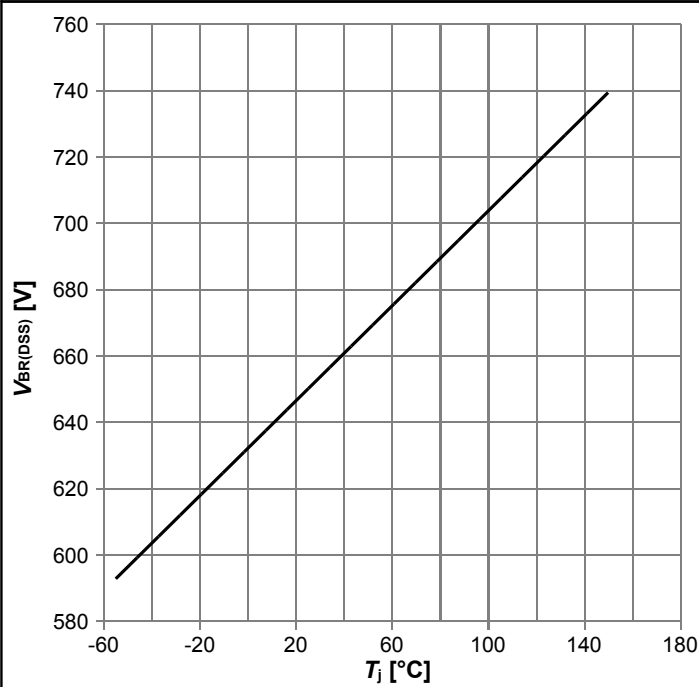
$I_F=f(V_{SD}); \text{parameter: } T_j$

Diagram 12: Avalanche energy



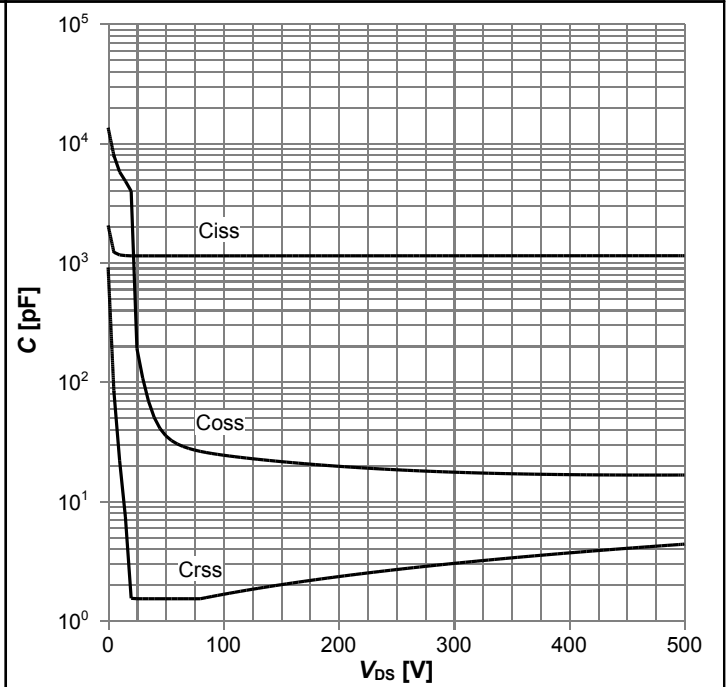
$E_{AS}=f(T_j); I_D=5.4 \text{ A}; V_{DD}=50 \text{ V}$

Diagram 13: Drain-source breakdown voltage



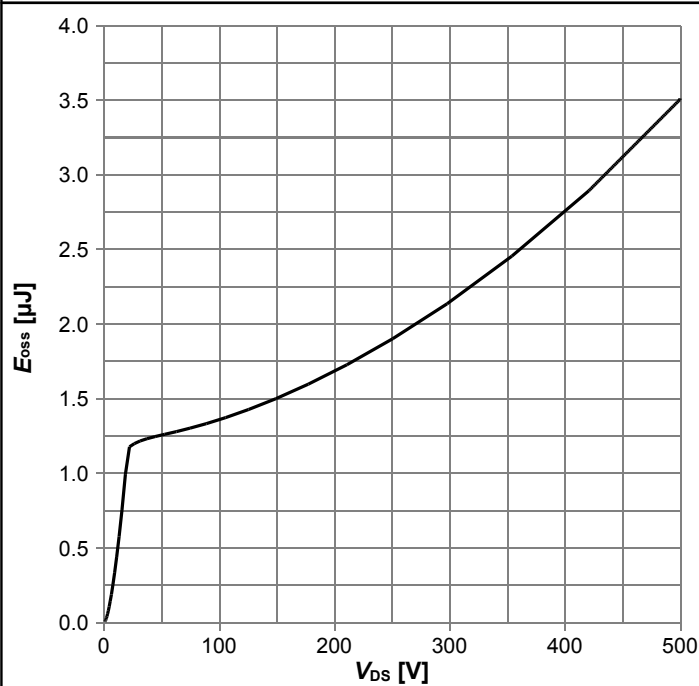
$V_{BR(DSS)}=f(T_j); I_D=1 \text{ mA}$

Diagram 14: Typ. capacitances



$C=f(V_{DS}); V_{GS}=0 \text{ V}; f=250 \text{ kHz}$

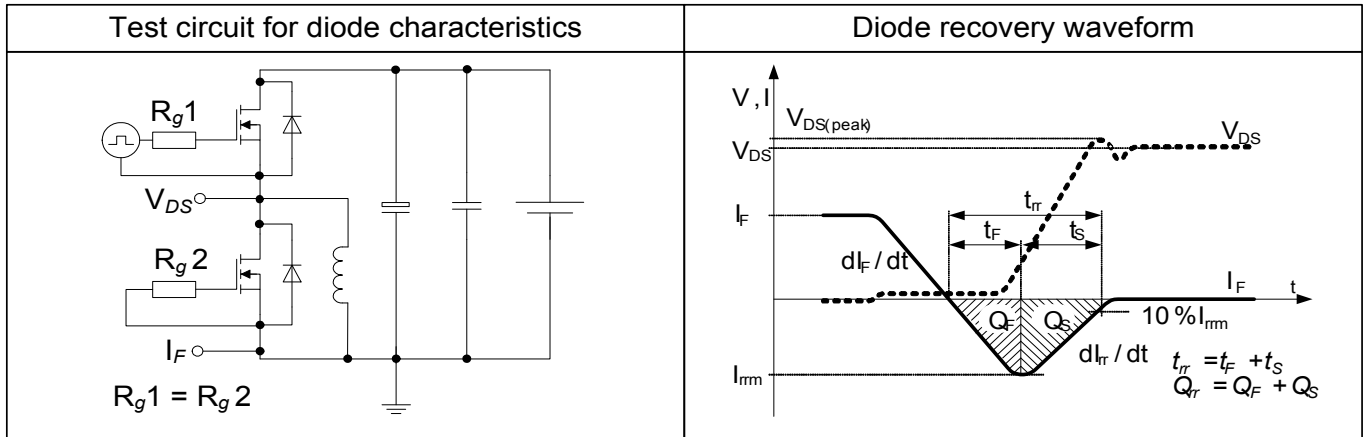
Diagram 15: Typ. Coss stored energy



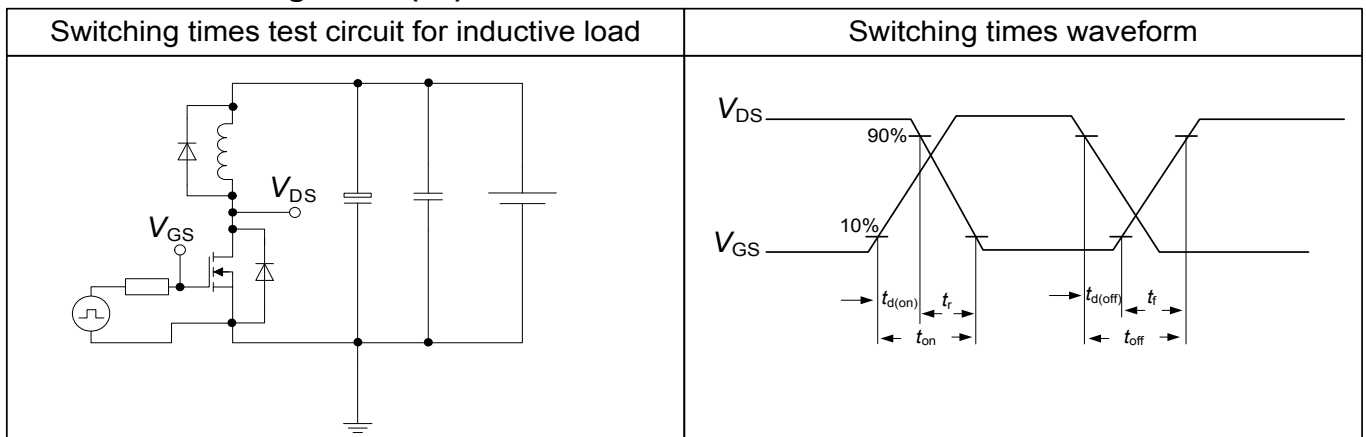
$E_{oss}=f(V_{DS})$

## 6 Test Circuits

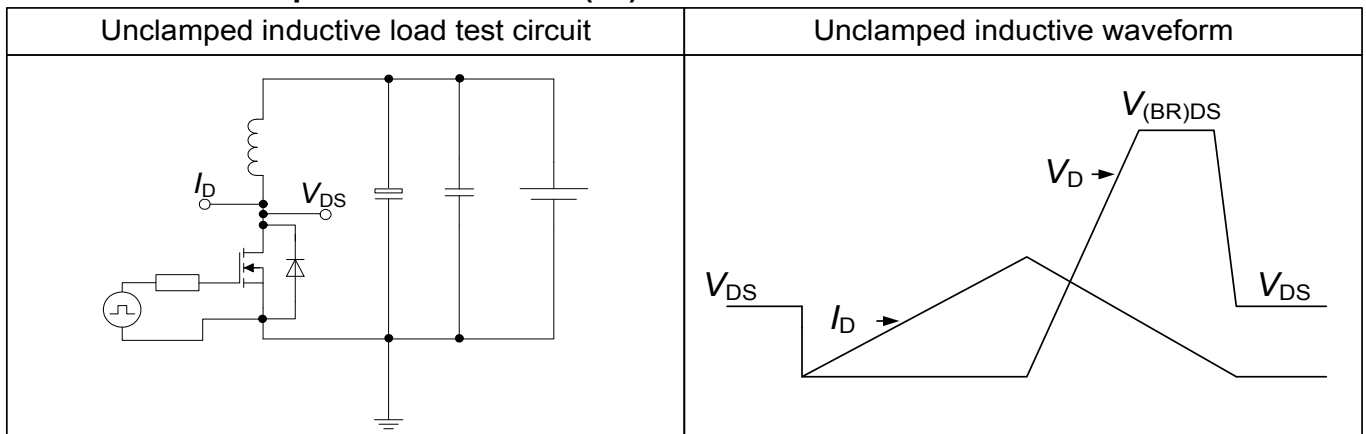
**Table 8 Diode characteristics**



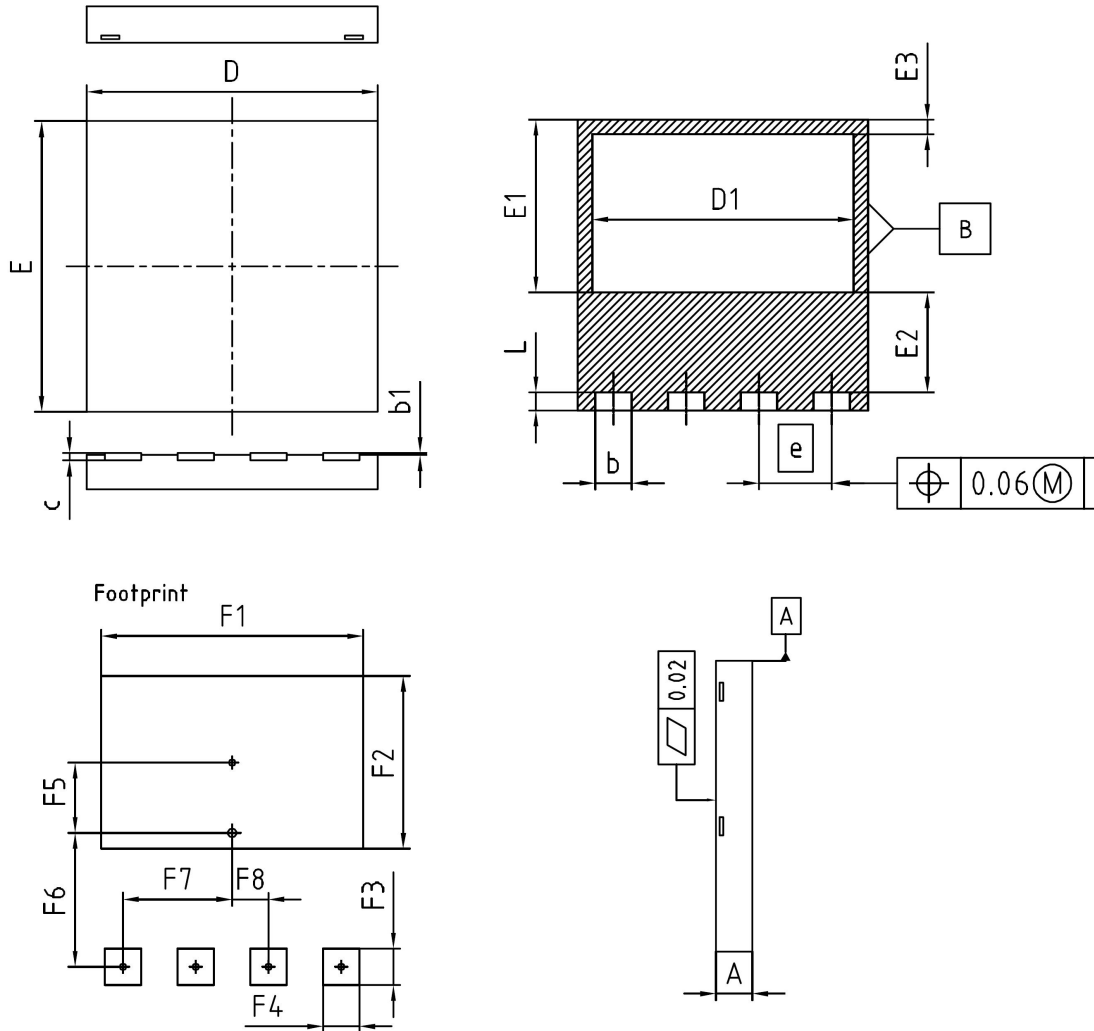
**Table 9 switching times (ss)**



**Table 10 Unclamped inductive load (ss)**



## 7 Package Outlines



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	0.90	1.10	0.035	0.043
b	0.90	1.10	0.035	0.043
b1	0.00	0.05	0.000	0.002
c	0.10	0.30	0.004	0.012
D	7.90	8.10	0.311	0.319
D1	7.10	7.30	0.280	0.287
E	7.90	8.10	0.311	0.319
E1	4.65	4.85	0.183	0.191
E2	2.65	2.85	0.104	0.112
E3	0.30	0.50	0.012	0.020
e	2.00 (BSC)		0.079 (BSC)	
L	0.40	0.60	0.016	0.024
N	4		4	
F1	7.20		0.283	
F2	4.75		0.187	
F3	1.00		0.039	
F4	1.00		0.039	
F5	1.43		0.056	
F6	4.20		0.165	
F7	3.00		0.118	
F8	1.00		0.039	

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Figure 1 Outline PG-VSON-4, dimensions in mm/inches

## 8 Appendix A

### Table 11 Related Links

- IFX CoolMOS™ C7 Webpage: [www.infineon.com](http://www.infineon.com)
- IFX CoolMOS™ C7 application note: [www.infineon.com](http://www.infineon.com)
- IFX CoolMOS™ C7 simulation model: [www.infineon.com](http://www.infineon.com)
- IFX Design tools: [www.infineon.com](http://www.infineon.com)

## Revision History

IPL65R195C7

**Revision: 2013-11-06, Rev. 2.0**

Previous Revision

Revision	Date	Subjects (major changes since last revision)
2.0	2013-11-06	Release of final version

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Any information within this document that you feel is wrong, unclear or missing at all? Your feedback will help us to continuously improve the quality of this document. Please send your proposal (including a reference to this document) to:

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