

MOSFET

700V CoolMOS™ CE Power Transistor

CoolMOS™ is a revolutionary technology for high voltage power MOSFETs, designed according to the superjunction (SJ) principle and pioneered by Infineon Technologies. CoolMOS™ CE is a price-performance optimized platform enabling to target cost sensitive applications in Consumer and Lighting markets by still meeting highest efficiency standards. The new series provides all benefits of a fast switching Superjunction MOSFET while not sacrificing ease of use and offering the best cost down performance ratio available on the market.

Features

- Extremely low losses due to very low FOM $R_{DS(on)} \cdot Q_g$ and Eoss
- Very high commutation ruggedness
- Easy to use/drive
- Pb-free plating, Halogen free mold compound
- Qualified for standard grade applications

Applications

(QR) Flyback in low power chargers for mobile devices and power tools

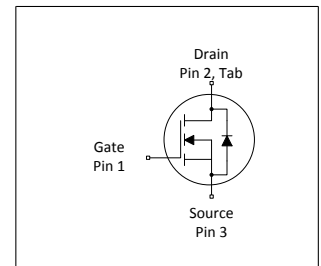
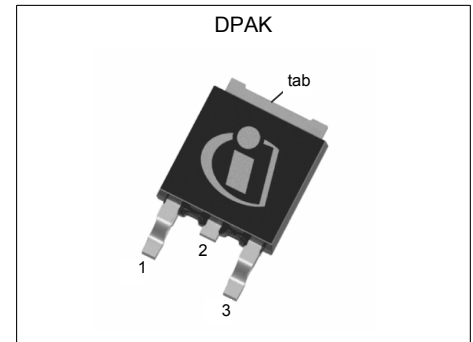


Table 1 Key Performance Parameters

| Parameter | Value | Unit |
|----------------------|-------|------------|
| $V_{DS} @ T_{j,max}$ | 750 | V |
| $R_{DS(on),max}$ | 2000 | m Ω |
| $I_{d,typ}$ | 4 | A |
| $Q_{g,typ}$ | 7.8 | nC |
| $I_{D,pulse}$ | 6.3 | A |
| $E_{oss@400V}$ | 0.85 | μ J |



| Type / Ordering Code | Package | Marking | Related Links |
|----------------------|-----------|----------|----------------|
| IPD70R2K0CE | PG-TO 252 | 70S2K0CE | see Appendix A |

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1 Maximum ratings

at $T_j = 25^\circ\text{C}$, unless otherwise specified

Table 2 Maximum ratings

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|--|---------------|--------|------|----------|------------------|---|
| | | Min. | Typ. | Max. | | |
| Continuous drain current ¹⁾ | I_D | - | - | 4 2.6 | A | $T_C=25^\circ\text{C}$ $T_C=100^\circ\text{C}$ |
| Pulsed drain current ²⁾ | $I_{D,pulse}$ | - | - | 6.3 | A | $T_C=25^\circ\text{C}$ |
| Avalanche energy, single pulse | E_{AS} | - | - | 11 | mJ | $I_D=0.4\text{A}$; $V_{DD}=50\text{V}$; see table 10 |
| Avalanche energy, repetitive | E_{AR} | - | - | 0.07 | mJ | $I_D=0.4\text{A}$; $V_{DD}=50\text{V}$; see table 10 |
| Avalanche current, repetitive | I_{AR} | - | - | 0.4 | A | - |
| MOSFET dv/dt ruggedness | dv/dt | - | - | 50 | V/ns | $V_{DS}=0\dots480\text{V}$ |
| Gate source voltage (static) | V_{GS} | -20 | - | 20 | V | static; |
| Gate source voltage (dynamic) | V_{GS} | -30 | - | 30 | V | AC ($f>1\text{ Hz}$) |
| Power dissipation | P_{tot} | - | - | 42 | W | $T_C=25^\circ\text{C}$ |
| Storage temperature | T_{stg} | -40 | - | 150 | $^\circ\text{C}$ | - |
| Operating junction temperature | T_j | -40 | - | 150 | $^\circ\text{C}$ | - |
| Continuous diode forward current | I_S | - | - | 2.9 | A | $T_C=25^\circ\text{C}$ |
| Diode pulse current ²⁾ | $I_{S,pulse}$ | - | - | 6.3 | A | $T_C=25^\circ\text{C}$ |
| Reverse diode dv/dt ³⁾ | dv/dt | - | - | 15 | V/ns | $V_{DS}=0\dots400\text{V}$, $I_{SD}\leq I_S$, $T_j=25^\circ\text{C}$ see table 8 |
| Maximum diode commutation speed | di_f/dt | - | - | 500 | A/ μs | $V_{DS}=0\dots400\text{V}$, $I_{SD}\leq I_S$, $T_j=25^\circ\text{C}$ see table 8 |

¹⁾ Limited by $T_{j,max}$. Maximum duty cycle $D=0.50$

²⁾ Pulse width t_p limited by $T_{j,max}$

³⁾ Identical low side and high side switch with identical R_G

2 Thermal characteristics

Table 3 Thermal characteristics

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|--|------------|--------|------|------|------|-------------------------------------|
| | | Min. | Typ. | Max. | | |
| Thermal resistance, junction - case | R_{thJC} | - | - | 2.95 | °C/W | - |
| Thermal resistance, junction - ambient | R_{thJA} | - | - | 62 | °C/W | leaded |
| Soldering temperature, wavesoldering only allowed at leads | T_{sold} | - | - | 260 | °C | 1.6mm (0.063 in.) from case for 10s |

3 Electrical characteristics

at $T_j=25^\circ\text{C}$, unless otherwise specified

Table 4 Static characteristics

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|----------------------------------|---------------|--------|--------------|-----------|----------|---|
| | | Min. | Typ. | Max. | | |
| Drain-source breakdown voltage | $V_{(BR)DSS}$ | 700 | - | - | V | $V_{GS}=0V, I_D=1mA$ |
| Gate threshold voltage | $V_{(GS)th}$ | 2.5 | 3.0 | 3.5 | V | $V_{DS}=V_{GS}, I_D=0.07mA$ |
| Zero gate voltage drain current | I_{DSS} | - | - | 1 | μA | $V_{DS}=700V, V_{GS}=0V, T_j=25^\circ C$ $V_{DS}=700V, V_{GS}=0V, T_j=150^\circ C$ |
| Gate-source leakage current | I_{GSS} | - | - | 100 | nA | $V_{GS}=20V, V_{DS}=0V$ |
| Drain-source on-state resistance | $R_{DS(on)}$ | - | 1.80 4.68 | 2.00 - | Ω | $V_{GS}=10V, I_D=1A, T_j=25^\circ C$ $V_{GS}=10V, I_D=1A, T_j=150^\circ C$ |
| Gate resistance | R_G | - | 6.5 | - | Ω | $f=1MHz, \text{open drain}$ |

Table 5 Dynamic characteristics

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|--|--------------|--------|------|------|------|--|
| | | Min. | Typ. | Max. | | |
| Input capacitance | C_{iss} | - | 163 | - | pF | $V_{GS}=0V, V_{DS}=100V, f=1MHz$ |
| Output capacitance | C_{oss} | - | 14 | - | pF | $V_{GS}=0V, V_{DS}=100V, f=1MHz$ |
| Effective output capacitance, energy related ¹⁾ | $C_{o(er)}$ | - | 10 | - | pF | $V_{GS}=0V, V_{DS}=0...480V$ |
| Effective output capacitance, time related ²⁾ | $C_{o(tr)}$ | - | 33 | - | pF | $I_D=\text{constant}, V_{GS}=0V, V_{DS}=0...480V$ |
| Turn-on delay time | $t_{d(on)}$ | - | 6.4 | - | ns | $V_{DD}=400V, V_{GS}=13V, I_D=1.1A,$ $R_G=10.2\Omega$; see table 9 |
| Rise time | t_r | - | 9 | - | ns | $V_{DD}=400V, V_{GS}=13V, I_D=1.1A,$ $R_G=10.2\Omega$; see table 9 |
| Turn-off delay time | $t_{d(off)}$ | - | 25 | - | ns | $V_{DD}=400V, V_{GS}=13V, I_D=1.1A,$ $R_G=10.2\Omega$; see table 9 |
| Fall time | t_f | - | 27 | - | ns | $V_{DD}=400V, V_{GS}=13V, I_D=1.1A,$ $R_G=10.2\Omega$; see table 9 |

Table 6 Gate charge characteristics

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|-----------------------|---------------|--------|------|------|------|---|
| | | Min. | Typ. | Max. | | |
| Gate to source charge | Q_{GS} | - | 0.9 | - | nC | $V_{DD}=480V, I_D=1.1A, V_{GS}=0 \text{ to } 10V$ |
| Gate to drain charge | Q_{gd} | - | 4.3 | - | nC | $V_{DD}=480V, I_D=1.1A, V_{GS}=0 \text{ to } 10V$ |
| Gate charge total | Q_g | - | 7.8 | - | nC | $V_{DD}=480V, I_D=1.1A, V_{GS}=0 \text{ to } 10V$ |
| Gate plateau voltage | $V_{plateau}$ | - | 5.4 | - | V | $V_{DD}=480V, I_D=1.1A, V_{GS}=0 \text{ to } 10V$ |

¹⁾ $C_{o(er)}$ is a fixed capacitance that gives the same stored energy as C_{oss} while V_{DS} is rising from 0 to 480V

²⁾ $C_{o(tr)}$ is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 to 480V

Table 7 Reverse diode characteristics

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|-------------------------------|-----------|--------|------|------|---------|---|
| | | Min. | Typ. | Max. | | |
| Diode forward voltage | V_{SD} | - | 0.9 | - | V | $V_{GS}=0V, I_F=1.1A, T_j=25^\circ C$ |
| Reverse recovery time | t_{rr} | - | 187 | - | ns | $V_R=400V, I_F=1.1A, di_F/dt=100A/\mu s$; see table 8 |
| Reverse recovery charge | Q_{rr} | - | 0.8 | - | μC | $V_R=400V, I_F=1.1A, di_F/dt=100A/\mu s$; see table 8 |
| Peak reverse recovery current | I_{rrm} | - | 7 | - | A | $V_R=400V, I_F=1.1A, di_F/dt=100A/\mu s$; see table 8 |

4 Electrical characteristics diagrams

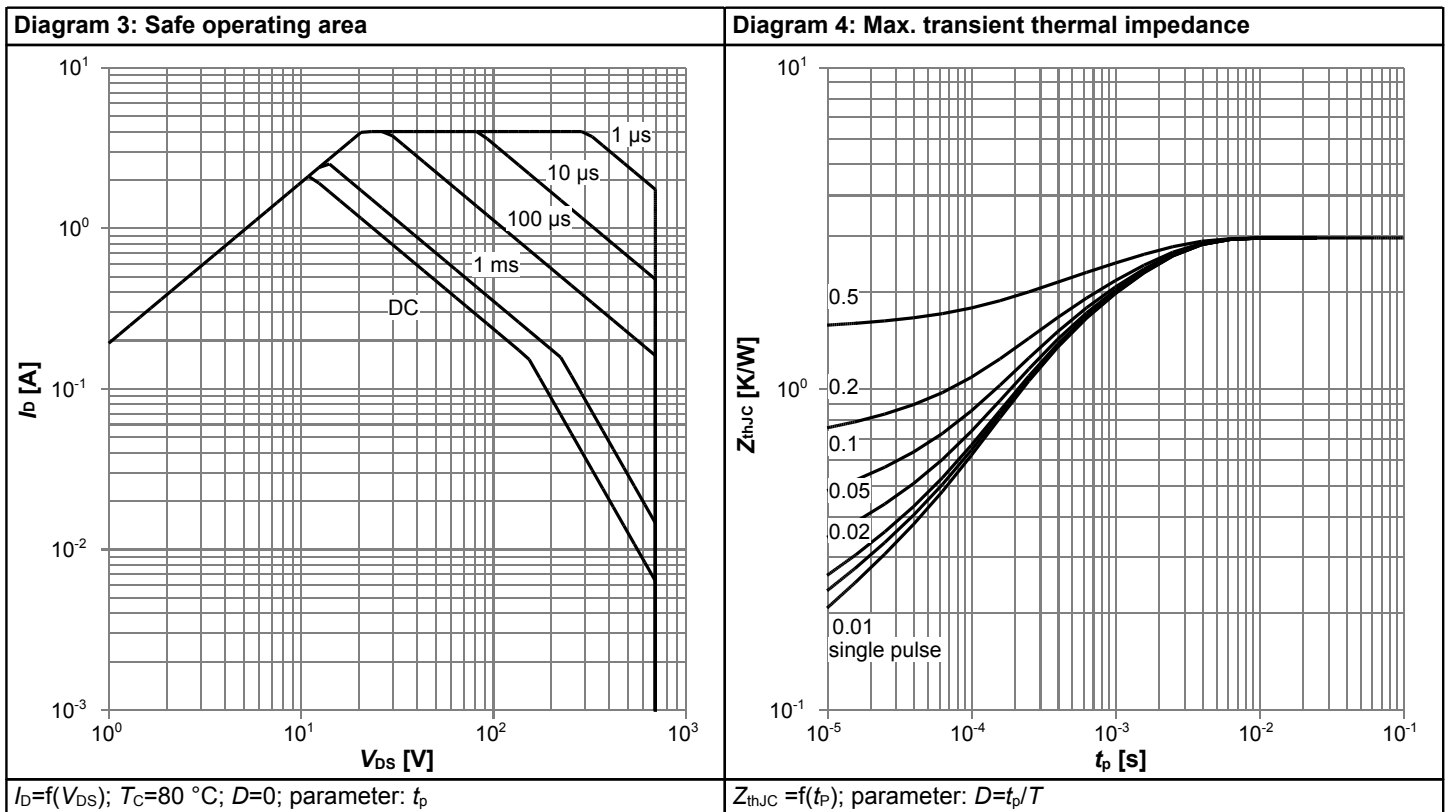
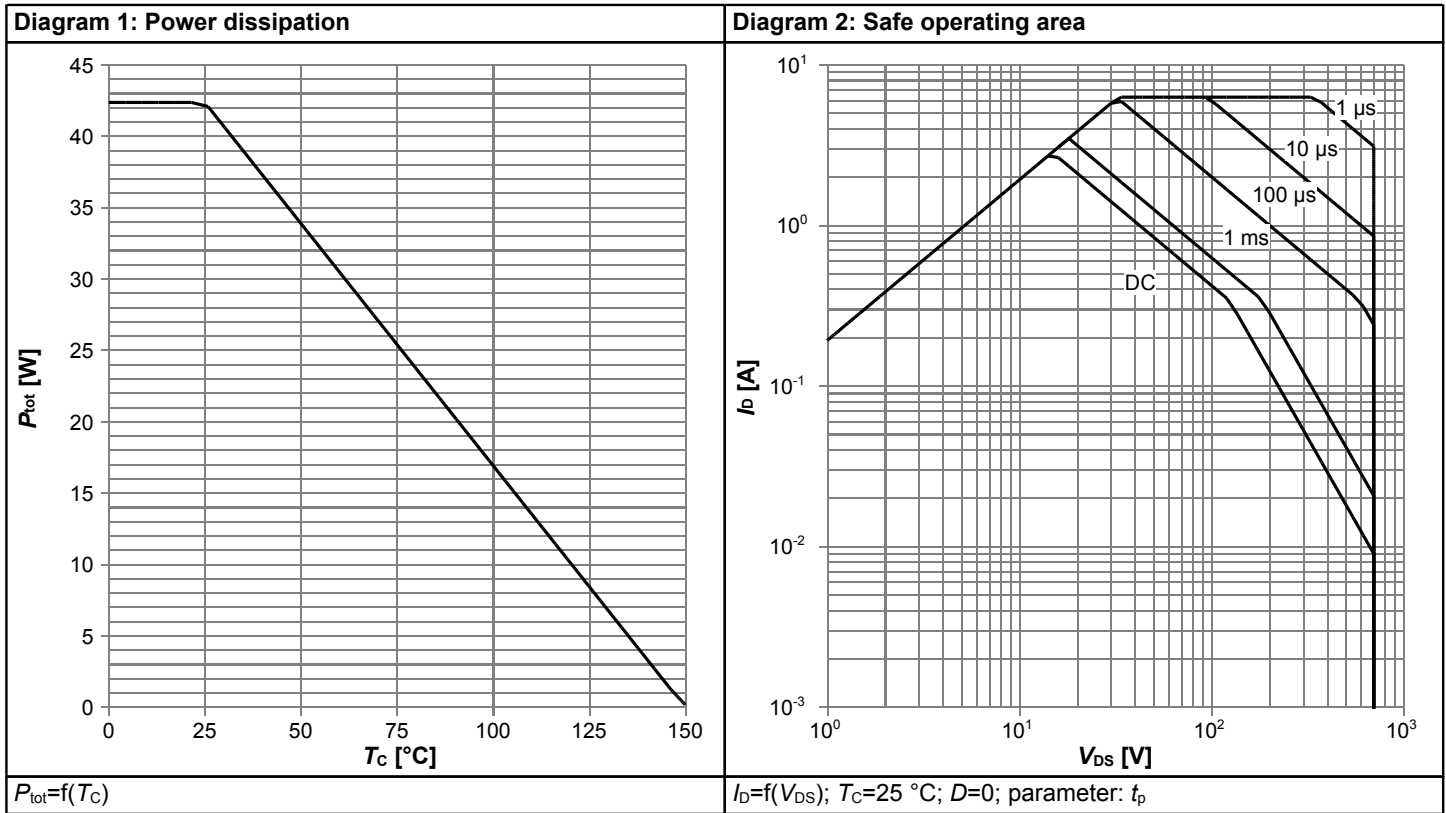
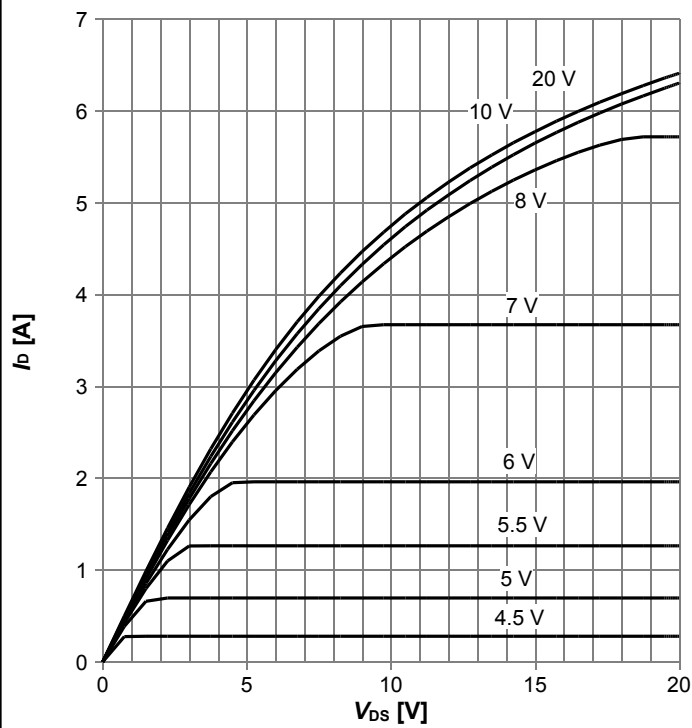
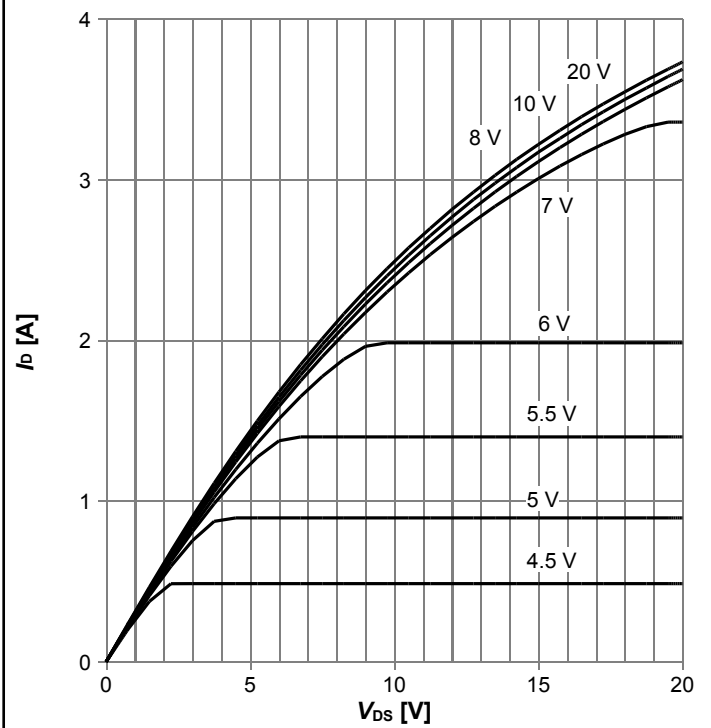


Diagram 5: Typ. output characteristics



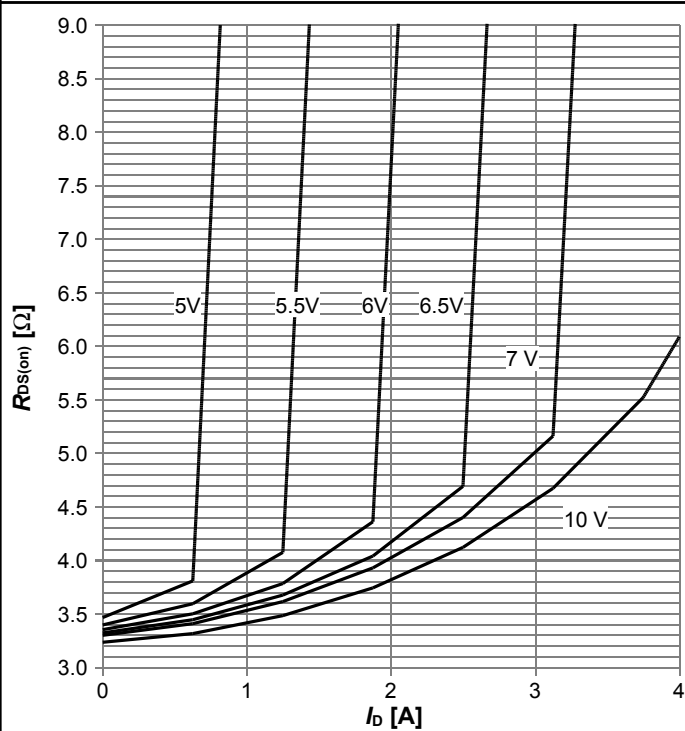
$I_D=f(V_{DS})$; $T_j=25\text{ }^\circ\text{C}$; parameter: V_{GS}

Diagram 6: Typ. output characteristics



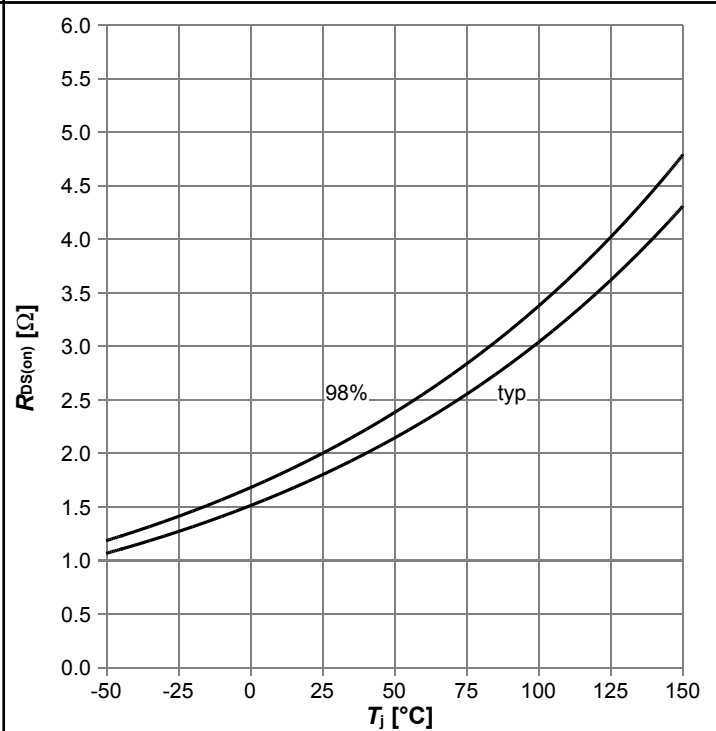
$I_D=f(V_{DS})$; $T_j=125\text{ }^\circ\text{C}$; parameter: V_{GS}

Diagram 7: Typ. drain-source on-state resistance



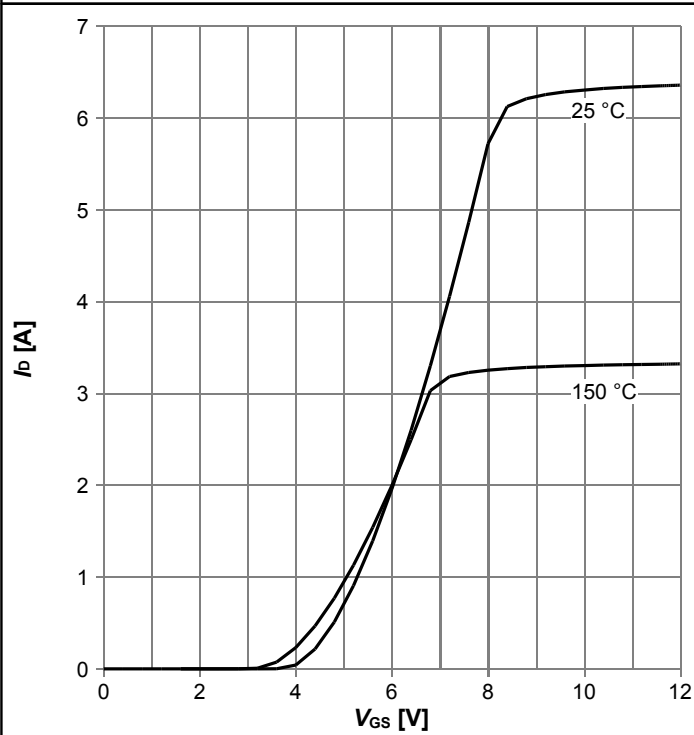
$R_{DS(on)}=f(I_D)$; $T_j=125\text{ }^\circ\text{C}$; parameter: V_{GS}

Diagram 8: Drain-source on-state resistance



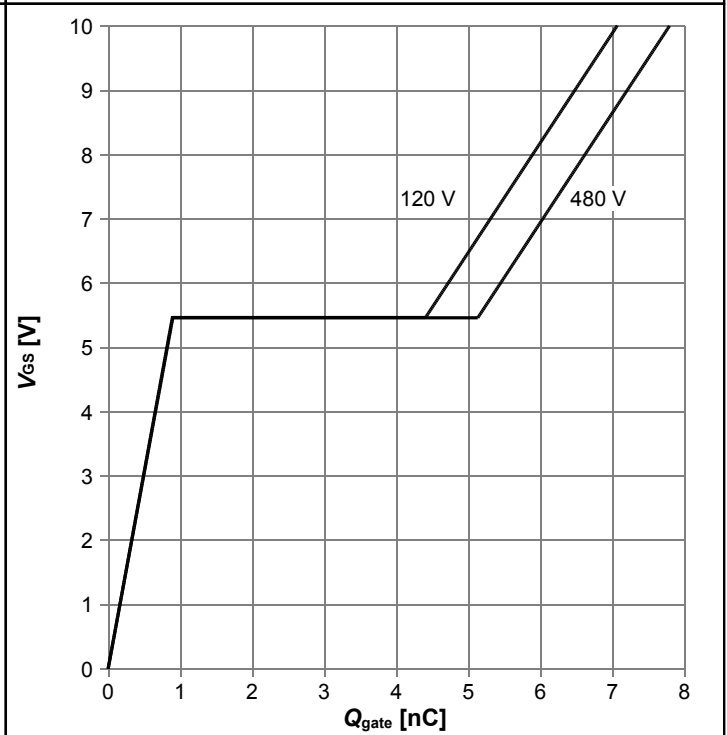
$R_{DS(on)}=f(T_j)$; $I_D=1.0\text{ A}$; $V_{GS}=10\text{ V}$

Diagram 9: Typ. transfer characteristics



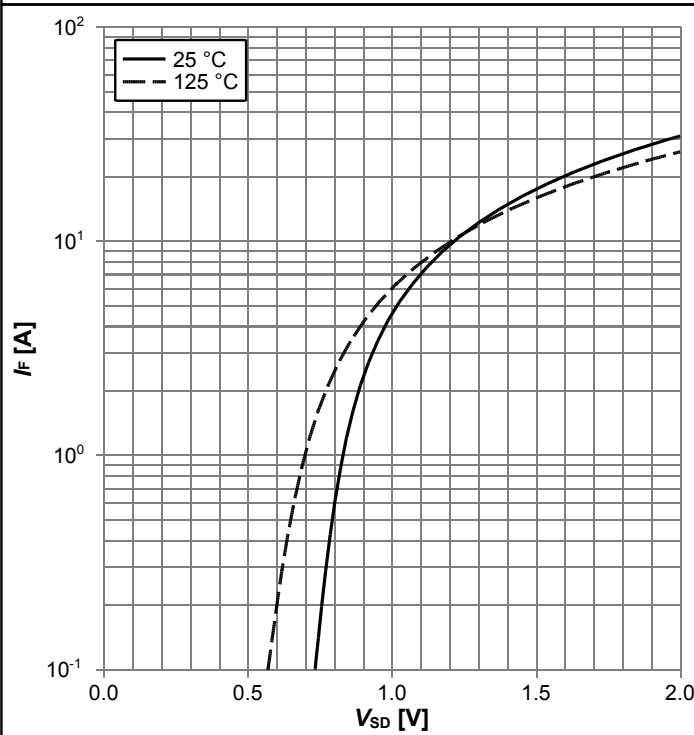
$I_D = f(V_{GS}); V_{DS} = 20V; \text{parameter: } T_j$

Diagram 10: Typ. gate charge



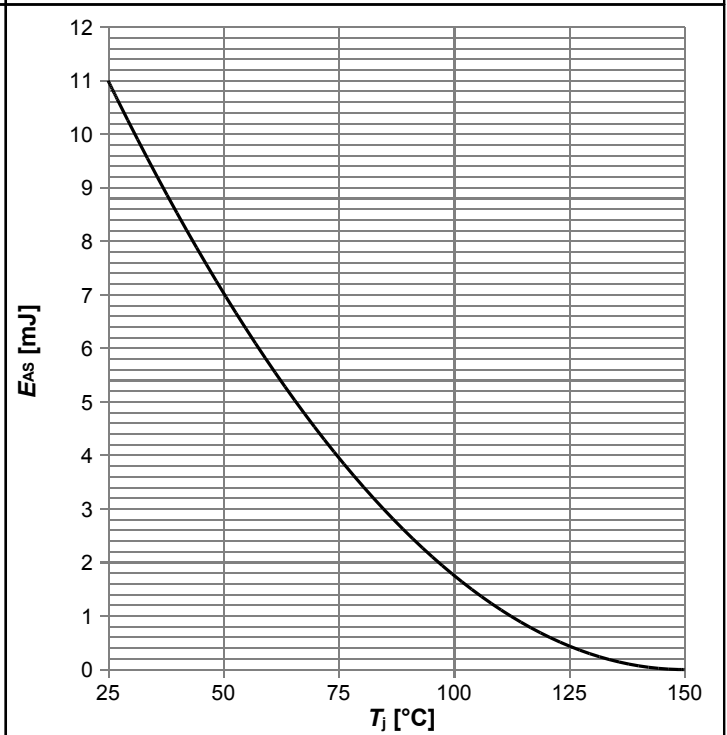
$V_{GS} = f(Q_{gate}); I_D = 1.1 \text{ A pulsed}; \text{parameter: } V_{DD}$

Diagram 11: Forward characteristics of reverse diode



$I_F = f(V_{SD}); \text{parameter: } T_j$

Diagram 12: Avalanche energy

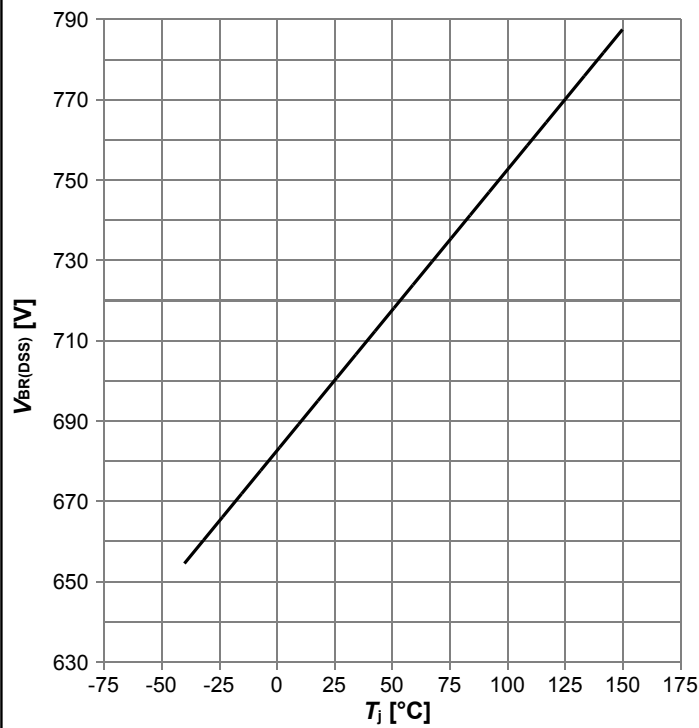


$E_{AS} = f(T_j); I_D = 0.5 \text{ A}; V_{DD} = 50 \text{ V}$

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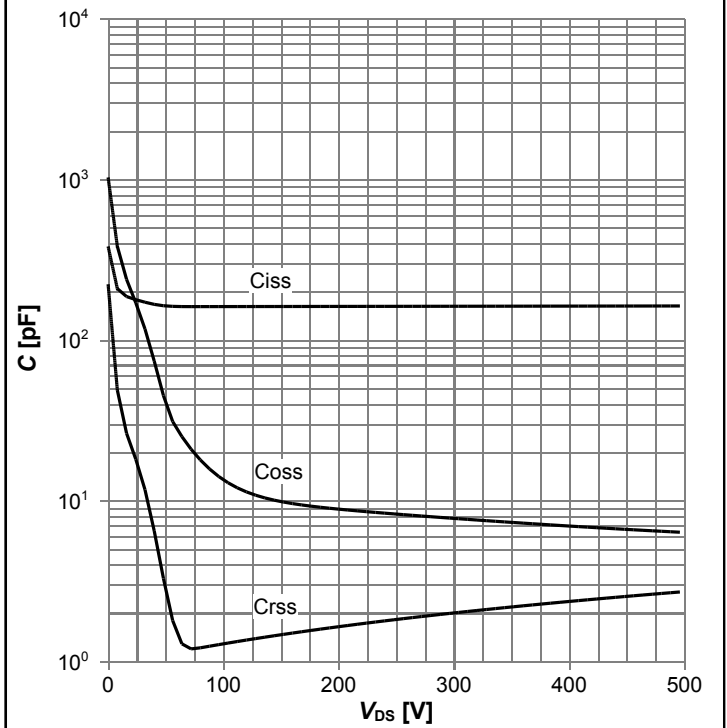
IPD70R2K0CE

Diagram 13: Drain-source breakdown voltage



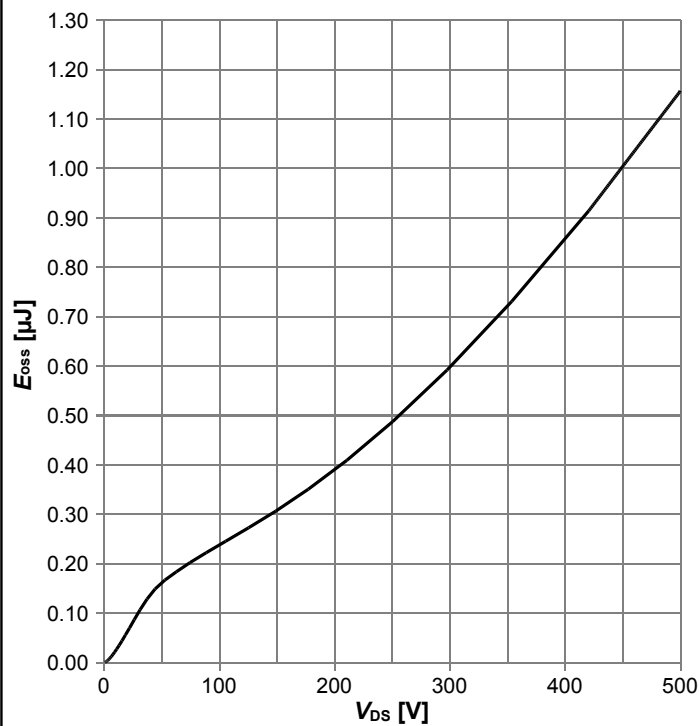
$V_{BR(DSS)}=f(T_j); I_D=1.0 \text{ mA}$

Diagram 14: Typ. capacitances



$C=f(V_{DS}); V_{GS}=0 \text{ V}; f=1 \text{ MHz}$

Diagram 15: Typ. Coss stored energy



$E_{oss}=f(V_{DS})$

5 Test Circuits

Table 8 Diode characteristics

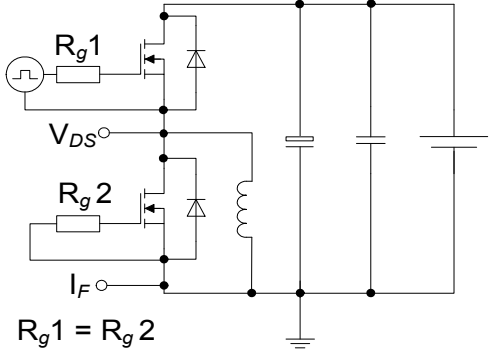
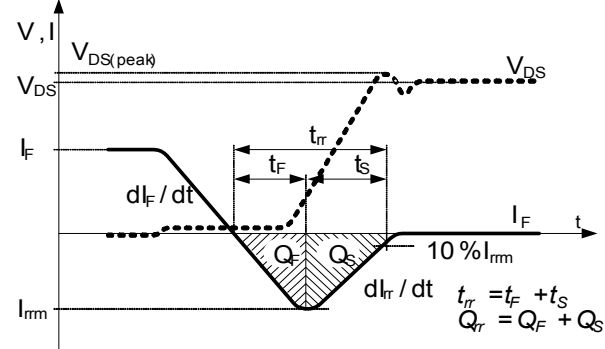
| Test circuit for diode characteristics | Diode recovery waveform |
|---|--|
|  <p>$R_{g1} = R_{g2}$</p> |  <p>$t_{rr} = t_r + t_s$ $Q_{rr} = Q_r + Q_s$</p> |

Table 9 Switching times

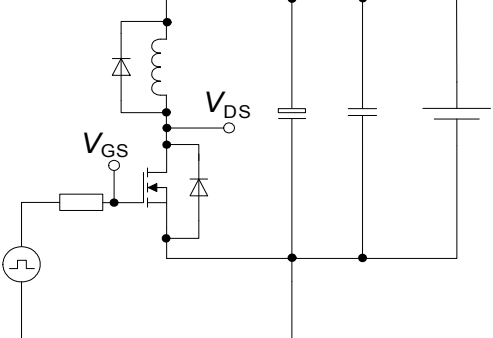
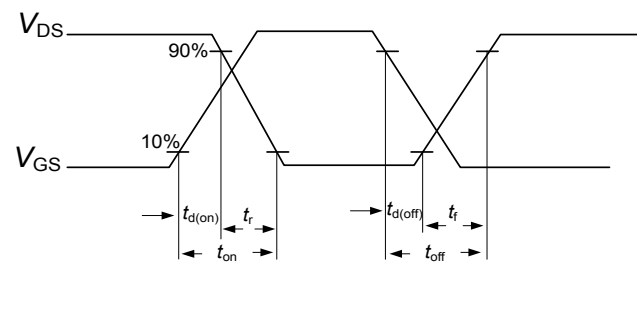
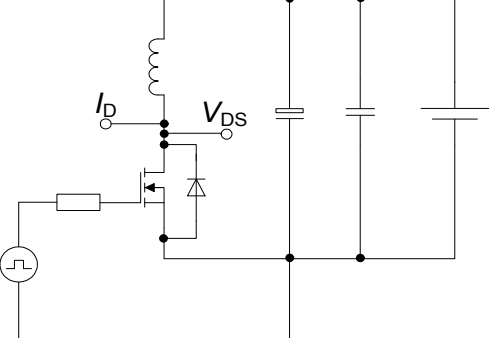
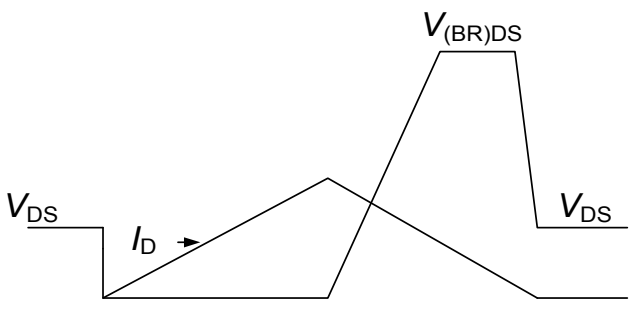
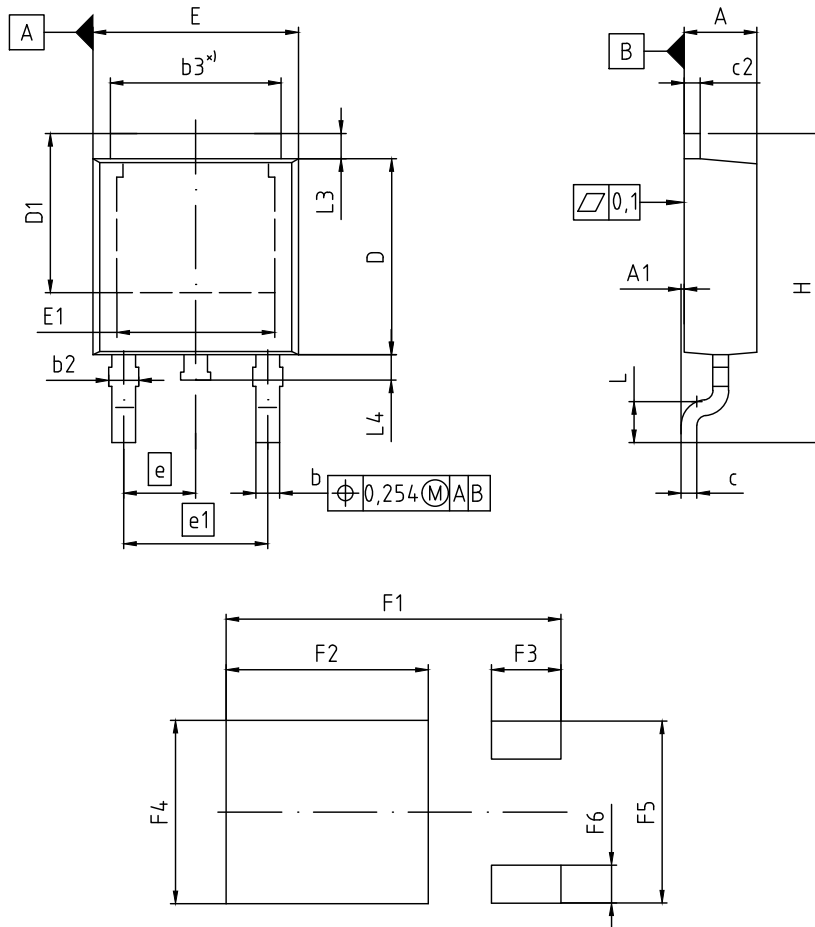
| Switching times test circuit for inductive load | Switching times waveform |
|--|---|
|  |  |

Table 10 Unclamped inductive load

| Unclamped inductive load test circuit | Unclamped inductive waveform |
|---|--|
|  |  |

6 Package Outlines



*) mold flash not included

| DIM | MILLIMETERS | | INCHES | |
|-----|-------------|-------|-------------|-------|
| | MIN | MAX | MIN | MAX |
| A | 2.16 | 2.41 | 0.085 | 0.095 |
| A1 | 0.00 | 0.15 | 0.000 | 0.006 |
| b | 0.64 | 0.89 | 0.025 | 0.035 |
| b2 | 0.65 | 1.15 | 0.026 | 0.045 |
| b3 | 5.00 | 5.50 | 0.197 | 0.217 |
| c | 0.46 | 0.60 | 0.018 | 0.024 |
| c2 | 0.46 | 0.98 | 0.018 | 0.039 |
| D | 5.97 | 6.22 | 0.235 | 0.245 |
| D1 | 5.02 | 5.84 | 0.198 | 0.230 |
| E | 6.40 | 6.73 | 0.252 | 0.265 |
| E1 | 4.70 | 5.60 | 0.185 | 0.220 |
| e | 2.29 (BSC) | | 0.090 (BSC) | |
| e1 | 4.57 (BSC) | | 0.180 (BSC) | |
| N | 3 | | 3 | |
| H | 9.40 | 10.48 | 0.370 | 0.413 |
| L | 1.18 | 1.70 | 0.046 | 0.067 |
| L3 | 0.90 | 1.25 | 0.035 | 0.049 |
| L4 | 0.51 | 1.00 | 0.020 | 0.039 |
| F1 | 10.60 | | 0.417 | |
| F2 | 6.40 | | 0.252 | |
| F3 | 2.20 | | 0.087 | |
| F4 | 5.80 | | 0.228 | |
| F5 | 5.76 | | 0.227 | |
| F6 | 1.20 | | 0.047 | |

| |
|------------------------------------|
| DOCUMENT NO. Z8B00003328 |
| SCALE 0 2.0 4mm |
| EUROPEAN PROJECTION |
| ISSUE DATE 01-09-2015 |
| REVISION 05 |

Figure 1 Outline PG-TO 252, dimensions in mm/inches

7 Appendix A

Table 11 Related Links

- **IFX CoolMOS™ CE Webpage:** www.infineon.com
- **IFX CoolMOS™ CE application note:** www.infineon.com
- **IFX CoolMOS™ CE simulation model:** www.infineon.com
- **IFX Design tools:** www.infineon.com

700V CoolMOS™ CE Power Transistor

IPD70R2K0CE

Revision History

IPD70R2K0CE

Revision: 2016-02-16, Rev. 2.0

Previous Revision

| Revision | Date | Subjects (major changes since last revision) |
|----------|------------|--|
| 2.0 | 2016-02-16 | Release of final version |

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