

# OT408

## 1 A Four-quadrant triac, high surge capability

Rev. 01 — 30 July 2008

Product data sheet

## 1. Product profile

### 1.1 General description

Passivated sensitive gate triac in a SOT223 surface-mountable plastic package

### 1.2 Features

- Sensitive gate
- Direct interfacing to logic level ICs
- High surge capability
- Gate triggering in four quadrants
- Direct interfacing to low power gate drive circuits
- High blocking voltage of 800 V

### 1.3 Applications

- Home appliances
- Small lamp control
- Low power motor control
- Low power loads in industrial process control

### 1.4 Quick reference data

- $V_{\text{DRM}} \leq 800 \text{ V}$
- $I_{\text{TSM}} \leq 12.5 \text{ A}$  ( $t = 20 \text{ ms}$ )
- $I_{\text{T(RMS)}} \leq 1 \text{ A}$
- $I_{\text{GT}} \leq 5 \text{ mA}$
- $I_{\text{GT}} \leq 7 \text{ mA}$  (T2– G+)

## 2. Pinning information

Table 1. Pinning

Pin	Description	Simplified outline	Graphic symbol
1	main terminal 1 (T1)	<p>SOT223</p>	<p>sym051</p>
2	main terminal 2 (T2)		
3	gate (G)		
4	mounting base; main terminal 2 (T2)		

### 3. Ordering information

**Table 2. Ordering information**

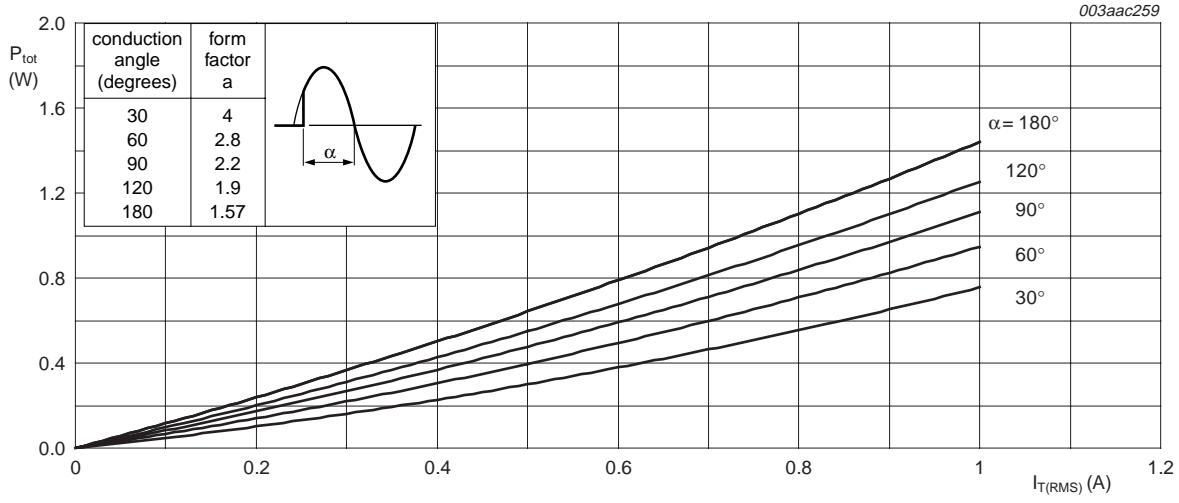
Type number	Package		Version
	Name	Description	
OT408	SC-73	plastic surface-mounted package with increased heatsink; 4 leads	SOT223

### 4. Limiting values

**Table 3. Limiting values**

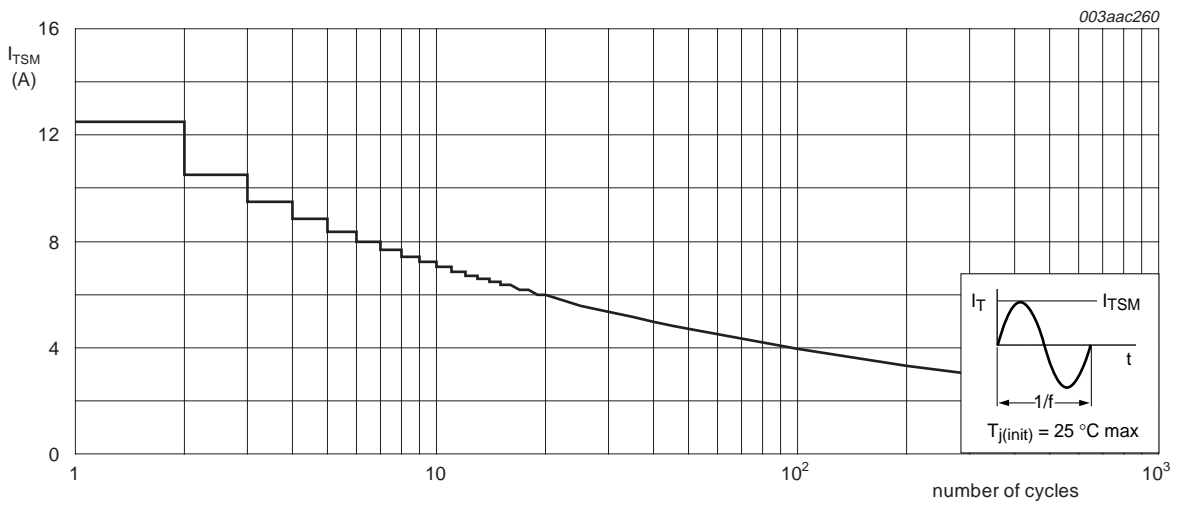
In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{DRM}$	repetitive peak off-state voltage		-	800	V
$V_{RRM}$	repetitive peak reverse voltage		-	800	V
$I_{T(RMS)}$	RMS on-state current	full sine wave; $T_{sp} \leq 103\text{ °C}$ ; see <a href="#">Figure 4</a> and <a href="#">5</a>	-	1	A
$I_{TSM}$	non-repetitive peak on-state current	full sine wave; $T_j = 25\text{ °C}$ prior to surge; see <a href="#">Figure 2</a> and <a href="#">3</a>			
		$t = 20\text{ ms}$	-	12.5	A
		$t = 16.7\text{ ms}$	-	13.8	A
$I^2t$	$I^2t$ for fusing	$t_p = 10\text{ ms}$	-	0.78	A <sup>2</sup> s
$di_T/dt$	rate of rise of on-state current	$I_{TM} = 1\text{ A}$ ; $I_G = 20\text{ mA}$ ; $di_G/dt = 0.2\text{ A}/\mu\text{s}$			
		T2+ G+	-	50	A/ $\mu\text{s}$
		T2+ G-	-	50	A/ $\mu\text{s}$
		T2- G-	-	50	A/ $\mu\text{s}$
		T2- G+	-	10	A/ $\mu\text{s}$
$I_{GM}$	peak gate current		-	1	A
$P_{GM}$	peak gate power		-	2	W
$P_{G(AV)}$	average gate power	over any 20 ms period	-	0.1	W
$T_{stg}$	storage temperature		-40	+150	°C
$T_j$	junction temperature		-	125	°C



$\alpha$  = conduction angle

Fig 1. Total power dissipation as a function of RMS on-state current; maximum values



f = 50 Hz

Fig 2. Non-repetitive peak on-state current as a function of the number of sinusoidal current cycles; maximum values

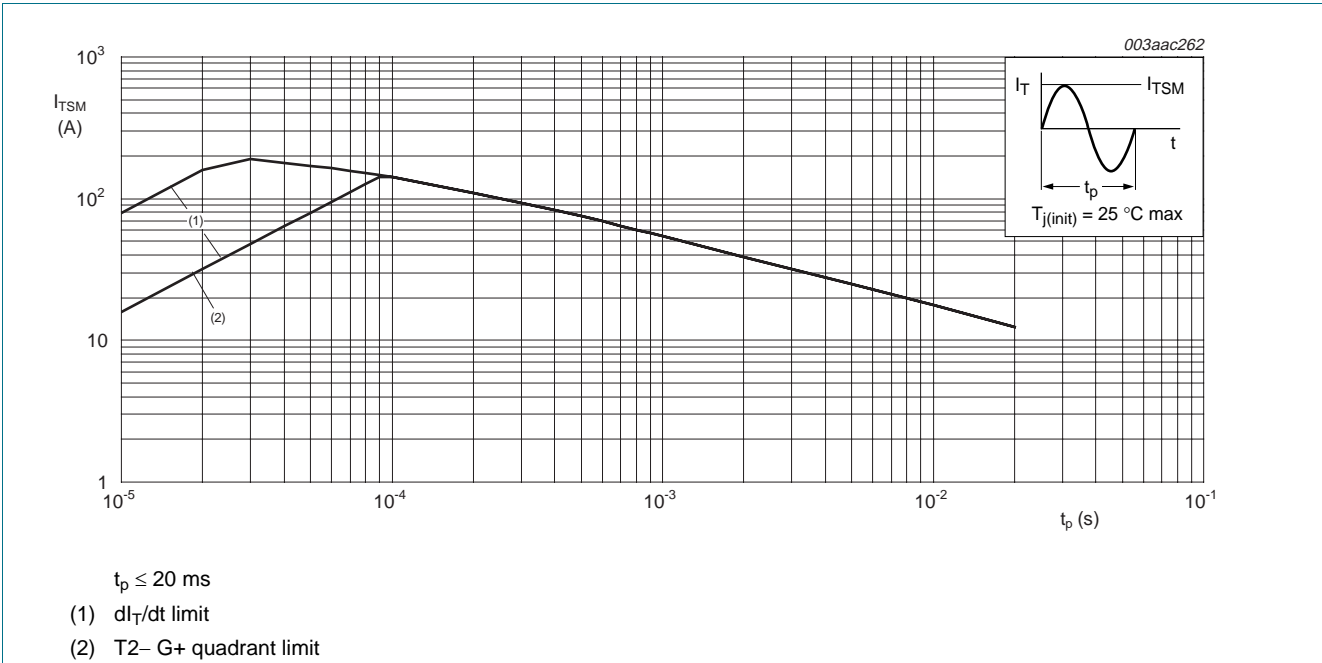


Fig 3. Non-repetitive peak on-state current as a function of pulse width; maximum values

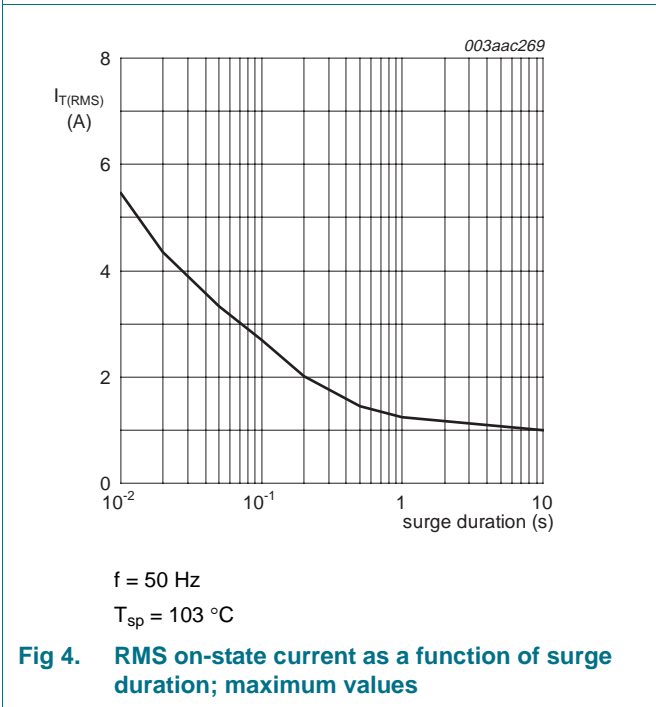


Fig 4. RMS on-state current as a function of surge duration; maximum values

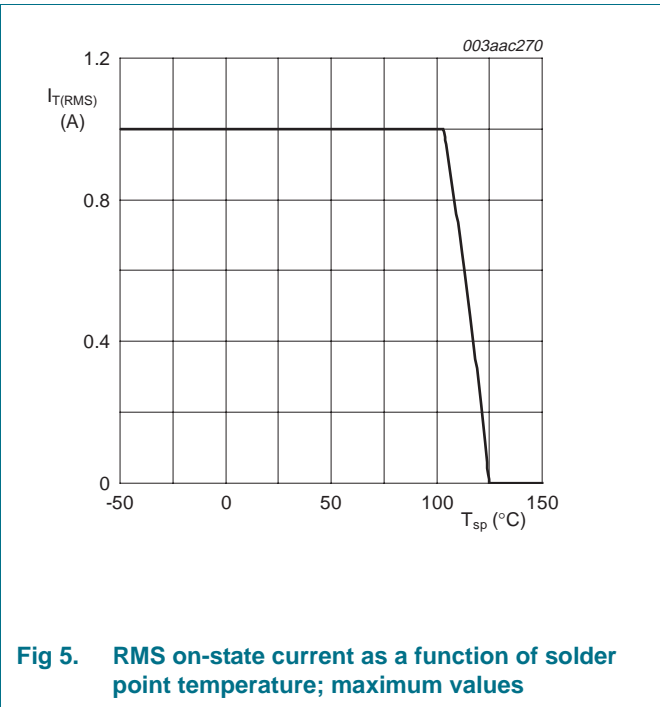
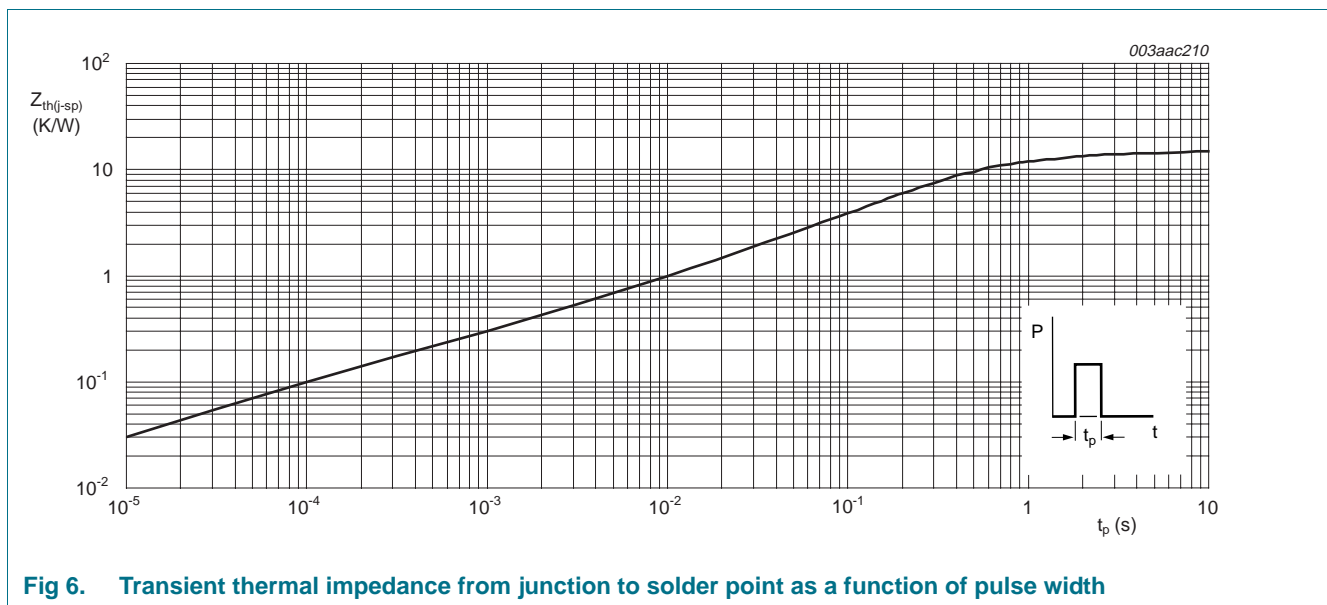


Fig 5. RMS on-state current as a function of solder point temperature; maximum values

## 5. Thermal characteristics

**Table 4. Thermal characteristics**

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-sp)}$	thermal resistance from junction to solder point	full cycle; see <a href="#">Figure 6</a>	-	-	15	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient	full cycle				
		for minimum footprint see <a href="#">Figure 13</a>	-	156	-	K/W
		for pad area see <a href="#">Figure 14</a>	-	70	-	K/W



**Fig 6. Transient thermal impedance from junction to solder point as a function of pulse width**

## 6. Static characteristics

**Table 5. Static characteristics**

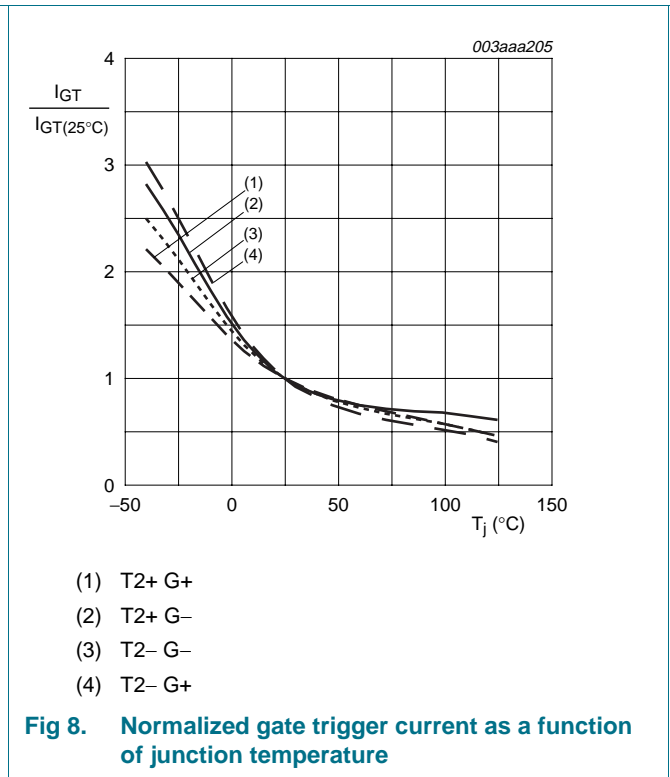
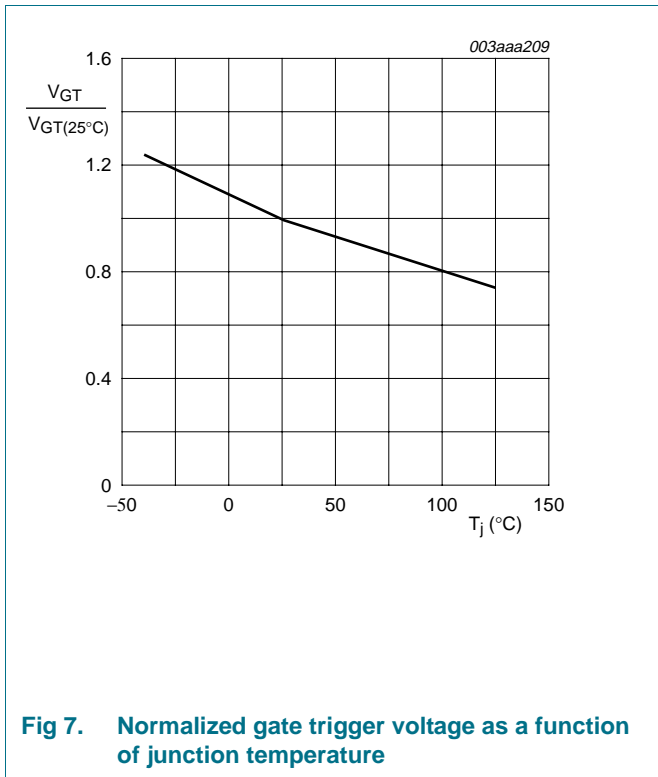
$T_j = 25\text{ °C}$  unless otherwise specified.

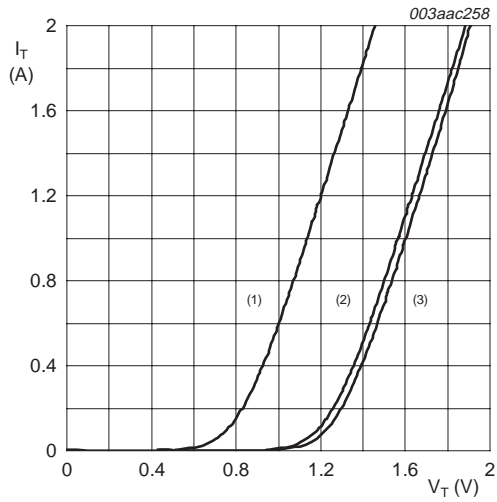
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$I_{GT}$	gate trigger current	$V_D = 12\text{ V}$ ; $I_T = 0.1\text{ A}$ ; see <a href="#">Figure 8</a>				
		T2+ G+	-	-	5	mA
		T2+ G-	-	-	5	mA
		T2- G-	-	-	5	mA
$I_L$	latching current	$V_D = 12\text{ V}$ ; $I_G = 0.1\text{ A}$ ; see <a href="#">Figure 10</a>				
		T2+ G+	-	-	10	mA
		T2+ G-	-	-	20	mA
		T2- G-	-	-	10	mA
$I_H$	holding current	$V_D = 12\text{ V}$ ; $I_G = 0.1\text{ A}$ ; see <a href="#">Figure 11</a>	-	-	10	mA
		T2- G+	-	-	10	mA
$V_T$	on-state voltage	$I_T = 1\text{ A}$ ; see <a href="#">Figure 9</a>	-	1.3	1.6	V
$V_{GT}$	gate trigger voltage	$V_D = 12\text{ V}$ ; $I_T = 0.1\text{ A}$ ; see <a href="#">Figure 7</a>	-	-	1.3	V
		$V_D = V_{DRM}$ ; $I_T = 0.1\text{ A}$ ; $T_j = 125\text{ °C}$	0.2	-	-	V
$I_D$	off-state current	$V_D = V_{DRM(max)}$ ; $T_j = 125\text{ °C}$	-	-	0.5	mA

## 7. Dynamic characteristics

**Table 6. Dynamic characteristics**

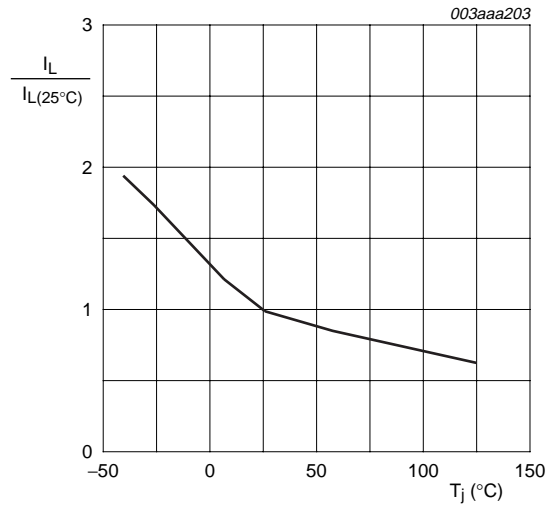
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$dV_D/dt$	rate of rise of off-state voltage	$V_{DM} = 0.67V_{DRM(max)}$ ; $T_j = 110\text{ }^\circ\text{C}$ ; exponential waveform; gate open circuit	20	-	-	V/ $\mu\text{s}$
$dV_{com}/dt$	rate of change of commutating voltage	$V_{DM} = 400\text{ V}$ ; $T_j = 110\text{ }^\circ\text{C}$ ; $I_{TM} = 1\text{ A}$ ; $di_{com}/dt = 0.44\text{ A/ms}$	1	-	-	V/ $\mu\text{s}$



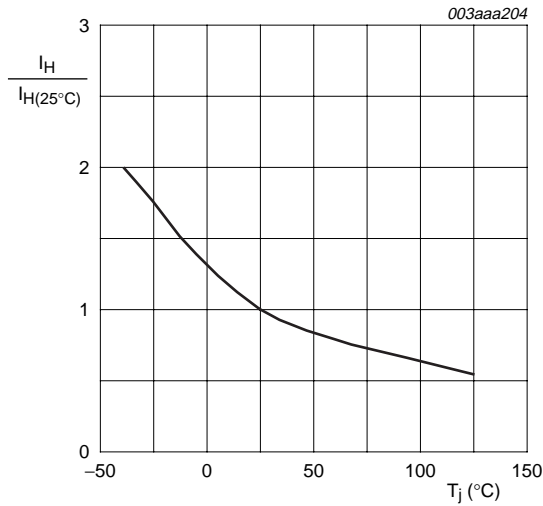


- $V_o = 1.254 \text{ V}; R_s = 0.31 \Omega$
- (1)  $T_j = 125 \text{ }^\circ\text{C}$ ; typical values
  - (2)  $T_j = 125 \text{ }^\circ\text{C}$ ; maximum values
  - (3)  $T_j = 25 \text{ }^\circ\text{C}$ ; maximum values

**Fig 9. On-state current as a function of on-state voltage**



**Fig 10. Normalized latching current as a function of junction temperature**



**Fig 11. Normalized holding current as a function of junction temperature**



8. Package outline

Plastic surface-mounted package with increased heatsink; 4 leads

SOT223

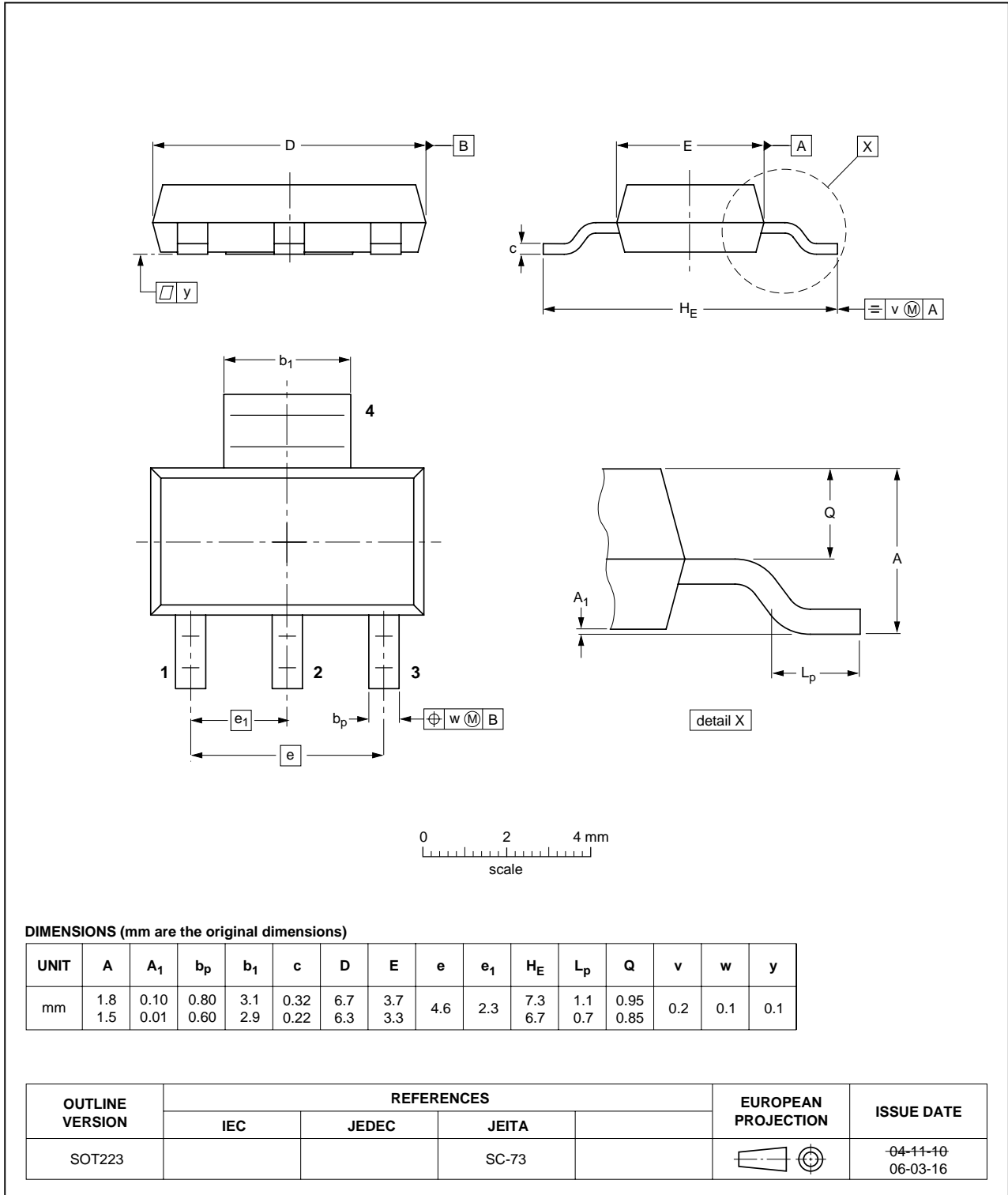
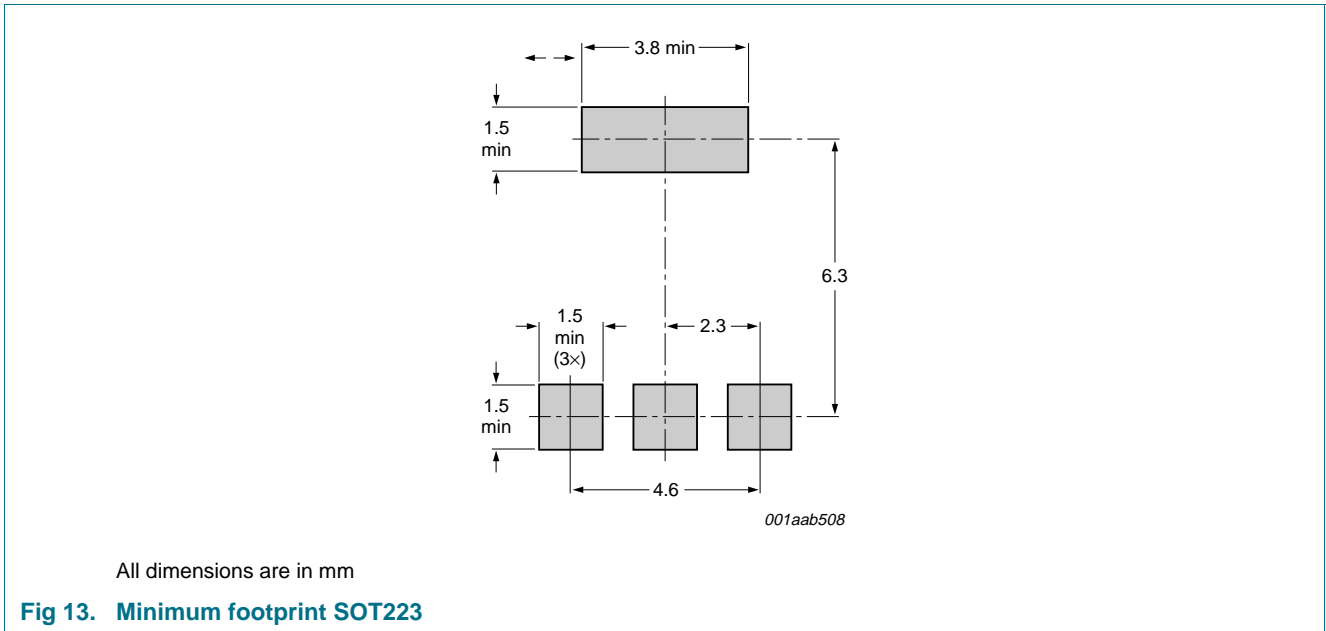


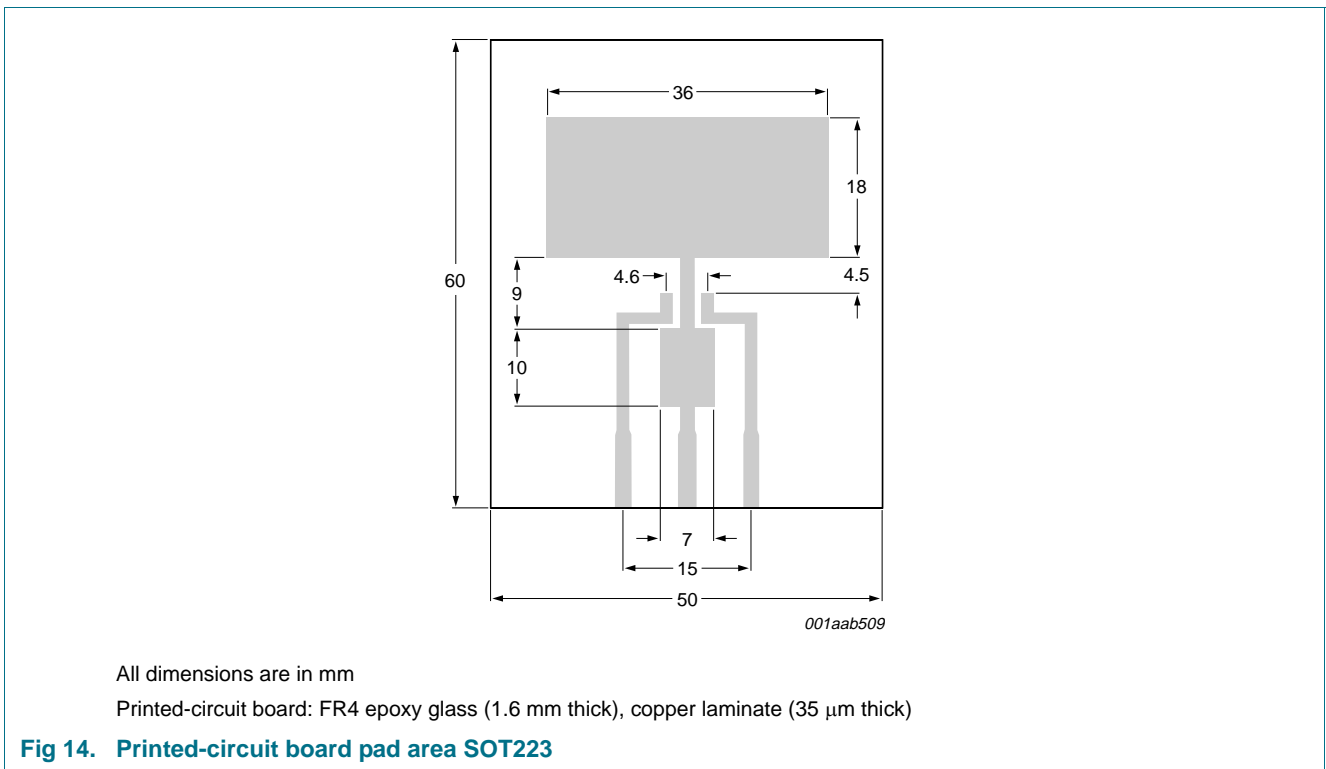
Fig 12. Package outline SOT223 (SC-73)

## 9. Mounting

### 9.1 Mounting instructions



### 9.2 Printed-circuit board



## 10. Revision history

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**Table 7.** Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
OT408_1	20080730	Product data sheet	-	-

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Document status <sup>[1][2]</sup>	Product status <sup>[3]</sup>	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
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