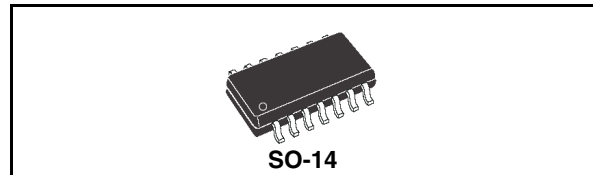


## 0.5 A high-side driver quad intelligent power switch

### Features

- Multipower BCD technology
- 0.5 A output current
- 8 to 35 V supply voltage range
- Externally programmable current limit
- Non-dissipative over-current protection
- Thermal shutdown
- Under voltage lockout with hysteresis
- Diagnostic output for under voltage, over temperature and over current
- External asynchronous reset input
- Presetable delay for overcurrent diagnostic
- Open ground protection
- Protection against surge transient (IEC 61000-4-5)
- Immunity against burst transient (IEC 61000-4-4)



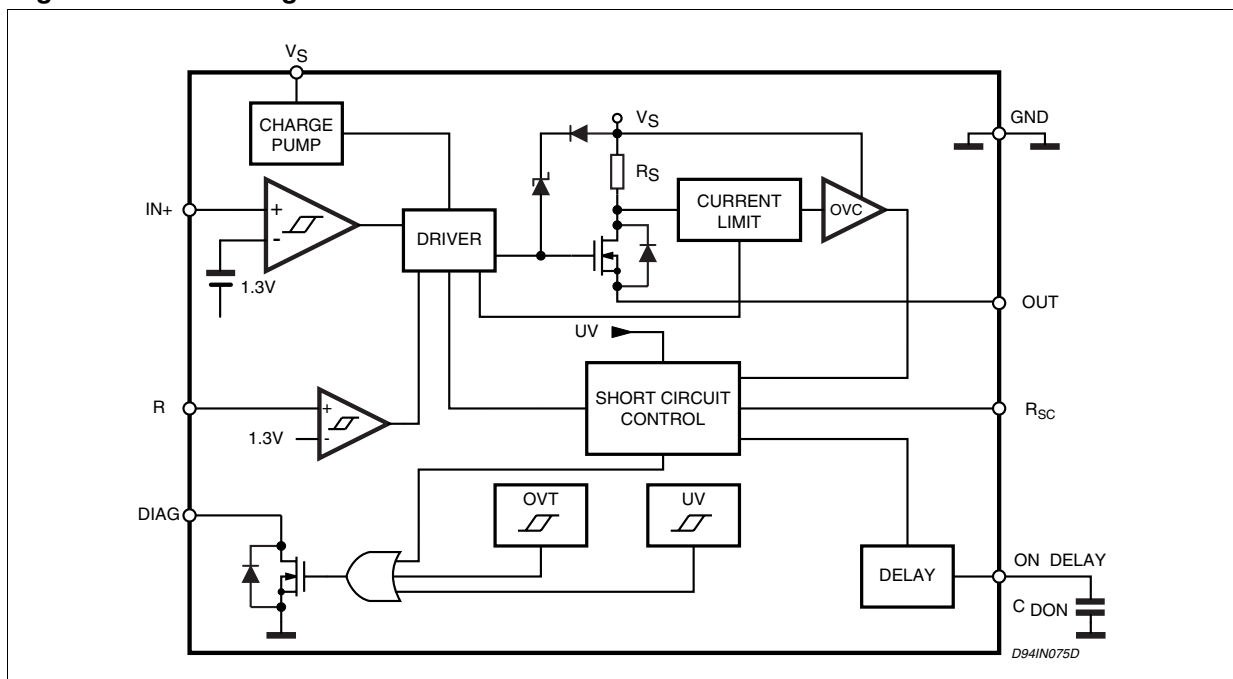
### Description

This device is a monolithic intelligent power switch in multipower BCD technology for driving inductive, capacitive or resistive loads. Diagnostic for CPU feedback and extensive use of electrical protections make this device inherently indestructible and suitable for general purpose industrial applications.

**Table 1. Device summary**

Order codes	Package	Packaging
L6377D	SO-14	Tube
L6377D013TR	SO-14	Tape and reel

**Figure 1. Block diagram**



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# 1 Maximum rating

## 1.1 Absolute maximum ratings

**Table 2. Absolute maximum ratings**

Symbol	Pin	Parameter	Value	Unit
$V_s$	4	Supply voltage ( $t_w \leq 10$ ms)	50	V
		Supply voltage (DC)	40	V
$V_s - V_{out}$	4 vs 3	Supply to output differential voltage	internally limited	
$V_{od}$	10	Externally forced voltage	-0.3 to 7	V
$I_{od}$		Externally forced current	$\pm 1$	mA
$I_{RESET}$	5	Reset input current (forced)	$\pm 2$	mA
$V_{RESET}$		Reset input voltage	-0.3 to 40	V
$I_{out}$	3	Output current (see also $I_{sc}$ )	internally limited	
$V_{out}$		Output voltage	internally limited	
$E_{il}$		Total energy inductive load ( $T_J = 125$ °C)	50	mJ
$P_{tot}$		Power dissipation	internally limited	
$V_{diag}$	11	External voltage	-0.3 to 40	V
$I_{diag}$		Externally forced current	-10 to 10	mA
$I_i$	12	Input current	20	mA
$V_i$		Input voltage	-10 to $V_s + 0.3$	V
$T_{op}$		Ambient temperature, operating range	-25 to 85	°C
$T_J$		Junction temperature, operating range (see overtemperature protection)	-25 to 125	°C
$T_{stg}$		Storage temperature	-55 to 150	°C

## 1.2 Thermal data

**Table 3. Thermal data**

Symbol	Parameter	Value	Unit
$R_{thJA}$	Thermal resistance, junction to ambient (max)	150	°C/W

## 2 Pin connections

Figure 2. Pin connections (top view)

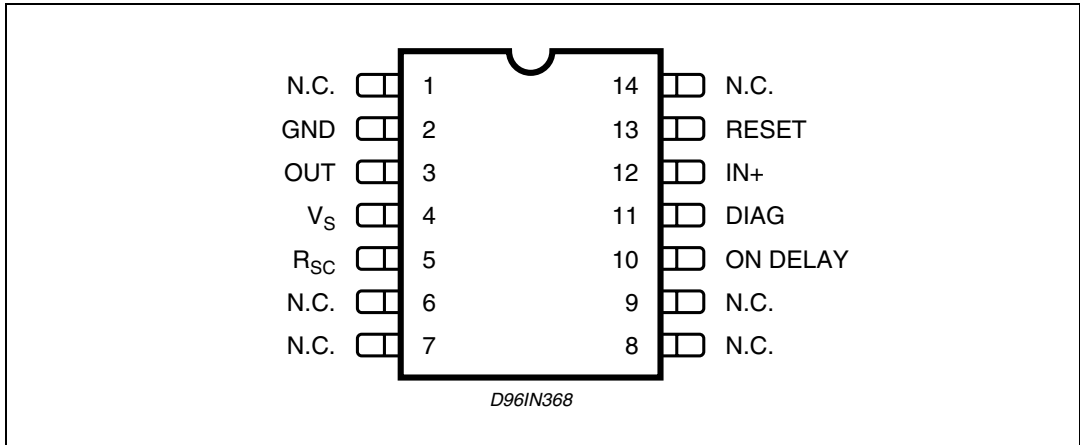


Table 4. Pin description

N#	Pin name	Function
1, 6, 7, 8, 9, 14	N.C.	Not connected
2	GND	Ground pin
3	OUT	High side output. Controlled output with current limitation
4	Vs	Supply voltage. Range with under voltage monitoring
5	Rsc	Current limiting setting
10	ON DELAY	Delay setting for overcurrent diagnostic
11	DIAG	Diagnostic open drain output for over temperature, under voltage and overcurrent
12	IN+	Comparator non inverting input
13	RESET	Asynchronous reset input

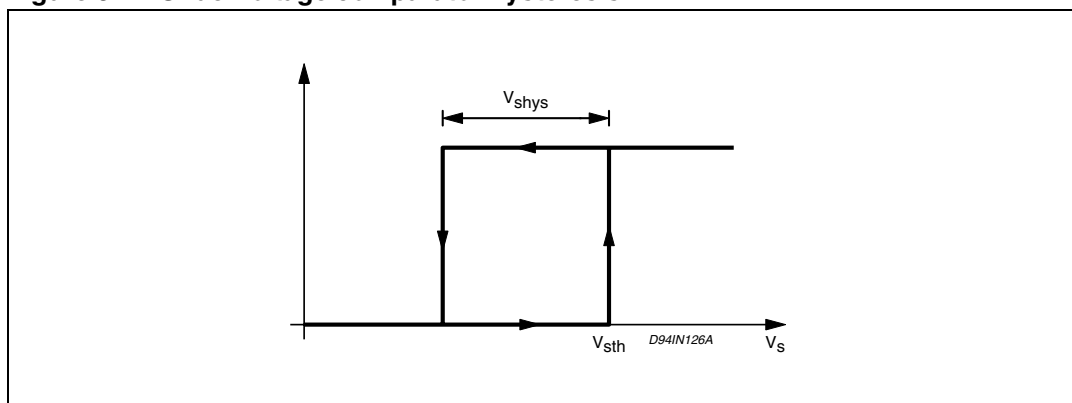
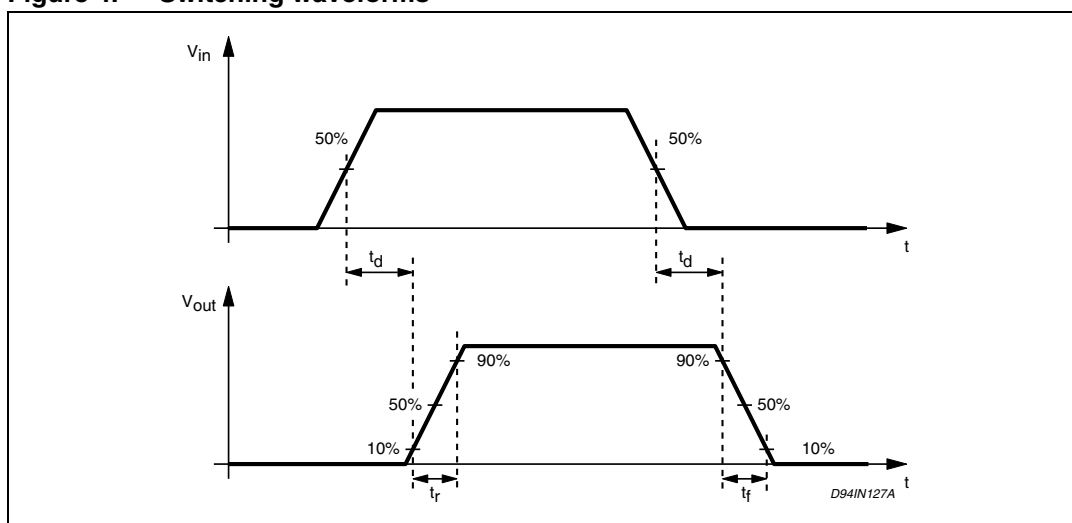
### 3 Electrical characteristics

**Table 5. Electrical characteristics**  
( $V_s = 24\text{ V}$ ;  $T_J = -25\text{ to }125\text{ }^\circ\text{C}$ ; unless otherwise specified.)

Symbol	Pin	Parameter	Test condition	Min	Typ	Max	Unit
<b>DC operation</b>							
$V_{smin}$	4	Supply voltage for valid diagnostic	$I_{diag} \geq 0.5\text{ mA}$ ; $V_{diag} = 1.5\text{ V}$ ;	4		35	V
$V_s$		Operative supply voltage		8	24	35	V
$V_{sth}$		Under voltage lower threshold		7		8	V
$V_{shys}$		Under voltage hysteresis		300	500	700	mV
$I_q$		Quiescent current	Output open		800		$\mu\text{A}$
$I_{qo}$		Quiescent current	Output on		1.6		mA
$V_{ith}$		12	Input threshold voltage		0.8	1.3	2
$V_{iths}$	Input threshold hysteresis			50		400	mV
$V_{il}$	Input low level voltage			-7		0.8	V
$V_{ih}$	Input high level voltage		$V_s < 18\text{ V}$	2		$V_s - 3$	V
			$V_s > 18\text{ V}$	2		15	V
$I_{ib}$	Input bias current		$V_i = -7\text{ to }15\text{ V}$	-250		250	$\mu\text{A}$
$V_{rth}$	13	Reset threshold voltage		0.8	1.3	2	V
$V_{rl}$		Reset low level voltage		0		0.8	V
$V_{rh}$		Reset high level voltage		2		40	V
$I_{rb}$		Reset pull down current			5		$\mu\text{A}$
$I_{dch}$	10	Delay capacitor charging current	ON delay pin shorted to Ground		2.5		$\mu\text{A}$
$V_{rsc}$	5	Output voltage on $R_{sc}$ pin	$R_{sc}$ pin floating		1.25		V
$I_{rsc}$		Output current on $R_{sc}$ pin	$R_{sc}$ pin shorted to GND			300	$\mu\text{A}$
$I_{dlkg}$	11	Diagnostic output leakage current	Diagnostic off			25	$\mu\text{A}$
$V_{diag}$		Diagnostic output voltage drop	$I_{diag} = 5\text{ mA}$ ;			1.5	V

**Table 5. Electrical characteristics** (continued)  
( $V_s = 24\text{ V}$ ;  $T_J = -25\text{ to }125\text{ }^\circ\text{C}$ ; unless otherwise specified.)

Symbol	Pin	Parameter	Test condition	Min	Typ	Max	Unit	
$V_{don}$		Output voltage drop	$I_{out} = 625\text{ mA}$ ; $T_J = 25\text{ }^\circ\text{C}$		250	350	mV	
			$I_{out} = 625\text{ mA}$ ; $T_J = 125\text{ }^\circ\text{C}$		400	550	mV	
$I_{olk}$	3	Output leakage current	$V_i = \text{LOW}$ ; $V_{out} = 0$			100	$\mu\text{A}$	
$V_{ol}$		Output low state voltage	$V_i = \text{HIGH}$ ; pin floating		0.8	1.5	V	
$V_{cl}$		Internal voltage clamp ( $V_s - V_{out}$ )	$I_o = 200\text{ mA}$ single pulsed =300ms	48	53	58	V	
$I_{sc}$		Short circuit output current	$V_s = 8\text{ to }35\text{ V}$ ; $R_l = 2\text{ }\Omega$ ; $R_{sc} = 5\text{ to }30\text{ K}\Omega$	$5/R_{sc} = \text{K}\Omega$				A
			$V_s = 8\text{ to }35\text{ V}$ ; $R_l = 2\text{ }\Omega$ ; $R_{sc} < 5\text{ K}\Omega$	0.75	1.1	1.5	A	
$T_{max}$		Over temperature upper threshold			150		$^\circ\text{C}$	
$T_{hys}$		Over temperature hysteresis			20		$^\circ\text{C}$	
<b>AC operation</b>								
$t_r - t_f$	3	Rise or fall time	$V_s = 24\text{ V}$ ; $R_l = 70\text{ }\Omega$ $R_l$ to ground		20		$\mu\text{s}$	
$t_d$		Delay time			5		$\mu\text{s}$	
dV/dt		Slew rate (rise and fall edge)	$V_s = 24\text{ V}$ ; $R_l = 70\text{ }\Omega$ $R_l$ to ground	0.7	1	1.5	V/ $\mu\text{s}$	
$t_{ON}$	10	On time during short circuit condition	$50\text{ pF} < C_{DON} < 2\text{ nF}$		1.28		$\mu\text{s/pF}$	
$t_{OFF}$		Off time during short circuit condition			64		$t_{ON}$	
$f_{max}$		Maximum operating frequency			25		kHz	
<b>Source drain NDMOS diode</b>								
$V_{fSD}$		Forward on voltage	$I_{fSD} = 625\text{ mA}$		1	1.5	V	
$I_{fp}$		Forward peak current	$t_p = 10\text{ ms}$ ; duty cycle = 20 %			1.5	A	
$t_{rr}$		Reverse recovery time	$I_{fSD} = 500\text{ mA}$ ; $dI_{fSD}/dt = 25\text{ A}/\mu\text{s}$		200		ns	
$t_{fr}$		Forward recovery time			50		ns	

**Figure 3. Undervoltage comparator hysteresis****Figure 4. Switching waveforms**

## 4 Input section

An Input and Asynchronous RESET, both TTL/CMOS compatible with wide voltage range and high noise immunity (thanks to a built in hysteresis) are available.

## 5 Over temperature protection (OVT)

An on-chip Over Temperature Protection provides an excellent protection of the device in extreme conditions. Whenever the temperature - measured on a central portion of the chip - exceeds  $T_{\max} = 150\text{ }^{\circ}\text{C}$  (typical value) the device is shut off, and the DIAG output goes LOW.

Normal operation is resumed as the chip temperature (normally after few seconds) falls below  $T_{\max} - T_{\text{hys}} = 130\text{ }^{\circ}\text{C}$  (typical value). The hysteresis avoid that an intermittent behaviour take place.

## 6 Under voltage protection (UV)

The supply voltage is expected to range from 8 to 35 V. In this range the device operates correctly. Below 8V the overall system has to be considered not reliable. To avoid any misfunctioning the supply voltage is continuously monitored to provide an under voltage protection. As  $V_s$  falls below  $V_{\text{sth}} - V_{\text{shys}}$  (typically 7.5 V, see fig. 4) the output power MOS is switched off and DIAG output goes LOW. Normal operation is resumed as soon as  $V_s$  exceeds  $V_{\text{sth}}$ . The hysteretic behaviour prevents intermittent operation at low supply voltage.



## 7 Over current operation

In order to implement a short circuit protection the output power MOS is driven in linear mode to limit the output current to the  $I_{sc}$  value. This  $I_{sc}$  limit is externally settable by means of an external 1/4 W resistor connected from  $R_{sc}$  pin and GND. The value of the resistor must be chosen according to the following formula:

$$I_{sc} \text{ (A)} = 5/R_{sc} \text{ (k}\Omega\text{)}$$

with

$$5 < R_{sc} < 30 \text{ (k}\Omega\text{)}$$

For

$$R_{sc} < 5 \text{ (k}\Omega\text{)}$$

$I_{sc}$  is limited to  $I_{sc} = 1.1 \text{ A}$  (typical value).

This condition (current limited to the  $I_{sc}$  value) lasts for a  $t_{on}$  time interval, that can be set by means of a capacitor ( $C_{DON}$ ) connected to the ON DELAY pin according to the following formula:

$$t_{on} = 1.28 \mu\text{s/pF}$$

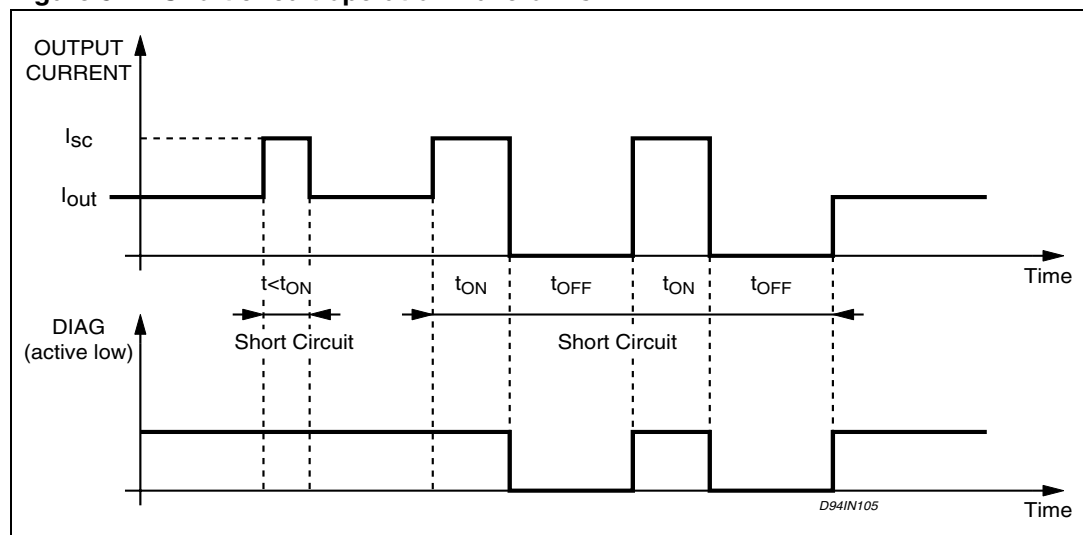
for

$$50 \text{ pF} < C_{DON} < 2 \text{ nF}$$

After the  $t_{on}$  interval has expired the output power MOS is switched off for the  $t_{off}$  time interval with:

$$t_{off} = 64 \cdot t_{on}$$

**Figure 5. Short circuit operation waveforms**



When also the  $t_{OFF}$  interval has expired, the output power MOS is switched ON.

Now two conditions may occur

- the overload is still present. In this case the output power MOS is again driven in linear mode (limiting the output current to  $I_{sc}$ ) for another  $t_{ON}$ , starting a new cycle, or
- the overload condition is removed, and the output power MOS is no longer driven in linear mode.

All these occurrences are presented on the DIAG pin (see fig 5). We call this unique feature non dissipative short circuit protection and it ensures a very safe operation even in permanent overload conditions. Note that, of course, choosing the most appropriate value for the  $t_{ON}$  interval (i.e. the value of the  $C_{DON}$  capacitor) a delay (the  $t_{ON}$  itself) will prevent that a misleading Short Circuit information is presented on the DIAG output, when driving capacitive loads (that acts like short circuit in the very beginning) or Incandescent Lamp (a cold filament has a very low resistive value).

The non dissipative short circuit protection can be disabled (keeping  $t_{ON} = 0$  but with the output current still limited to  $I_{sc}$ , and Diagnostic disabled) simply shorting to ground the the ON DELAY pin.

## 8 Demagnetisation of inductive loads

The L6377 has an internal clamping zener diode able to demagnetise inductive loads. Note that the limitation comes from the peak power that the package can handle. Attention must be paid to a proper thermal design of the board. If, for whatever reason (load current or inductive value too big) the peak power dissipation is too high, an external Zener plus Diode arrangement, can perform a demagnetisation versus Ground or versus  $V_S$  (see fig 5 and 6). The breakdown voltage of the external Zener Diode must be chosen considering the internal clamping voltage ( $V_{cl}$ ) and the supply voltage ( $V_S$ ) according to:

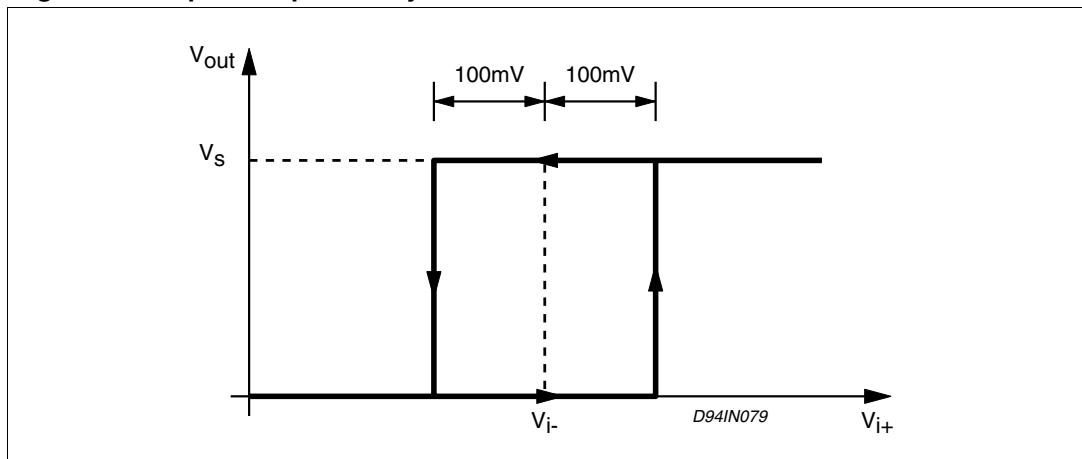
$$V_Z < V_{cl(min)} - V_{S(max)}$$

for demagnetisation versus ground or

$$V_{S(max)} < V_Z < V_{cl(min)}$$

for demagnetisation versus  $V_S$ .

**Figure 6. Input comparator hysteresis**



**Figure 7. External demagnetisation circuit (versus ground)**

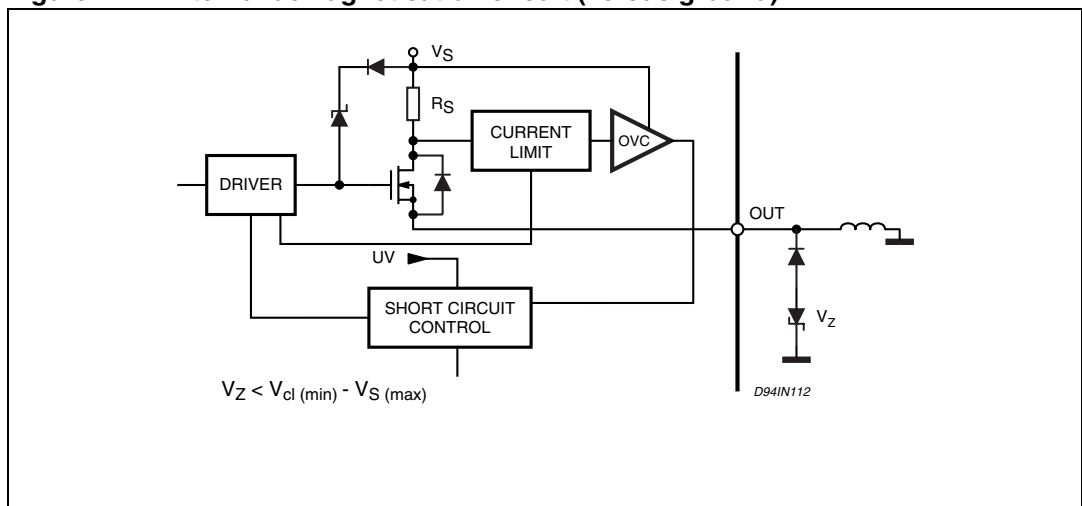
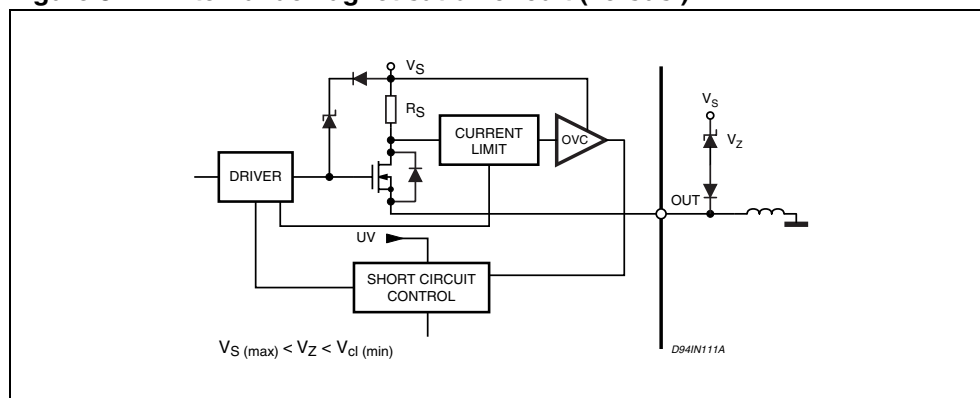


Figure 8. External demagnetisation circuit (versus )



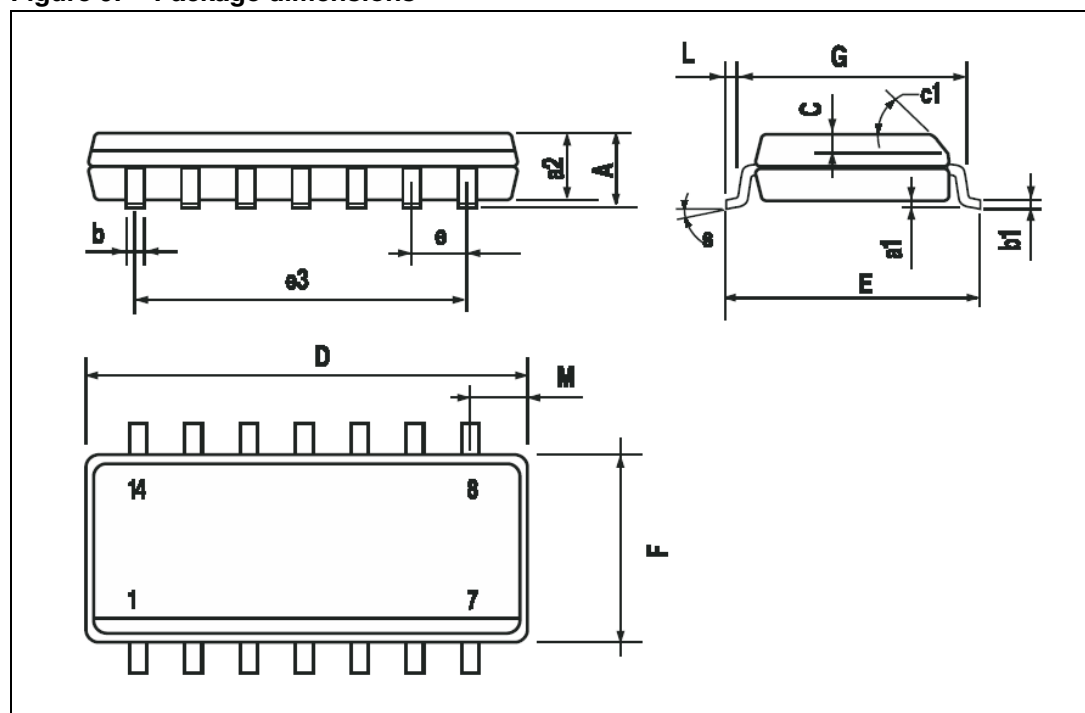
## 9 Package mechanical data

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a lead-free second level interconnect . The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: [www.st.com](http://www.st.com)

Table 6. SO-14 mechanical data

Dim.	mm			inch		
	Min	Typ	Max	Min	Typ	Max
A			1.75			0.069
a1	0.1		0.25	0.004		0.009
a2			1.6			0.063
b	0.35		0.46	0.014		0.018
b1	0.19		0.25	0.007		0.010
C		0.5			0.020	
c1	45° (typ.)					
D (1)	8.55		8.75	0.336		0.344
E	5.8		6.2	0.228		0.244
e		1.27			0.050	
e3		7.62			0.300	
F (1)	3.8		4	0.150		0.157
G	4.6		5.3	0.181		0.209
L	0.4		1.27	0.016		0.050
M			0.68			0.027
S	8° (max.)					

Figure 9. Package dimensions



## 10 Revision history

**Table 7. Document revision history**

<b>Date</b>	<b>Revision</b>	<b>Changes</b>
August 2001	3	First Issue in EDOCS dms
25-Feb-2008	4	Modified: Removed obsolete package DIP-14

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