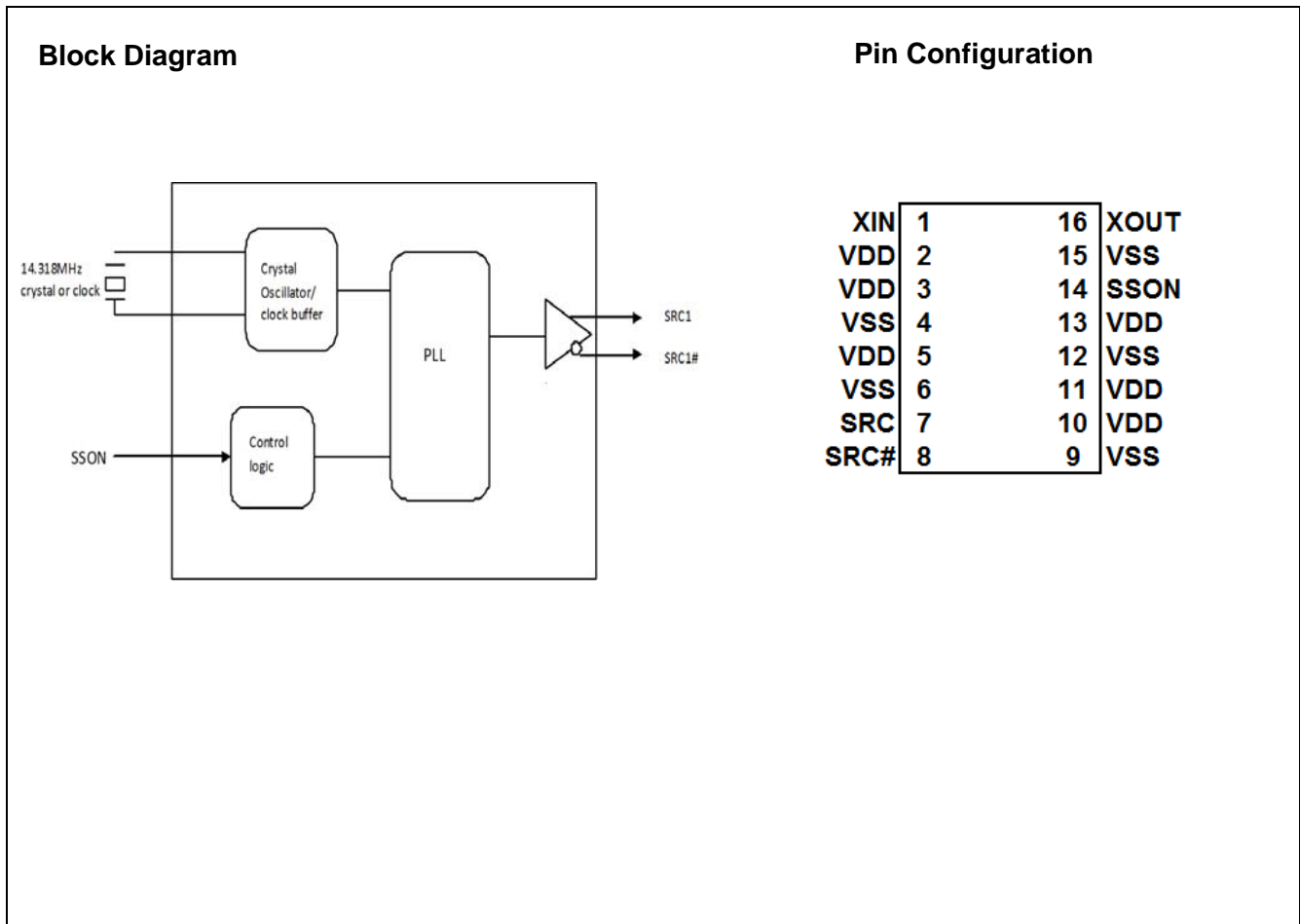


PCI Express Gen 2 & Gen 3 Clock Generator

Features

- Low power PCI Express Gen 2 & Gen 3 clock generator
- One 100-MHz differential SRC clocks
- Low power push-pull output buffers (no 50ohm to ground needed)
- Integrated 33ohm series termination resistors
- Low jitter (<50pS)
- SSON input for enabling spread spectrum clock
- Triangular Spread Spectrum profile for maximum electromagnetic interference (EMI) reduction
- Input frequency of 14.318MHz
- Industrial Temperature -40°C to 85°C
- 3.3V power supply
- 16-pin TSSOP package



Pin Definitions

Pin No.	Name	Type	Description
1	XIN	I	14.318 MHz Crystal input.
2	VDD	PWR	3.3V power supply
3	VDD	PWR	3.3V power supply
4	VSS	GND	Ground
5	VDD	PWR	3.3V power supply
6	VSS	GND	Ground
7	SRC1	O, DIF	100 MHz Differential serial reference clocks.
8	SRC1#	O, DIF	100 MHz Differential serial reference clocks.
9	VSS	GND	Ground
10	VDD	PWR	3.3V power supply
11	VDD	PWR	3.3V power supply
12	VSS	GND	Ground
13	VDD	PWR	3.3V power supply
14	SSON	I	3.3V LVTTTL input for enabling spread spectrum clock 0 = Disable, 1 = Enable (-0.5% SS) Extrenal 10K ohm pull-up or pull-down resistor required
15	VSS	GND	Ground
16	XOUT	O	14.318 MHz Crystal output.

Table 1. Crystal Recommendations

Frequency (Fund)	Cut	Loading	Load Cap	Drive (max.)	Shunt Cap (max.)	Motional (max.)	Tolerance (max.)	Stability (max.)	Aging (max.)
14.31818 MHz	AT	Parallel	20 pF	0.1 mW	5 pF	0.016 pF	35 ppm	30 ppm	5 ppm

The SL28SRC01 requires a Parallel Resonance Crystal. Substituting a series resonance crystal causes the SL28SRC01 to operate at the wrong frequency and violates the ppm specification. For most applications there is a 300-ppm frequency shift between series and parallel crystals due to incorrect loading.

Crystal Loading

Crystal loading plays a critical role in achieving low ppm performance. To realize low ppm performance, use the total capacitance the crystal sees to calculate the appropriate capacitive loading (CL).

Figure 1 shows a typical crystal configuration using the two trim capacitors. It is important that the trim capacitors are in series with the crystal. It is not true that load capacitors are in parallel with the crystal and are approximately equal to the load capacitance of the crystal.

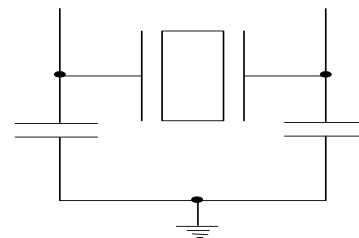


Figure 1. Crystal Capacitive Clarification

Calculating Load Capacitors

In addition to the standard external trim capacitors, consider the trace capacitance and pin capacitance to calculate the crystal loading correctly. Again, the capacitance on each side is in series with the crystal. The total capacitance on both side is twice the specified crystal load capacitance (CL). Trim

capacitors are calculated to provide equal capacitive loading on both sides.

Use the following formulas to calculate the trim capacitor values for Ce1 and Ce2 .

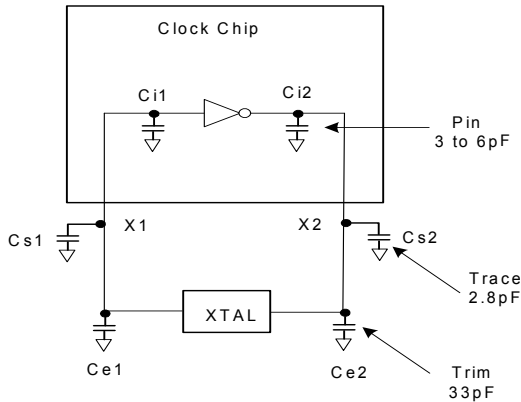


Figure 2. Crystal Loading Example

Load Capacitance (each side)

$$C_e = 2 * CL - (C_s + C_i)$$

Total Capacitance (as seen by the crystal)

$$CL_e = \frac{1}{\left(\frac{1}{C_{e1} + C_{s1} + C_{i1}} + \frac{1}{C_{e2} + C_{s2} + C_{i2}} \right)}$$

- CL.....Crystal load capacitance
- CLe..... Actual loading seen by crystal using standard value trim capacitors
- Ce..... External trim capacitors
- Cs..... Stray capacitance (terraced)
- Ci Internal capacitance (lead frame, bond wires, etc.)

Absolute Maximum Conditions

Parameter	Description	Condition	Min.	Max.	Unit
V _{DD}	Core Supply Voltage		–	4.6	V
V _{IN}	Input Voltage	Relative to V _{SS}	–0.5	4.6	V _{DC}
T _S	Temperature, Storage	Non-functional	–65	150	°C
T _{A (commercial)}	Temperature, Operating Ambient, Commercial	Functional	0	85	°C
T _{A (industrial)}	Temperature, Operating Ambient, Industrial	Functional	–40	85	°C
T _J	Temperature, Junction	Functional	–	150	°C
∅ _{JC}	Dissipation, Junction to Case	JEDEC (JESD 51)	–	20	°C/W
∅ _{JA}	Dissipation, Junction to Ambient	JEDEC (JESD 51)	–	60	°C/W
ESD _{HBM}	ESD Protection (Human Body Model)	JEDEC (JESD 22 - A114)	2000	–	V
UL-94	Flammability Rating	UL (Class)	V-0		

DC Electrical Specifications

Parameter	Description	Condition	Min.	Max.	Unit
V _{DD}	3.3V Operating Voltage	3.3 ± 5%	3.135	3.465	V
V _{IH}	3.3V Input High Voltage		2.0	V _{DD} + 0.3	V
V _{IL}	3.3V Input Low Voltage		V _{SS} – 0.3	0.8	V
I _{IH}	Input High Leakage Current	Except internal pull-down resistors, 0 < V _{IN} < V _{DD}	–	5	µA
I _{IL}	Input Low Leakage Current	Except internal pull-up resistors, 0 < V _{IN} < V _{DD}	–5	–	µA
V _{OH}	3.3V Output High Voltage	I _{OH} = –1 mA	2.4	–	V
V _{OL}	3.3V Output Low Voltage	I _{OL} = 1 mA	–	0.4	V
I _{OZ}	High-impedance Output Current		–10	10	µA



DC Electrical Specifications

Parameter	Description	Condition	Min.	Max.	Unit
C _{IN}	Input Pin Capacitance		1.5	5	pF
C _{OUT}	Output Pin Capacitance			6	pF
L _{IN}	Pin Inductance		–	7	nH
V _{XIH}	Xin High Voltage		0.7V _{DD}	V _{DD}	V
V _{XIL}	Xin Low Voltage		0	0.3V _{DD}	V
I _{DD3.3V}	Dynamic Supply Current		–	40	mA

AC Electrical Specifications

Parameter	Description	Condition	Min.	Max.	Unit
Crystal					
T _{DC}	XIN Duty Cycle	The device operates reliably with input duty cycles up to 30/70 but the REF clock duty cycle will not be within specification	47.5	52.5	%
T _{PERIOD}	XIN Period	When XIN is driven from an external clock source	69.841	71.0	ns
T _R /T _F	XIN Rise and Fall Times	Measured between 0.3V _{DD} and 0.7V _{DD}	–	10.0	ns
T _{CCJ}	XIN Cycle to Cycle Jitter	As an average over 1- μ s duration	–	500	ps
L _{ACC}	Long-term Accuracy	Measured at VDD/2 differential	–	250	ppm
Clock Input					
T _{DC}	CLKIN Duty Cycle	Measured at VDD/2	47	53	%
T _R /T _F	CLKIN Rise and Fall Times	Measured between 0.2V _{DD} and 0.8V _{DD}	0.5	4.0	V/ns
T _{CCJ}	CLKIN Cycle to Cycle Jitter	Measured at VDD/2	–	250	ps
T _{LTJ}	CLKIN Long Term Jitter	Measured at VDD/2	–	350	ps
V _{IL}	Input Low Voltage	XIN / CLKIN pin	–	0.8	V
V _{IH}	Input High Voltage	XIN / CLKIN pin	2	VDD+0.3	V
I _{IL}	Input Low Current	XIN / CLKIN pin, 0 < V _{IN} < 0.8	–	20	μ A
I _{IH}	Input High Current	XIN / CLKIN pin, V _{IN} = VDD	–	35	μ A
SRC					
T _{DC}	SRC Duty Cycle	Measured at 0V differential	45	55	%
T _{PERIOD}	100 MHz SRC Period	Measured at 0V differential at 0.1s	9.99900	10.0010	ns
T _{PERIODSS}	100 MHz SRC Period, SSC	Measured at 0V differential at 0.1s	10.02406	10.02607	ns
T _{PERIODAbs}	100 MHz SRC Absolute Period	Measured at 0V differential at 1 clock	9.87400	10.1260	ns
T _{PERIODSSAbs}	100 MHz SRC Absolute Period, SSC	Measured at 0V differential at 1 clock	9.87406	10.1762	ns
T _{CCJ}	SRC Cycle to Cycle Jitter	Measured at 0V differential	–	50	ps
RMS _{GEN1}	Output PCIe* Gen1 REFCLK phase jitter	BER = 1E-12 (including PLL BW 8 - 16 MHz, ζ = 0.54, Td=10 ns, Ftrk=1.5 MHz)	0	108	ps
RMS _{GEN2}	Output PCIe* Gen2 REFCLK phase jitter	Includes PLL BW 8 - 16 MHz, Jitter Peaking = 3dB, ζ = 0.54, Td=10 ns), Low Band, F < 1.5MHz	0	3.0	ps
RMS _{GEN2}	Output PCIe* Gen2 REFCLK phase jitter	Includes PLL BW 8 - 16 MHz, Jitter Peaking = 3dB, ζ = 0.54, Td=10 ns), Low Band, F < 1.5MHz	0	3.1	ps
RMS _{GEN3}	Output phase jitter impact – PCIe* Gen3	Includes PLL BW 2 - 4 MHz, CDR = 10MHz)	0	1.0	ps
L _{ACC}	SRC Long Term Accuracy	Measured at 0V differential	–	100	ppm
T _R / T _F	SRC Rising/Falling Slew Rate	Measured differentially from \pm 150 mV	2.5	8	V/ns
T _{RFM}	Rise/Fall Matching	Measured single-endedly from \pm 75 mV	–	20	%
V _{HIGH}	Voltage High			1.15	V
V _{LOW}	Voltage Low		–0.3	–	V
V _{OX}	Crossing Point Voltage at 0.7V Swing		300	550	mV

AC Electrical Specifications

Parameter	Description	Condition	Min.	Max.	Unit
T _{jphasepll}	Phase Jitter (PLL BW 8-16MHz, 5-16MHz)	RMS value		3.1	pS
ENABLE/DISABLE and SET-UP					
T _{STABLE}	Clock Stabilization from Power-up		–	1.8	ms
T _{SS}	Stopclock Set-up Time		10.0	–	ns

Test and Measurement Set-up

For SRC Signals

This diagram shows the test load configuration for the differential SRC outputs

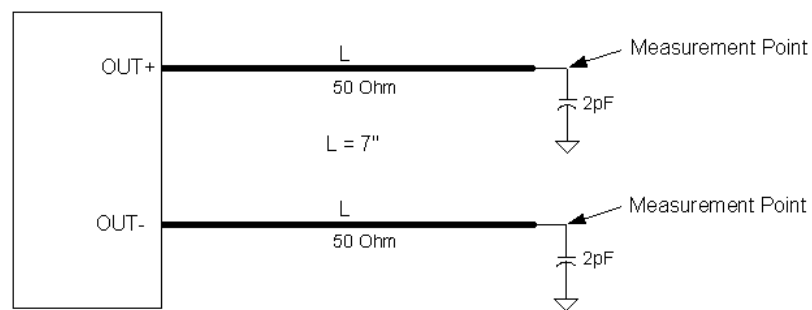


Figure 3. 0.7V Differential Load Configuration

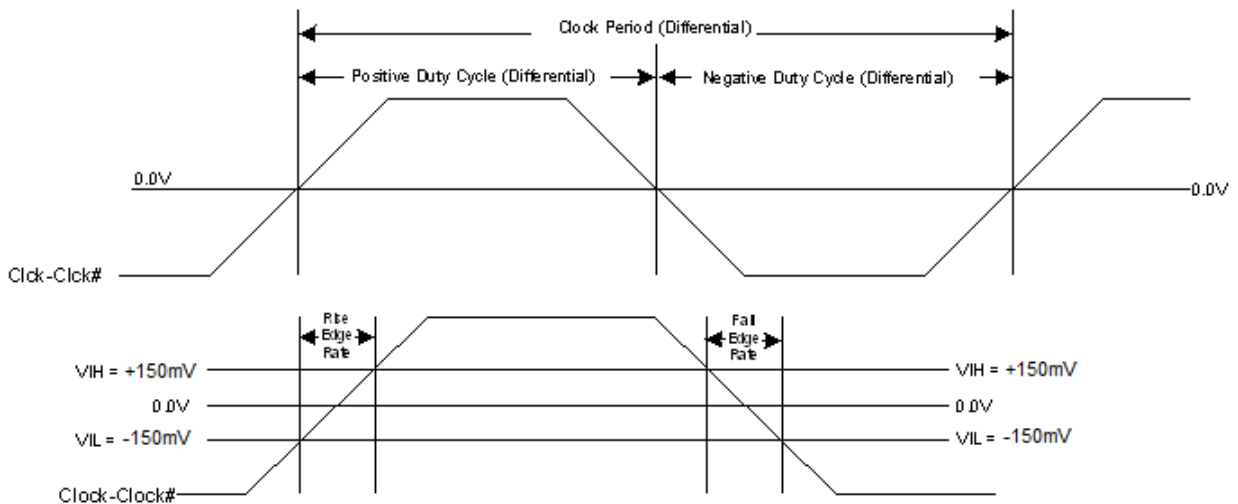


Figure 4. Differential Measurement for Differential Output Signals (for AC Parameters Measurement)

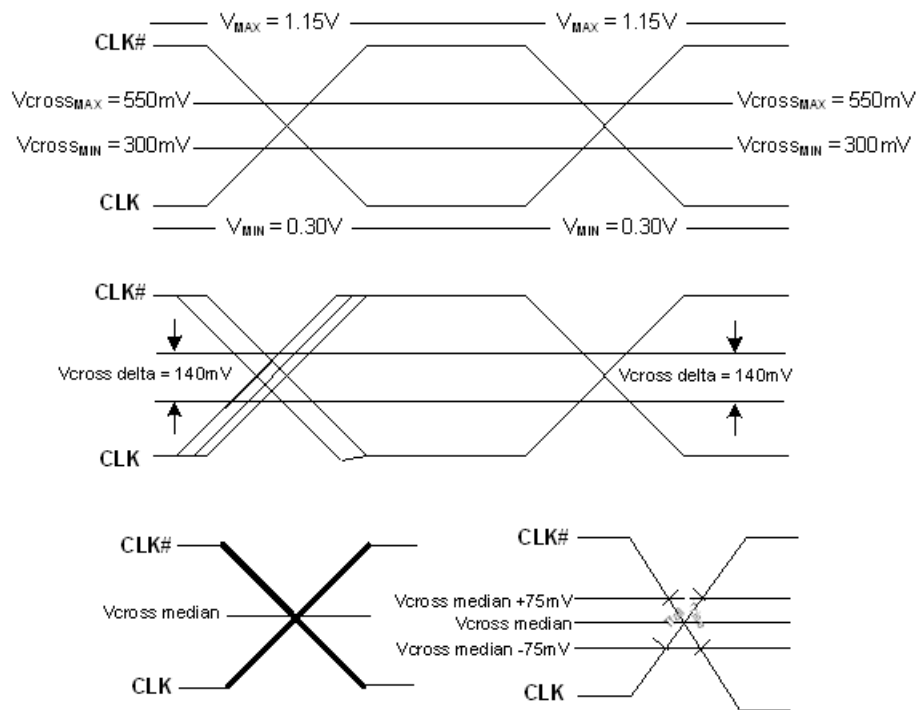
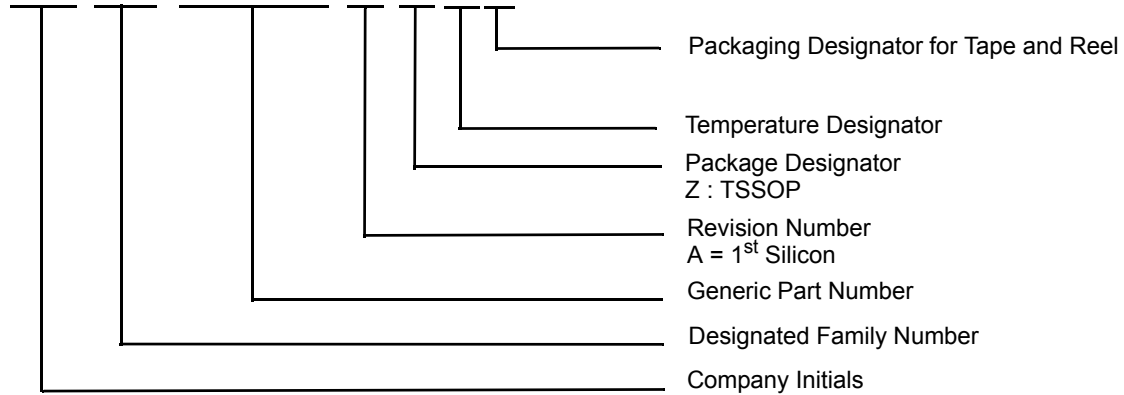


Figure 5. Single-ended Measurement for Differential Output Signals (for AC Parameters Measurement)

Ordering Information

Part Number	Package Type	Product Flow
Lead-free		
SL28SRC01BZI	16-pin TSSOP	Industrial, -40° to 85°C
SL28SRC01BZIT	16-pin TSSOP–Tape and Reel	Industrial, -40° to 85°C

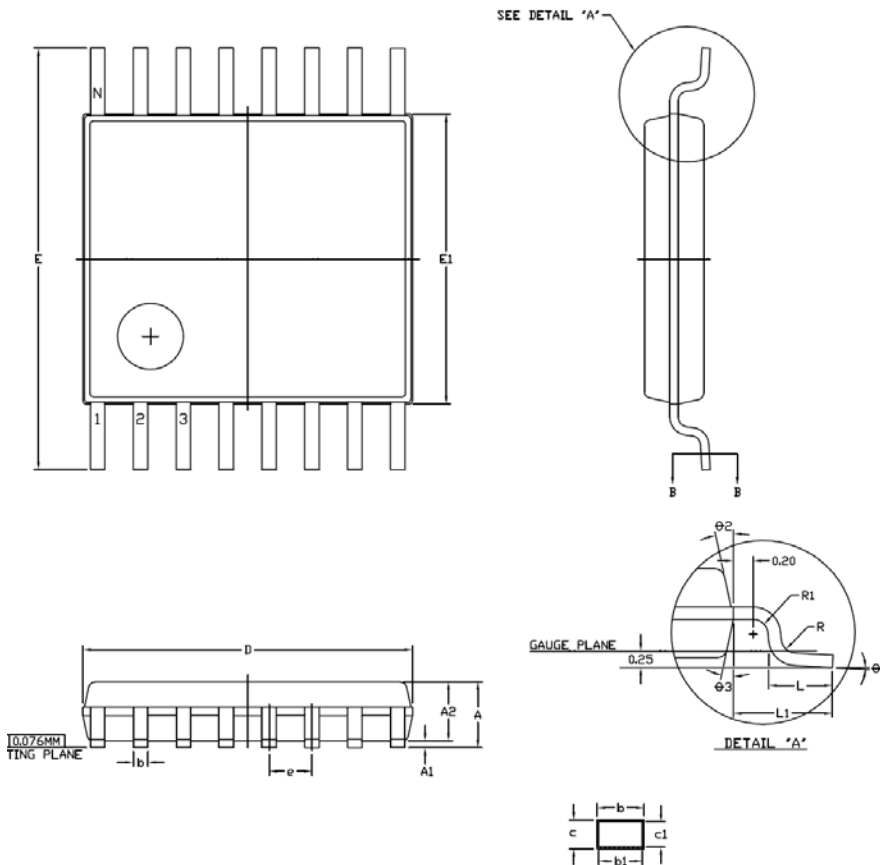
SL 28 SRC01 B Z I T



This device is Pb free and RoHS compliant

Package Diagrams

16-pin TSSOP



NOTES:

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. DIMENSION 'D' DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.15 PER SIDE.
3. DIMENSION 'E1' DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION, INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 PER SIDE.
4. 'N' IS THE NUMBER OF TERMINAL POSITIONS.
5. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
6. REFERENCE DRAWING JEDEC MO-153, VARIATION AB.

SYMBOL	DIMENSION IN MM			DIMENSION IN INCH		
	MIN.	NDM.	MAX.	MIN.	NDM.	MAX.
A			1.20			.047
A1	0.05		0.15	.002		.006
A2	0.80	0.90	1.05	.031	.035	.041
b	0.19		0.30	.007		.012
b1	0.19	0.22	0.25	.007	.009	.010
c	0.09		0.20	.004		.008
c1	0.09		0.16	.004		.006
D	4.90	5.00	5.10	.193	.197	.200
e	0.65 BSC.			.026 BSC.		
E	6.40 BSC.			.252 BSC.		
E1	4.30	4.40	4.50	.169	.173	.177
L	0.50	0.60	0.75	.020	.024	.030
L1	1.00 REF.			.039 REF.		
R	0.09			.004		
R1	0.09			.004		
$\theta 1$	0		8	0		8
$\theta 2$	12 REF.			12 REF.		
$\theta 3$	12 REF.			12 REF.		



Document History Page

Document Title: SL28SRC01 PCI Express Gen 2 & Gen 3 Clock Generator				
REV.	ECR#	Issue Date	Orig. of Change	Description of Change
1.0		09/13/09	JMA	New datasheet
1.1		11/06/09	JMA	Updated Figure 4
AA	1454	04/25/10	JMA	1. Updated pin 6 definition on page 2 2. Updated revision to be ISO compliant 3. Updated package information 4. Added commercial temperature grade 5. Added clock in features



ClockBuilder Pro

One-click access to Timing tools, documentation, software, source code libraries & more. Available for Windows and iOS (CBGo only).

www.silabs.com/CBPro



Timing Portfolio
www.silabs.com/timing



SW/HW
www.silabs.com/CBPro



Quality
www.silabs.com/quality



Support and Community
community.silabs.com

Disclaimer

Silicon Laboratories intends to provide customers with the latest, accurate, and in-depth documentation of all peripherals and modules available for system and software implementers using or intending to use the Silicon Laboratories products. Characterization data, available modules and peripherals, memory sizes and memory addresses refer to each specific device, and "Typical" parameters provided can and do vary in different applications. Application examples described herein are for illustrative purposes only. Silicon Laboratories reserves the right to make changes without further notice and limitation to product information, specifications, and descriptions herein, and does not give warranties as to the accuracy or completeness of the included information. Silicon Laboratories shall have no liability for the consequences of use of the information supplied herein. This document does not imply or express copyright licenses granted hereunder to design or fabricate any integrated circuits. The products are not designed or authorized to be used within any Life Support System without the specific written consent of Silicon Laboratories. A "Life Support System" is any product or system intended to support or sustain life and/or health, which, if it fails, can be reasonably expected to result in significant personal injury or death. Silicon Laboratories products are not designed or authorized for military applications. Silicon Laboratories products shall under no circumstances be used in weapons of mass destruction including (but not limited to) nuclear, biological or chemical weapons, or missiles capable of delivering such weapons.

Trademark Information

Silicon Laboratories Inc.®, Silicon Laboratories®, Silicon Labs®, SiLabs® and the Silicon Labs logo®, Bluegiga®, Bluegiga Logo®, Clockbuilder®, CMEMS®, DSPLL®, EFM®, EFM32®, EFR®, Ember®, Energy Micro, Energy Micro logo and combinations thereof, "the world's most energy friendly microcontrollers", Ember®, EZLink®, EZRadio®, EZRadioPRO®, Gecko®, ISOModem®, Precision32®, ProSLIC®, Simplicity Studio®, SiPHY®, Telegesis, the Telegesis Logo®, USBXpress® and others are trademarks or registered trademarks of Silicon Laboratories Inc. ARM, CORTEX, Cortex-M3 and THUMB are trademarks or registered trademarks of ARM Holdings. Keil is a registered trademark of ARM Limited. All other products or brand names mentioned herein are trademarks of their respective holders.



Silicon Laboratories Inc.
400 West Cesar Chavez
Austin, TX 78701
USA

<http://www.silabs.com>