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# R1LV1616H-I Series

Wide Temperature Range Version

16 M SRAM (1-Mword  $\times$  16-bit / 2-Mword  $\times$  8-bit)

REJ03C0195-0101

Rev.1.01

Nov.18.2004

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## Description

The R1LV1616H-I Series is 16-Mbit static RAM organized 1-Mword  $\times$  16-bit / 2-Mword  $\times$  8-bit. R1LV1616H-I Series has realized higher density, higher performance and low power consumption by employing CMOS process technology (6-transistor memory cell). It offers low power standby power dissipation; therefore, it is suitable for battery backup systems. It is packaged in 48-pin plastic TSOPI for high density surface mounting.

## Features

- Single 3.0 V supply: 2.7 V to 3.6 V
- Fast access time: 45/55 ns (max)
- Power dissipation:
  - Active: 9 mW/MHz (typ)
  - Standby: 1.5  $\mu$ W (typ)
- Completely static memory.
  - No clock or timing strobe required
- Equal access and cycle times
- Common data input and output.
  - Three state output
- Battery backup operation.
  - 2 chip selection for battery backup
- Temperature range:  $-40$  to  $+85^{\circ}\text{C}$
- Byte function ( $\times 8$  mode) available by BYTE# & A-1.

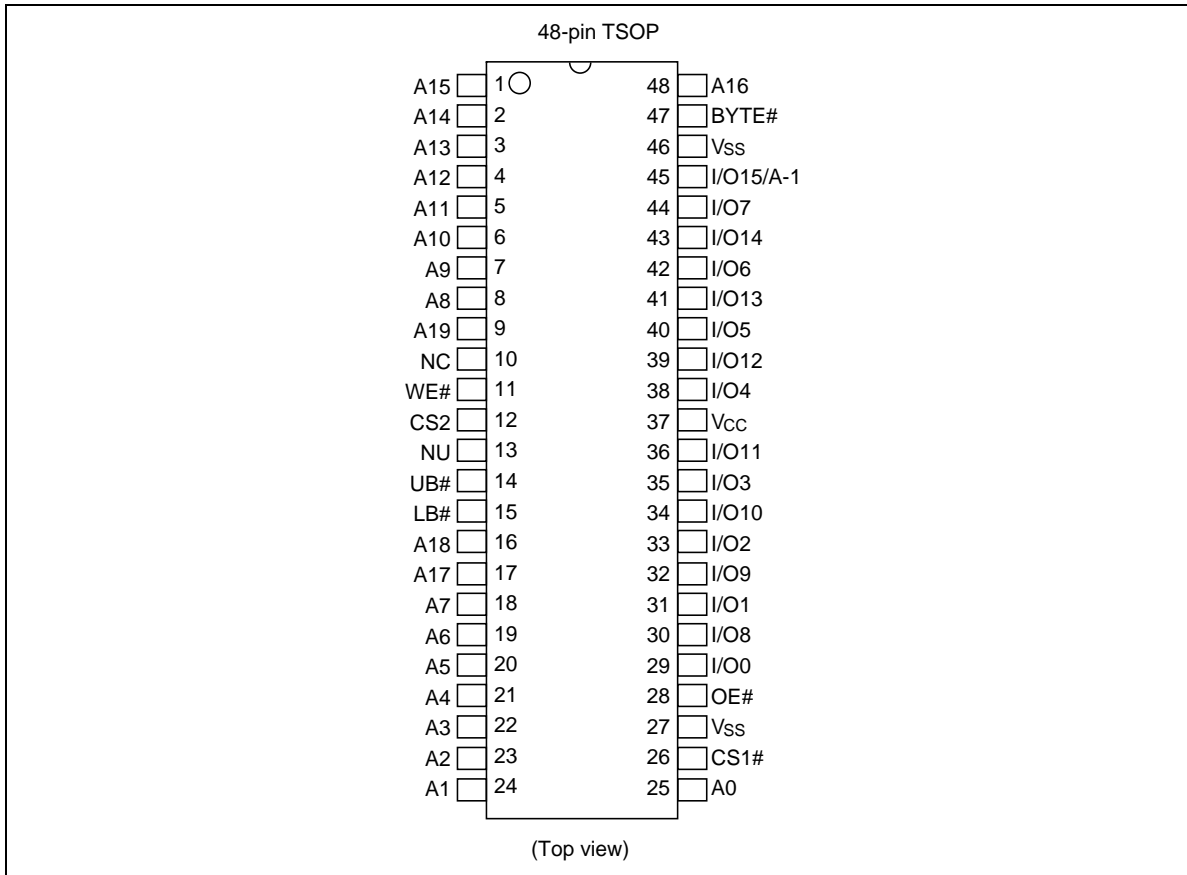
## R1LV1616H-I Series

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### Ordering Information

Type No.	Access time	Package
R1LV1616HSA-4LI	45 ns	48-pin plastic TSOPI (48P3R-B)
R1LV1616HSA-4SI	45 ns	
R1LV1616HSA-5SI	55 ns	

Pin Arrangement

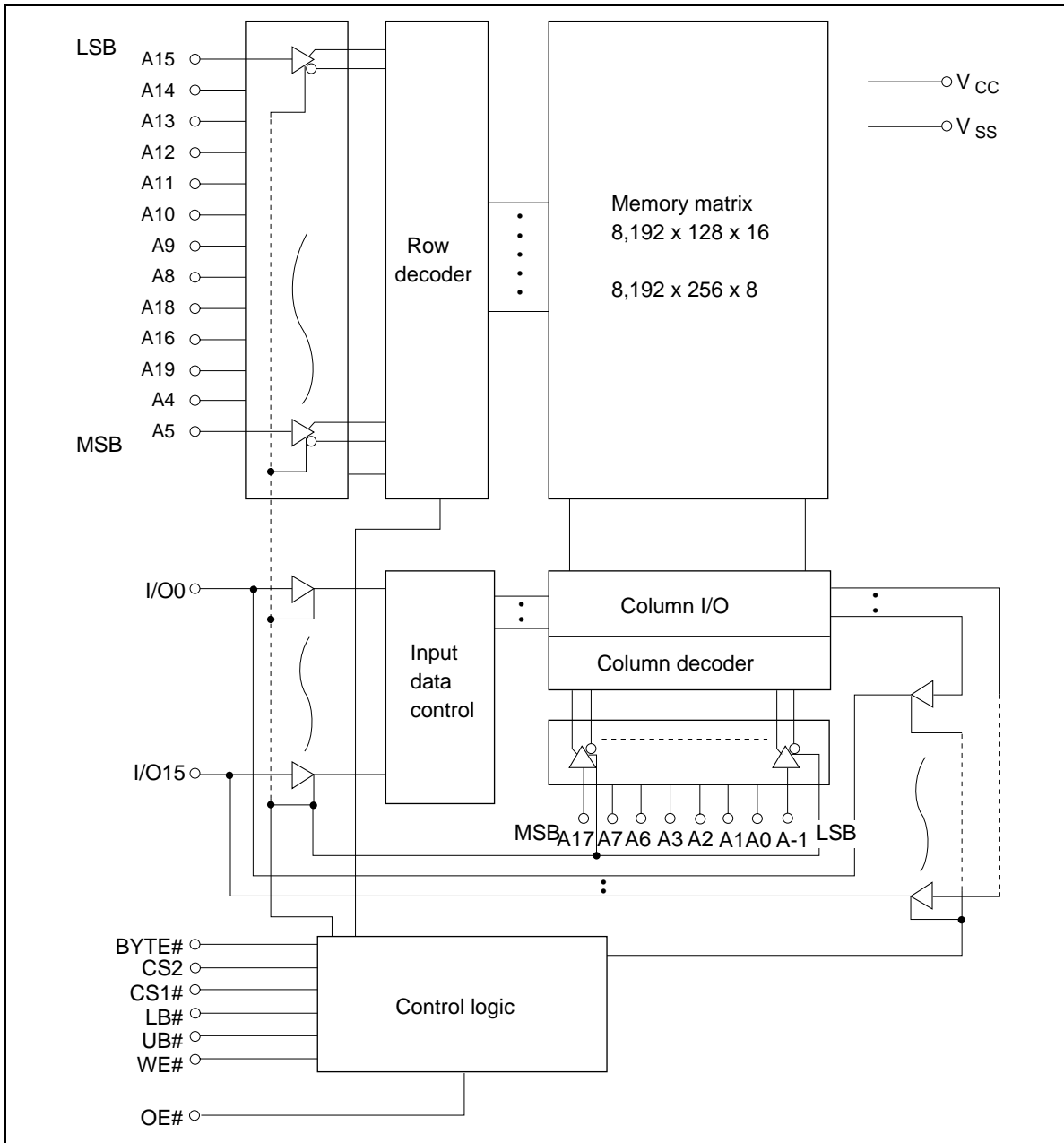


**Pin Description (TSOP)**

<b>Pin name</b>	<b>Function</b>
A0 to A19	Address input (word mode)
A-1 to A19	Address input (byte mode)
I/O0 to I/O15	Data input/output
CS1# ( $\overline{\text{CS1}}$ )	Chip select 1
CS2	Chip select 2
WE# ( $\overline{\text{WE}}$ )	Write enable
OE# ( $\overline{\text{OE}}$ )	Output enable
LB# ( $\overline{\text{LB}}$ )	Lower byte select
UB# ( $\overline{\text{UB}}$ )	Upper byte select
BYTE# ( $\overline{\text{BYTE}}$ )	Byte enable
V <sub>CC</sub>	Power supply
V <sub>SS</sub>	Ground
NC	No connection
NU* <sup>1</sup>	Not used (test mode pin)

Note: 1. This pin should be connected to a ground (V<sub>SS</sub>), or not be connected (open).

Block Diagram (TSOP)



## Operation Table (TSOP)

### Byte mode

CS1#	CS2	WE#	OE#	UB#	LB#	BYTE#	I/O0 to I/O7	I/O8 to I/O14	I/O15	Operation
H	x	x	x	x	x	L	High-Z	High-Z	High-Z	Standby
x	L	x	x	x	x	L	High-Z	High-Z	High-Z	Standby
L	H	H	L	x	x	L	Dout	High-Z	A-1	Read
L	H	L	x	x	x	L	Din	High-Z	A-1	Write
L	H	H	H	x	x	L	High-Z	High-Z	High-Z	Output disable

Note: H:  $V_{IH}$ , L:  $V_{IL}$ , x:  $V_{IH}$  or  $V_{IL}$

### Word mode

CS1#	CS2	WE#	OE#	UB#	LB#	BYTE#	I/O0 to I/O7	I/O8 to I/O14	I/O15	Operation
H	x	x	x	x	x	H	High-Z	High-Z	High-Z	Standby
x	L	x	x	x	x	H	High-Z	High-Z	High-Z	Standby
x	x	x	x	H	H	H	High-Z	High-Z	High-Z	Standby
L	H	H	L	L	L	H	Dout	Dout	Dout	Read
L	H	H	L	H	L	H	Dout	High-Z	High-Z	Lower byte read
L	H	H	L	L	H	H	High-Z	Dout	Dout	Upper byte read
L	H	L	x	L	L	H	Din	Din	Din	Write
L	H	L	x	H	L	H	Din	High-Z	High-Z	Lower byte write
L	H	L	x	L	H	H	High-Z	Din	Din	Upper byte write
L	H	H	H	x	x	H	High-Z	High-Z	High-Z	Output disable

Note: H:  $V_{IH}$ , L:  $V_{IL}$ , x:  $V_{IH}$  or  $V_{IL}$

**Absolute Maximum Ratings**

Parameter	Symbol	Value	Unit
Power supply voltage relative to $V_{SS}$	$V_{CC}$	-0.5 to +4.6	V
Terminal voltage on any pin relative to $V_{SS}$	$V_T$	-0.5* <sup>1</sup> to $V_{CC} + 0.3$ * <sup>2</sup>	V
Power dissipation	$P_T$	1.0	W
Storage temperature range	Tstg	-55 to +125	°C
Storage temperature range under bias	Tbias	-40 to +85	°C

Notes: 1.  $V_T$  min: -2.0 V for pulse half-width  $\leq 10$  ns.  
2. Maximum voltage is +4.6 V.

**DC Operating Conditions**

Parameter	Symbol	Min	Typ	Max	Unit	Note
Supply voltage	$V_{CC}$	2.7	3.0	3.6	V	
	$V_{SS}$	0	0	0	V	
Input high voltage	$V_{IH}$	2.2	—	$V_{CC} + 0.3$	V	
Input low voltage	$V_{IL}$	-0.3	—	0.6	V	1
Ambient temperature range	Ta	-40	—	+85	°C	

Note: 1.  $V_{IL}$  min: -2.0 V for pulse half-width  $\leq 10$  ns.

**DC Characteristics**

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions*2	
Input leakage current	$ I_{LI} $	—	—	1	$\mu\text{A}$	$V_{in} = V_{SS}$ to $V_{CC}$	
Output leakage current	$ I_{LO} $	—	—	1	$\mu\text{A}$	CS1# = $V_{IH}$ or CS2 = $V_{IL}$ or OE# = $V_{IH}$ or WE# = $V_{IL}$ or LB# = UB# = $V_{IH}$ , $V_{I/O} = V_{SS}$ to $V_{CC}$	
Operating current	$I_{CC}$	—	—	20	mA	CS1# = $V_{IL}$ , CS2 = $V_{IH}$ , Others = $V_{IH}/V_{IL}$ , $I_{I/O} = 0$ mA	
Average operating current	$I_{CC1}$ (READ)	—	22*1	35	mA	Min. cycle, duty = 100%, $I_{I/O} = 0$ mA, CS1# = $V_{IL}$ , CS2 = $V_{IH}$ , WE# = $V_{IH}$ , Others = $V_{IH}/V_{IL}$	
	$I_{CC1}$	—	30*1	50	mA	Min. cycle, duty = 100%, $I_{I/O} = 0$ mA, CS1# = $V_{IL}$ , CS2 = $V_{IH}$ , Others = $V_{IH}/V_{IL}$	
	$I_{CC2}$ *3 (READ)	—	3*1	8	mA	Cycle time = 70 ns, duty = 100%, $I_{I/O} = 0$ mA, CS1# = $V_{IL}$ , CS2 = $V_{IH}$ , WE# = $V_{IH}$ , Others = $V_{IH}/V_{IL}$ Address increment scan or decrement scan	
	$I_{CC2}$ *3	—	20*1	30	mA	Cycle time = 70 ns, duty = 100%, $I_{I/O} = 0$ mA, CS1# = $V_{IL}$ , CS2 = $V_{IH}$ , Others = $V_{IH}/V_{IL}$ Address increment scan or decrement scan	
	$I_{CC3}$	—	3*1	8	mA	Cycle time = 1 $\mu\text{s}$ , duty = 100%, $I_{I/O} = 0$ mA, CS1# $\leq 0.2$ V, CS2 $\geq V_{CC} - 0.2$ V $V_{IH} \geq V_{CC} - 0.2$ V, $V_{IL} \leq 0.2$ V	
Standby current	$I_{SB}$	—	0.1*1	0.5	mA	CS2 = $V_{IL}$	
Standby current	-4SI -5SI	$I_{SB1}$	—	0.5*1	8	$\mu\text{A}$	$0 \text{ V} \leq V_{in}$ (1) $0 \text{ V} \leq \text{CS2} \leq 0.2 \text{ V}$ or (2) CS1# $\geq V_{CC} - 0.2 \text{ V}$ , CS2 $\geq V_{CC} - 0.2 \text{ V}$ or (3) LB# = UB# $\geq V_{CC} - 0.2 \text{ V}$ , CS2 $\geq V_{CC} - 0.2 \text{ V}$ , CS1# $\leq 0.2 \text{ V}$ Average value
	-4LI	$I_{SB1}$	—	0.5*1	25	$\mu\text{A}$	
Output high voltage	$V_{OH}$	2.4	—	—	V	$I_{OH} = -1$ mA	
	$V_{OH}$	$V_{CC} - 0.2$	—	—	V	$I_{OH} = -100$ $\mu\text{A}$	
Output low voltage	$V_{OL}$	—	—	0.4	V	$I_{OL} = 2$ mA	
	$V_{OL}$	—	—	0.2	V	$I_{OL} = 100$ $\mu\text{A}$	



## R1LV1616H-I Series

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- Notes: 1. Typical values are at  $V_{CC} = 3.0\text{ V}$ ,  $T_a = +25^\circ\text{C}$  and not guaranteed.  
2.  $\text{BYTE}\# \geq V_{CC} - 0.2\text{ V}$  or  $\text{BYTE}\# \leq 0.2\text{ V}$   
3.  $I_{CC2}$  is the value measured while the valid address is increasing or decreasing by one bit.  
Word mode: LSB (least significant bit) is A0.  
Byte mode: LSB (least significant bit) is A-1.

## Capacitance

( $T_a = +25^\circ\text{C}$ ,  $f = 1.0\text{ MHz}$ )

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions	Note
Input capacitance	$C_{in}$	—	—	8	pF	$V_{in} = 0\text{ V}$	1
Input/output capacitance	$C_{I/O}$	—	—	10	pF	$V_{I/O} = 0\text{ V}$	1

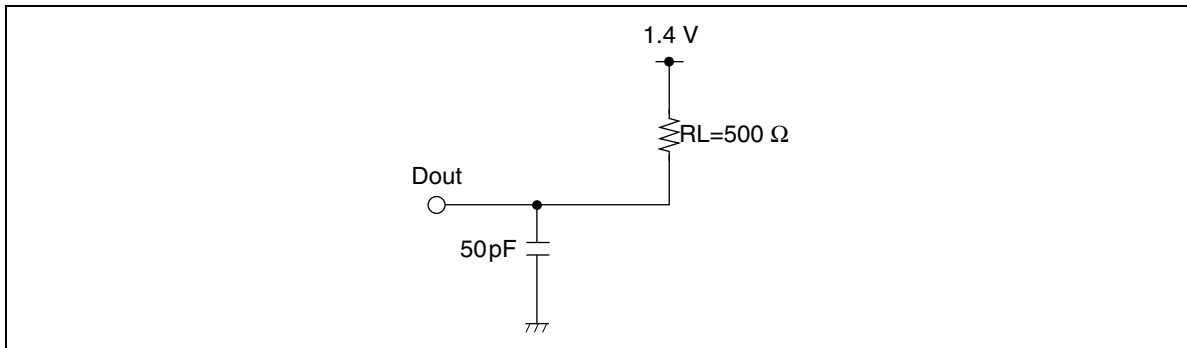
Note: 1. This parameter is sampled and not 100% tested.

## AC Characteristics

( $T_a = -40$  to  $+85^\circ\text{C}$ ,  $V_{CC} = 2.7$  V to  $3.6$  V, unless otherwise noted.)

### Test Conditions

- Input pulse levels:  $V_{IL} = 0.4$  V,  $V_{IH} = 2.4$  V
- Input rise and fall time: 5 ns
- Input and output timing reference levels: 1.4 V
- Output load: See figures (Including scope and jig)



## R1LV1616H-I Series

### Read Cycle

Parameter	Symbol	R1LV1616H-I				Unit	Notes
		-4SI, -4LI		-5SI			
		Min	Max	Min	Max		
Read cycle time	$t_{RC}$	45	—	55	—	ns	
Address access time	$t_{AA}$	—	45	—	55	ns	
Chip select access time	$t_{ACS1}$	—	45	—	55	ns	
	$t_{ACS2}$	—	45	—	55	ns	
Output enable to output valid	$t_{OE}$	—	30	—	35	ns	
Output hold from address change	$t_{OH}$	10	—	10	—	ns	
LB#, UB# access time	$t_{BA}$	—	45	—	55	ns	
Chip select to output in low-Z	$t_{CLZ1}$	10	—	10	—	ns	2, 3
	$t_{CLZ2}$	10	—	10	—	ns	2, 3
LB#, UB# enable to low-Z	$t_{BLZ}$	5	—	5	—	ns	2, 3
Output enable to output in low-Z	$t_{OLZ}$	5	—	5	—	ns	2, 3
Chip deselect to output in high-Z	$t_{CHZ1}$	0	20	0	20	ns	1, 2, 3
	$t_{CHZ2}$	0	20	0	20	ns	1, 2, 3
LB#, UB# disable to high-Z	$t_{BHZ}$	0	15	0	20	ns	1, 2, 3
Output disable to output in high-Z	$t_{OHZ}$	0	15	0	20	ns	1, 2, 3

### Write Cycle

Parameter	Symbol	R1LV1616H-I				Unit	Notes
		-4SI, -4LI		-5SI			
		Min	Max	Min	Max		
Write cycle time	$t_{WC}$	45	—	55	—	ns	
Address valid to end of write	$t_{AW}$	45	—	50	—	ns	
Chip selection to end of write	$t_{CW}$	45	—	50	—	ns	5
Write pulse width	$t_{WP}$	35	—	40	—	ns	4
LB#, UB# valid to end of write	$t_{BW}$	45	—	50	—	ns	
Address setup time	$t_{AS}$	0	—	0	—	ns	6
Write recovery time	$t_{WR}$	0	—	0	—	ns	7
Data to write time overlap	$t_{DW}$	25	—	25	—	ns	
Data hold from write time	$t_{DH}$	0	—	0	—	ns	
Output active from end of write	$t_{OW}$	5	—	5	—	ns	2
Output disable to output in high-Z	$t_{OHZ}$	0	15	0	20	ns	1, 2
Write to output in high-Z	$t_{WHZ}$	0	15	0	20	ns	1, 2

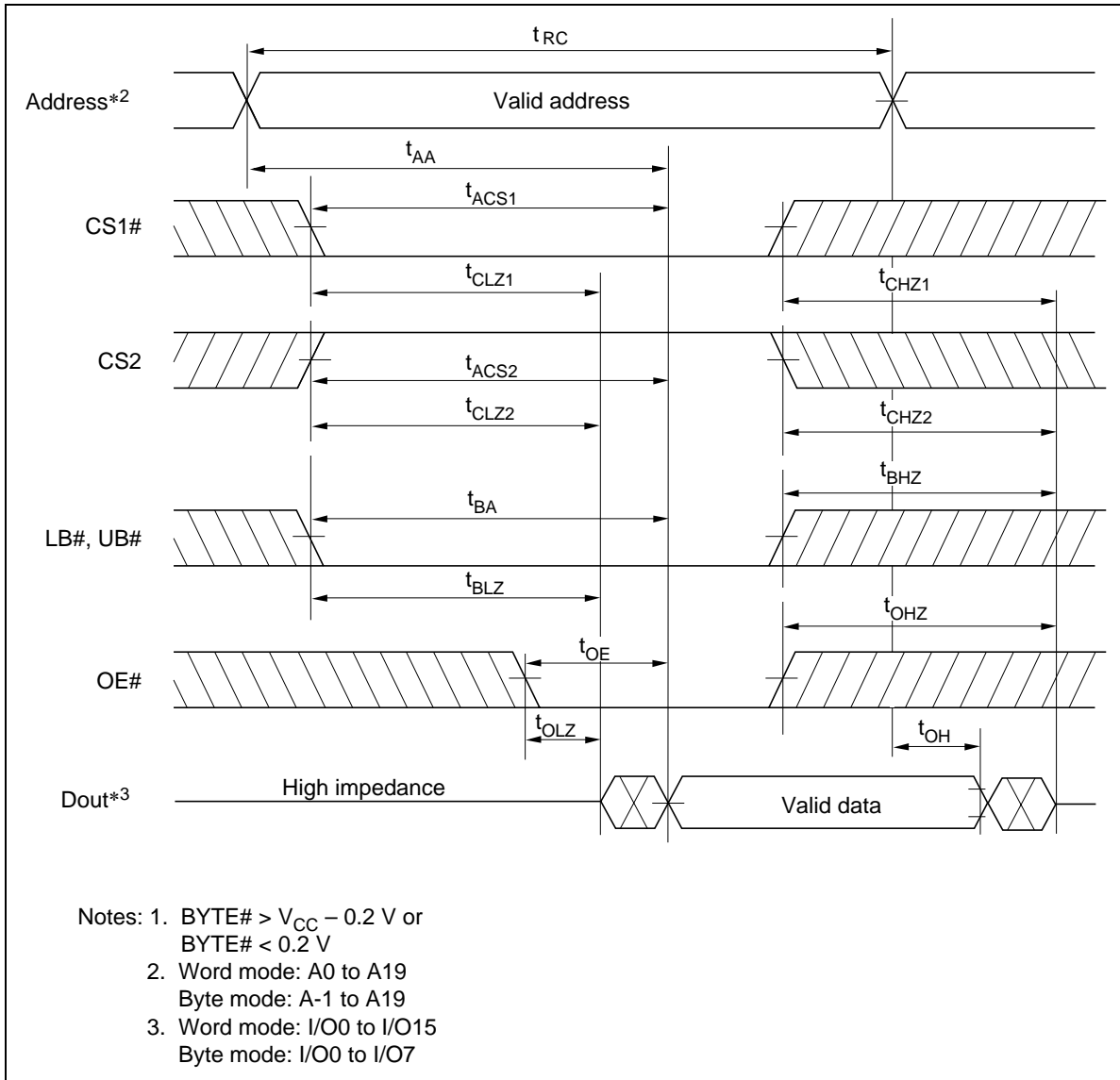
**Byte Control**

Parameter	Symbol	R1LV1616H-I				Unit	Notes
		-4SI, -4LI		-5SI			
		Min	Max	Min	Max		
BYTE# setup time	$t_{BS}$	5	—	5	—	ms	
BYTE# recovery time	$t_{BR}$	5	—	5	—	ms	

- Notes:
1.  $t_{CHZ}$ ,  $t_{OHZ}$ ,  $t_{WHZ}$  and  $t_{BHZ}$  are defined as the time at which the outputs achieve the open circuit conditions and are not referred to output voltage levels.
  2. This parameter is sampled and not 100% tested.
  3. At any given temperature and voltage condition,  $t_{HZ}$  max is less than  $t_{LZ}$  min both for a given device and from device to device.
  4. A write occurs during the overlap of a low CS1#, a high CS2, a low WE# and a low LB# or a low UB#. A write begins at the latest transition among CS1# going low, CS2 going high, WE# going low and LB# going low or UB# going low. A write ends at the earliest transition among CS1# going high, CS2 going low, WE# going high and LB# going high or UB# going high.  $t_{WP}$  is measured from the beginning of write to the end of write.
  5.  $t_{CW}$  is measured from the later of CS1# going low or CS2 going high to the end of write.
  6.  $t_{AS}$  is measured from the address valid to the beginning of write.
  7.  $t_{WR}$  is measured from the earliest of CS1# or WE# going high or CS2 going low to the end of write cycle.

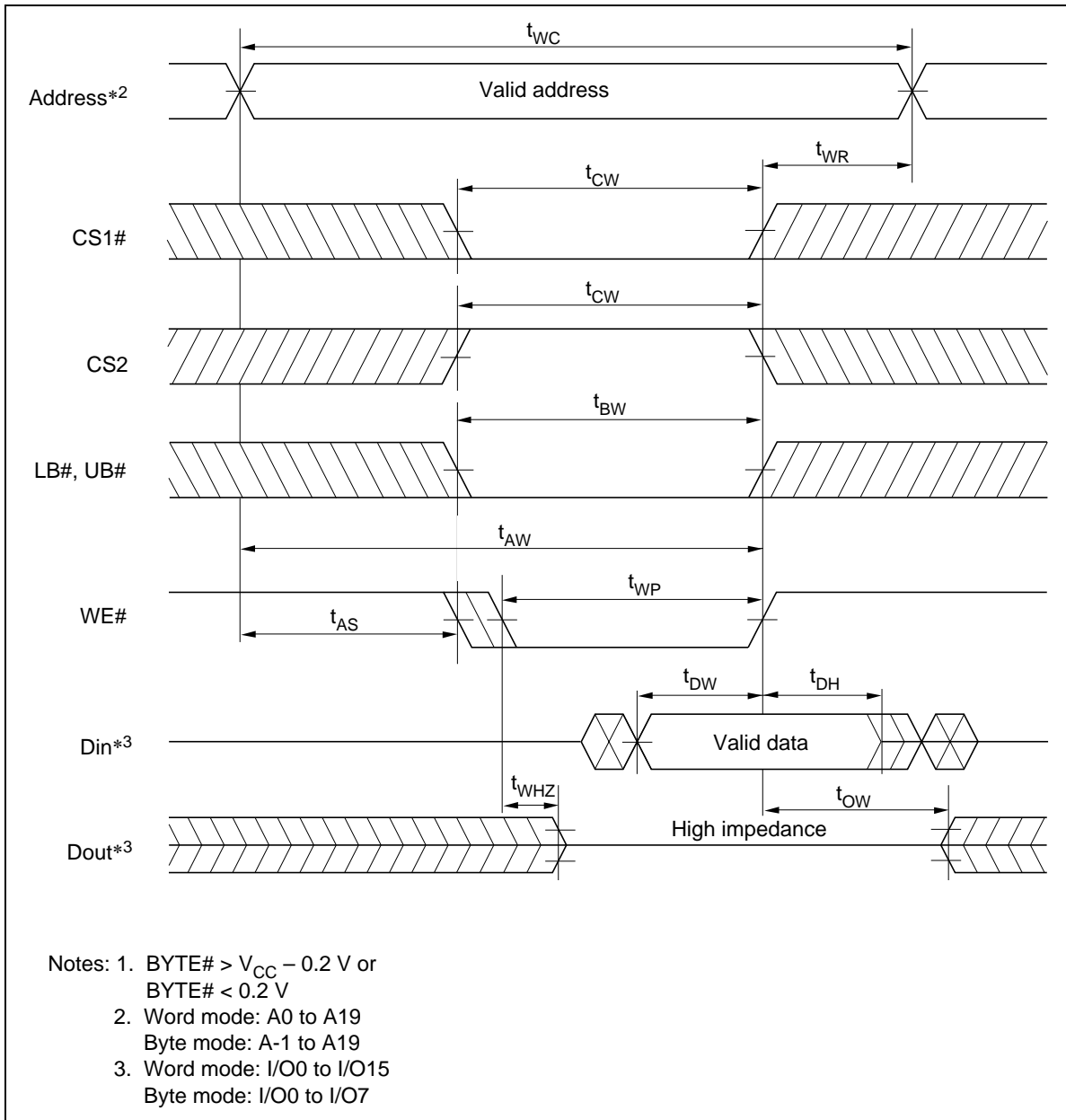
## Timing Waveform

### Read Cycle\*<sup>1</sup>



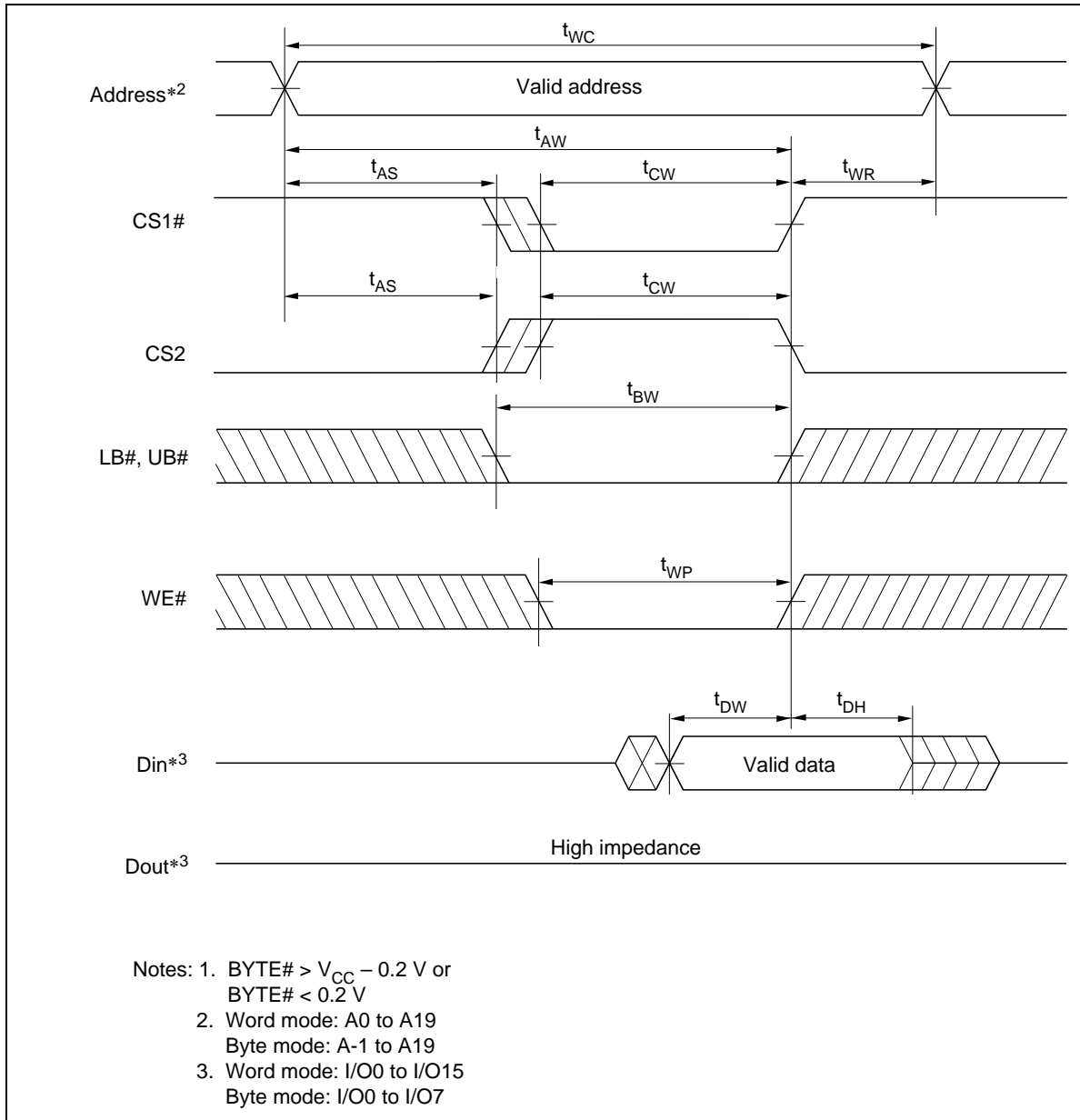
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### Write Cycle (1)\*<sup>1</sup> (WE# Clock)



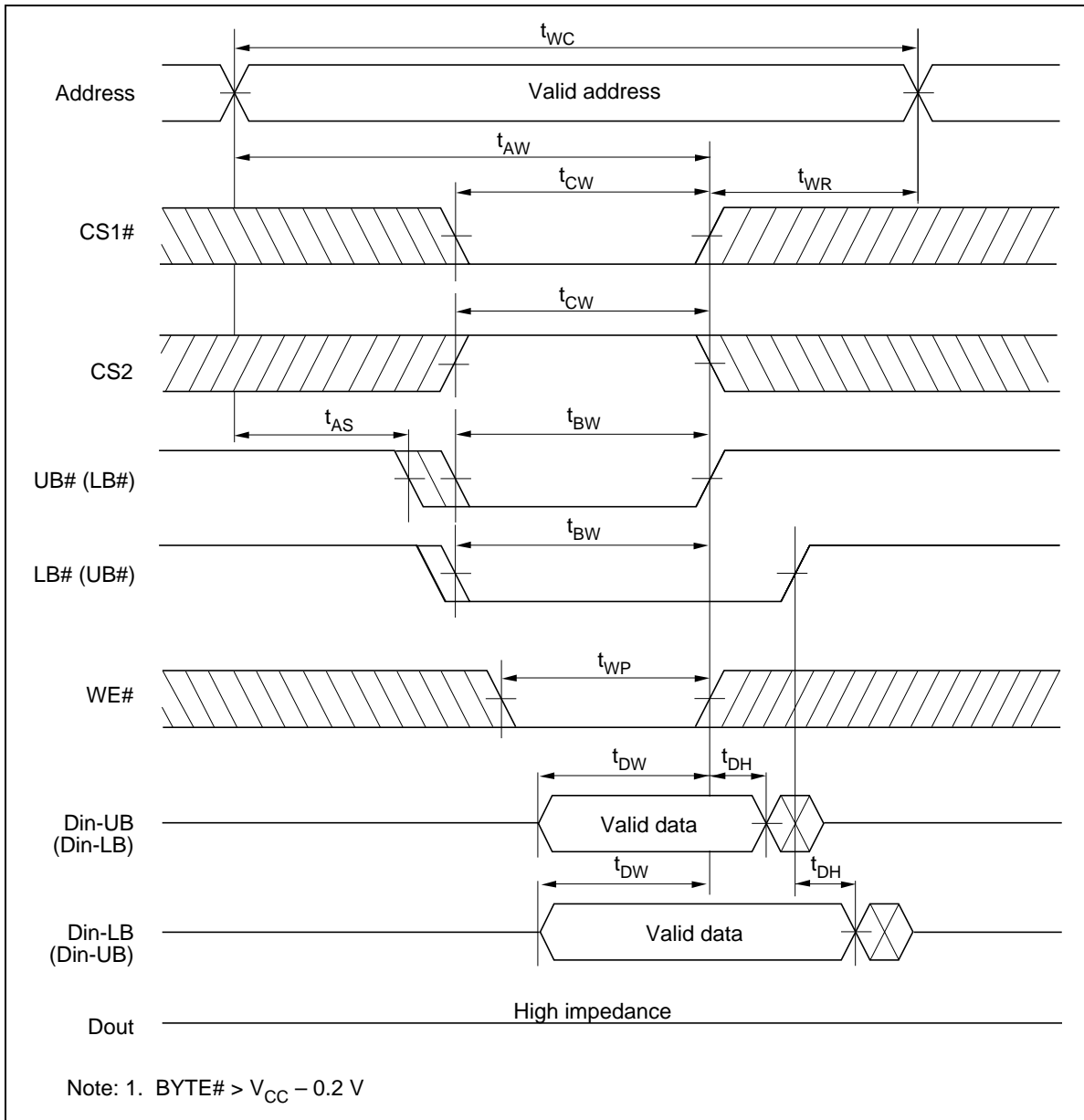
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Write Cycle (2)\*<sup>1</sup> (CS1#, CS2 Clock, OE# = V<sub>IH</sub>)



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**Write Cycle (3)\*<sup>1</sup> (LB#, UB# Clock, OE# = V<sub>IH</sub>)**

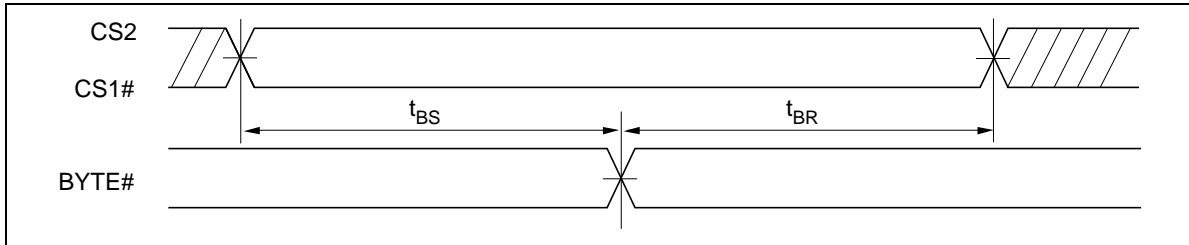




**R1LV1616H-I Series**

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**Byte Control (TSOP)**



**Low  $V_{CC}$  Data Retention Characteristics**

( $T_a = -40$  to  $+85^\circ\text{C}$ )

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions* <sup>2,3</sup>	
$V_{CC}$ for data retention	$V_{DR}$	1.5	—	3.6	V	$V_{in} \geq 0$ V (1) $0$ V $\leq$ CS2 $\leq$ 0.2 V or (2) CS2 $\geq$ $V_{CC} - 0.2$ V, CS1# $\geq$ $V_{CC} - 0.2$ V or (3) LB# = UB# $\geq$ $V_{CC} - 0.2$ V, CS2 $\geq$ $V_{CC} - 0.2$ V, CS1# $\leq$ 0.2 V	
Data retention current	-4SI	$I_{CCDR}$	—	0.5* <sup>1</sup>	8	$\mu\text{A}$	$V_{CC} = 3.0$ V, $V_{in} \geq 0$ V (1) $0$ V $\leq$ CS2 $\leq$ 0.2 V or (2) CS2 $\geq$ $V_{CC} - 0.2$ V, CS1# $\geq$ $V_{CC} - 0.2$ V or (3) LB# = UB# $\geq$ $V_{CC} - 0.2$ V, CS2 $\geq$ $V_{CC} - 0.2$ V, CS1# $\leq$ 0.2 V Average value
	-5SI			0.5* <sup>1</sup>	25	$\mu\text{A}$	
Chip deselect to data retention time	$t_{CDR}$	0	—	—	ns	See retention waveforms	
Operation recovery time	$t_R$	5	—	—	ms		

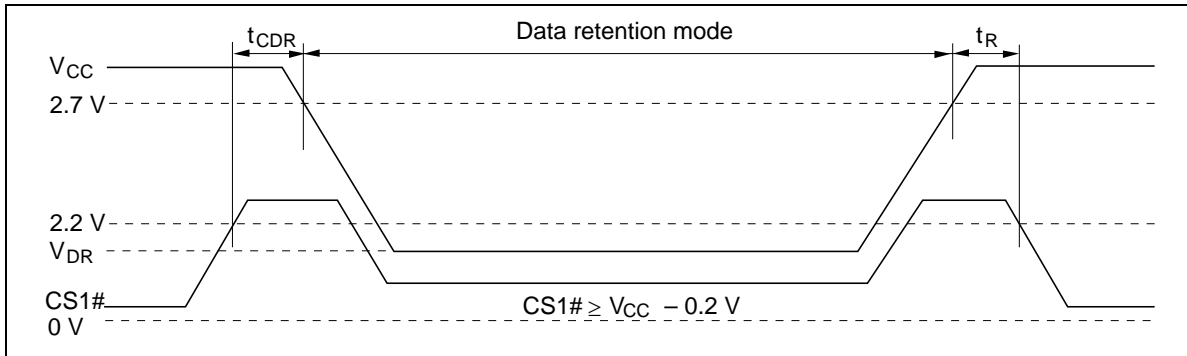
Notes: 1. Typical values are at  $V_{CC} = 3.0$  V,  $T_a = +25^\circ\text{C}$  and not guaranteed.

2. BYTE#  $\geq$   $V_{CC} - 0.2$  V or BYTE#  $\leq$  0.2 V

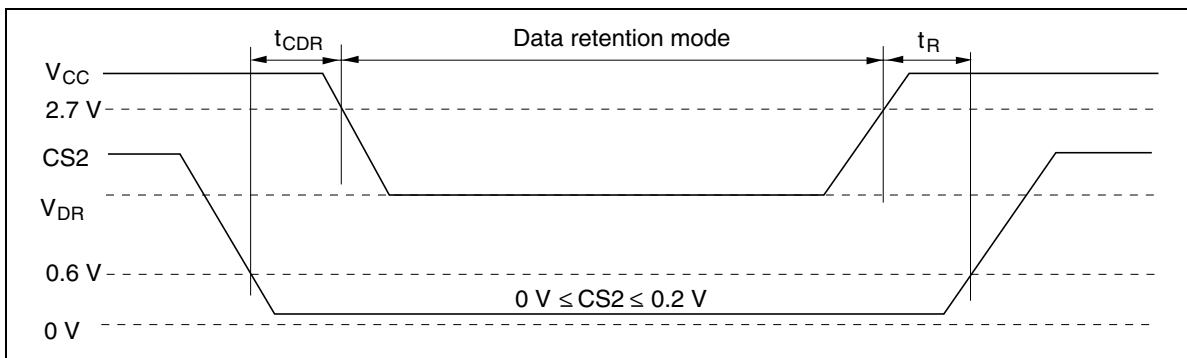
3. CS2 controls address buffer, WE# buffer, CS1# buffer, OE# buffer, LB#, UB# buffer and Din buffer. If CS2 controls data retention mode,  $V_{in}$  levels (address, WE#, OE#, CS1#, LB#, UB#, I/O) can be in the high impedance state. If CS1# controls data retention mode, CS2 must be CS2  $\geq$   $V_{CC} - 0.2$  V or  $0$  V  $\leq$  CS2  $\leq$  0.2 V. The other input levels (address, WE#, OE#, LB#, UB#, I/O) can be in the high impedance state.

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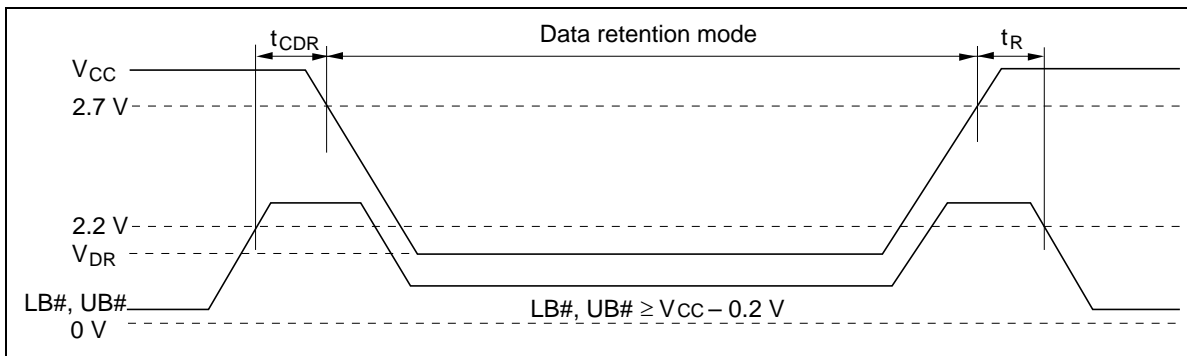
### Low $V_{CC}$ Data Retention Timing Waveform (1) (CS1# Controlled)



### Low $V_{CC}$ Data Retention Timing Waveform (2) (CS2 Controlled)



### Low $V_{CC}$ Data Retention Timing Waveform (3) (LB#, UB# Controlled)



## Revision History

## R1LV1616H-I Series Data Sheet

Rev.	Date	Contents of Modification	
		Page	Description
1.00	Apr. 22, 2004	—	Initial issue
1.01	Nov. 18, 2004	—	Addition of 2-Mword × 8-bit function

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