ELECTRONICS, INC. 44 FARRAND STREET

# NTE943, NTE943M, \& NTE943SM Integrated Circuit Low Power, Low Offset, Dual Voltage Comparator 

## Description:

The NTE943, NTE943M, and NTE943SM consist of two independent precision voltage comparators with an offset voltage speciication as low as 2.0 mV max for two comparators which were designed specifically to operate from a single power supply over a wid range of voltages. Operation from split power supplies is also possible and the low power supply current drain is independent of the magnitude of the power supply voltage. These comparators alos have a unique characteristic in that the input common-mode voltage range includesground, even though operated from a single powe supply voltage.
Application areas include limit comparators, simple analog to digital converters; pulse, squarewave and time delay generators; wide range VCO; MOS clock timers; multivibrators and high voltage digital logic gates. These devices are designed to directly interface with TTL and CMOS. When operated from both plus and minus power supplies they will directly interface with MOS logic where their low power drain is a distinct advantage over standard comparators.

## Features:

- Wide Single Supply

Volatge Range: 2.0 V to 36 V
Dual Supplies: $\pm 1.0 \mathrm{~V}$ to $\pm 18 \mathrm{~V}$

- Low Supply Current Drain ( 0.8 mA ) - Independent of Supply Voltage (1.0mW/Comparator at 5V)
- Low Input Biasing Current: 25nA
- Low Input Offset Current: $\pm 5 n \mathrm{~A}$
- Maximum Offset Voltage: $\pm 3 \mathrm{mV}$
- Input Common-Mode Voltage Range Includes Ground
- Differential Input Voltage Range Equal to the Power Supply Voltage
- Low Output Saturation Voltage: 240 mV @ 4mA
- Output Voltge Compatible with TTL, DTL, ECL, MOS, and CMOS Logic Sytems
- Available in 3 Different Case Styles:

8-Lead Metal Can: NTE943
8-Lead Mini DIP: NTE943M
8-Lead SOIC (Surface Mount): NTE943SM

Differential Input Voltage (Note 1) . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . 36V
Input Voltage . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . 0.3 C . i to +36 V
Power Dissipation (Note 2)
NTE943 . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . 660mW
NTE943M ......................................................................................... . . . . . . 780 mW
NTE943SM . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . 510mW
Output Short Circuit to GND (Note 3) . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . Continuous
Input Current ( $\mathrm{V}_{\mathrm{IN}}<-0.3 \mathrm{~V}$ ), Note 4) . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . 50mA
Operating Temperature Range . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . $0^{\circ}$ to $+70^{\circ} \mathrm{C}$
Storage Temperature Range . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . $65^{\circ}$ to $+150^{\circ} \mathrm{C}$
Lead Temperature (During Soldering, 10 sec) . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . $+260^{\circ} \mathrm{C}$
Note 1. Positive excursions of input voltage may exceed the power supply level. As long as the other voltage remains within the common-mode range, the comparator will provide a proper output state. The low input voltage state must not be less than -0.3 V (or 0.3 V below the the magnitude of the negative power supply, if used).
Note 2. For operating at elevated temperature, these devices must be derated based on a $125^{\circ} \mathrm{C}$ maximum junction temperature and a thermal resistance of $127^{\circ} \mathrm{C} / \mathrm{W}$ which applies for the device soldered in a printed circuit board, operating in a still air ambient. The low bias dissipation and the "ON-OFF" haracteristic of the output keeps the chip dissipation very small ( $\mathrm{P}_{\mathrm{D}} \leq 100 \mathrm{~mW}$ ), provided the output transistors are allowed to saturate.
Note 3. Short circuits from the output to V+ can cause excessive heating and eventual destruction. When considering short circuits to GND, the maximum output current is approximately 20 mA independent of the magnitude of $\mathrm{V}_{+}$.
Note 4. This input current will only exist when the voltage at any of th input leads is driven negative. It is due to the collector-base junction of the input PNP transistors becoming forward biased and thereby acting as input diode clamps. In addition to this diode action, there is also lateral NPN parasitic transistor action on the IC chip. This transistor action can cause the output voltages of the comparators to go to the V+ voltage level (or to GND for a large overdrive) for the time duration that an input is driven negative. This is not destructive and normal output states will re-establish when the input voltage, which was negative, again returns to a value greater than -0.3 V .

Electrical Characteristics: $\left(0^{\circ} \leq \mathrm{T}_{\mathrm{A}} \leq+70^{\circ} \mathrm{C}, \mathrm{V}+=5 \mathrm{~V}\right.$ unless otherwise specified)

| Parameter | Test Conditions | Min | Typ | Max | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: |
| Input Offset Voltage | Note 5 | - | - | $\pm 9.0$ | mV |
|  | $\mathrm{T}_{\mathrm{A}}=+25^{\circ} \mathrm{C}$, Note 5 | - | $\pm 1.0$ | $\pm 5.0$ | mV |
| Input Offset Current | $\mathrm{I}_{\mathrm{IN}}(+)-\mathrm{I}_{\mathrm{IN}}(-) \mathrm{V}_{\mathrm{CM}}=0 \mathrm{~V}$ | - | - | $\pm 150$ | nA |
|  | $\mathrm{I}_{\mathrm{IN}}(+)-\mathrm{I}_{\mathrm{IN}}(-) \mathrm{V}_{\mathrm{CM}}=0 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=+25^{\circ} \mathrm{C}$ | - | $\pm 5.0$ | $\pm 50$ | nA |
| Input Bias Current | $\mathrm{I}_{\mathrm{IN}}(+)$ or $\mathrm{I}_{\mathrm{IN}}(-)$ with Output in Linear Range, $\mathrm{V}_{\mathrm{CM}}=0 \mathrm{~V}$, Note 6 | - | - | 250 | nA |
|  | $\mathrm{l}_{\mathrm{IN}}(+)$ or $\mathrm{I}_{\mathrm{N}}(-)$ with Output in Linear Range, $\mathrm{V}_{\mathrm{CM}}=0 \mathrm{~V}$, $\mathrm{T}_{\mathrm{A}}=+25^{\circ} \mathrm{C}$, Note 6 | - | 25 | 250 | nA |

Note 5. At output switch point, $\mathrm{V}_{\mathrm{O}} \cong 1.4 \mathrm{~V}, \mathrm{R}_{\mathrm{S}}=0 \Omega$, with $\mathrm{V}+$ from 5 V to 30 V and over he full input common-mode range ( 0 V to $\mathrm{V}+-1.5 \mathrm{~V}$ ), at $25^{\circ} \mathrm{C}$.

Note 6. The direction of the input current is out of the IC due to the PNP input stage. This current is essentially constant, independent of the state of the output so no loading change exists on the reference or input lines.

Electrical Characteristics (Cont'd): $\left(0^{\circ} \leq \mathrm{T}_{\mathrm{A}} \leq+70^{\circ} \mathrm{C}, \mathrm{V}+=5 \mathrm{~V}\right.$ unless otherwise specified)

| Parameter | Test Conditions | Min | Typ | Max | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: |
| Input Common-Mode Voltage Range | $\mathrm{V}_{+}=30 \mathrm{~V}$, Note 7 | 0 | - | $\mathrm{V}+-2.0$ | V |
|  | $\mathrm{V}+=30 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=+25^{\circ} \mathrm{C}$, Note 7 | 0 | - | $\mathrm{V}+-1.5$ | V |
| Supply Current | $\mathrm{R}_{\mathrm{L}}=\infty$ on all Components, $\mathrm{T}_{\mathrm{A}}=+25^{\circ} \mathrm{C}$ | - | 0.4 | 1.0 | mA |
|  | $\mathrm{R}_{\mathrm{L}}=\infty$ on all Amps, $\mathrm{V}+=36 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=+25^{\circ} \mathrm{C}$ | - | 1 | 25 | mA |
| Voltage Gain | $\mathrm{R}_{\mathrm{L}} \geq 15 \mathrm{k} \Omega, \mathrm{V}+=15 \mathrm{~V}, \mathrm{~V}_{\mathrm{O}}=1 \mathrm{~V}$ to $11 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=+25^{\circ} \mathrm{C}$ | 50 | 200 | - | V/mV |
| Large Signal Response Time | $\begin{aligned} & V_{\text {IN }}=T T L \text { Logic Swing, } V_{\text {REF }}=1.4 \mathrm{~V}, \mathrm{~V}_{\mathrm{RL}}=5 \mathrm{~V}, \\ & \mathrm{R}_{\mathrm{L}}=1.5 \mathrm{k} \Omega, \mathrm{~T}_{\mathrm{A}}=+25^{\circ} \mathrm{C} \end{aligned}$ | - | 300 | - | ns |
| Response Time | $\mathrm{V}_{\mathrm{RL}}=5 \mathrm{~V}, \mathrm{R}_{\mathrm{L}}=1.5 \mathrm{k} \Omega, \mathrm{T}_{\mathrm{A}}=+25^{\circ} \mathrm{C}$, Note 7 | - | 1.3 | - | $\mu \mathrm{s}$ |
| Output Sink Current | $\mathrm{V}_{\text {IN }}(-)=1 \mathrm{~V}, \mathrm{~V}_{\mathrm{IN}}(+)=0, \mathrm{~V}_{\mathrm{O}} \geq 1.5 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=+25^{\circ} \mathrm{C}$ | 6 | 16 | - | mA |
| Saturation Voltage | $\mathrm{V}_{\text {IN }}(-)=1 \mathrm{~V}, \mathrm{~V}_{\text {IN }}(+)=0, \mathrm{I}_{\text {SINK }} \leq 4 \mathrm{~mA}$ | - | - | 700 | mV |
|  | $\mathrm{V}_{\text {IN }}(-)=1 \mathrm{~V}, \mathrm{~V}_{\text {IN }}(+)=0, \mathrm{I}_{\text {IINK }} \leq 4 \mathrm{~mA}, \mathrm{~T}_{\mathrm{A}}=+25^{\circ} \mathrm{C}$ | - | 250 | 400 | mV |
| Output Leakage Current | $\mathrm{V}_{\text {IN }}(-)=0, \mathrm{~V}_{\text {IN }}(+)=1 \mathrm{~V}, \mathrm{~V}_{\mathrm{O}}=30 \mathrm{~V}$ | - | - | 1.0 | $\mu \mathrm{A}$ |
|  | $\mathrm{V}_{\text {IN }}(-)=0, \mathrm{~V}_{\text {IN }}(+)=1 \mathrm{~V}, \mathrm{~V}_{\mathrm{O}}=5 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=+25^{\circ} \mathrm{C}$ | - | 0.1 | - | nA |
| Differential Input Voltage | Keep All $\mathrm{V}_{1 \times}$ 's $\geq 0 \mathrm{~V}$ (or V-, if Used), Note 1 | - | - | 36 | V |

Note 1. Positive excursions of input voltage may exceed the power supply level. As long as the other voltage remains within the common-mode range, the comparator will provide a proper output state. The low input voltage state must not be less than -0.3 V (or 0.3 V below the the magnitude of the negative power supply, if used).
Note 7. The response time specified is for a 100 mV input step with 5 mV overdrive. For larger overdrive signals 300 ns can be obtained.



