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NTE4000 & NTE4000T
Integrated Circuit
CMOS, Dual 3–Input NOR Gate Plus Inverter

Description:

The NTE4000 (14–Lead DIP) and NTE4000T (SOIC–14) are dual 3–input NOR gate plus inverter devices constructed with MOS P–Channel and N–Channel enhancement mode devices in a single monolithic structure. These complementary MOS logic gates find primary use where low power dissipation and/or high noise immunity is desired.

Features:

- Diode Protection on All Inputs
- Supply Voltage Range: 3Vdc to 18Vdc
- Logic Swing Independent of Fanout

Absolute Maximum Ratings: (Voltages referenced to V_{SS}, Note 1)

DC Supply Voltage, V_{DD} . . . . . –0.5 to +18.0V
Input Voltage (DC or Transient), V_{in} . . . . . –0.5 to V_{DD} to +0.5V
Output Voltage (DC or Transient), V_{out} . . . . . –0.5 to V_{DD} to +0.5V
Input Current (DC or Transient, Per Pin), I_{in} . . . . . ±10mA
Output Current (DC or Transient, Per Pin), I_{out} . . . . . ±10mA
Power Dissipation (Per Package), P_D 500mW
Temperature Derating (from +65° to +125°C) . . . . . –7.0mW/°C
Storage Temperature, T_{stg} . . . . . –65° to +150°C
Lead Temperature (During Soldering, 8sec max), T_L . . . . . +260°C

Note 1. Maximum Ratings are those values beyond which damage to the device may occur.

Electrical Characteristics: (Voltages referenced to V_{SS}, Note 2)

Parameter	Symbol	V_{DD} Vdc	−55°C		+25°C			+125°C		Unit
			Min	Max	Min	Typ	Max	Min	Max	
Output Voltage “0” Level	V_{OL}	5.0	–	0.05	–	0	0.05	–	0.05	Vdc
V_{in} = V_{DD} or 0		10	–	0.05	–	0	0.05	–	0.05	Vdc
		15	–	0.05	–	0	0.05	–	0.05	Vdc
“1” Level	V_{OH}	5.0	4.95	–	4.95	5.0	–	4.95	–	Vdc
V_{in} = 0 or V_{DD}		10	9.95	–	9.95	10	–	9.95	–	Vdc
		15	14.95	–	14.95	15	–	14.95	–	Vdc
Input Voltage “0” Level	V_{IL}									
(V_O = 4.5Vdc)		5.0	–	1.0	–	2.25	1.0	–	1.0	Vdc
(V_O = 9.0Vdc)		10	–	2.0	–	4.50	2.0	–	2.0	Vdc
(V_O = 13.5Vdc)		15	–	2.5	–	6.75	2.5	–	2.5	Vdc
“1” Level	V_{IH}									
(V_O = 0.5Vdc)		5.0	4.0	–	4.0	2.75	–	4.0	–	Vdc
(V_O = 1.0Vdc)		10	8.0	–	8.0	5.50	–	8.0	–	Vdc
(V_O = 1.5Vdc)		15	12.5	–	12.5	8.25	–	12.5	–	Vdc
Output Drive Current Source	I_{OH}									
(V_{OH} = 2.5Vdc)		5.0	–1.2	–	–1.0	–1.7	–	–0.7	–	mAdc
(V_{OH} = 4.6Vdc)		5.0	–0.25	–	–0.2	–0.36	–	–0.14	–	mAdc
(V_{OH} = 9.5Vdc)		10	–0.62	–	–0.5	–0.9	–	–0.35	–	mAdc
(V_{OH} = 13.5Vdc)		15	–1.8	–	–1.5	–1.5	–	–1.1	–	mAdc
Sink	I_{OL}									
(V_{OL} = 0.4Vdc)		5.0	0.64	–	0.51	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5Vdc)		10	1.6	–	1.3	2.25	–	0.9	–	mAdc
(V_{OL} = 1.5Vdc)		15	4.2	–	3.4	8.8	–	2.4	–	mAdc
Input Current	I_{in}	15	–	±0.1	–	±0.00001	±0.1	–	±0.1	µAdc
Input Capacitance (V_{IN} = 0)	C_{in}	–	–	–	–	5.0	7.5	–	–	pF
Quiescent Current	I_{DD}	5.0	–	0.25	–	0.0005	0.25	–	7.5	µAdc
(Per Package)		10	–	0.5	–	0.0010	0.5	–	15	µAdc
		15	–	1.0	–	0.0015	1.0	–	30	µAdc
Total Supply Current	I_T	5.0	I_T = (0.3µA/kHz) f + I_{DD}/N							µAdc
(Dynamic plus Quiescent, Per Gate, C_L = 50pF, Note 3, Note 4)		10	I_T = (0.6µA/kHz) f + I_{DD}/N							µAdc
		15	I_T = (0.8µA/kHz) f + I_{DD}/N							µAdc

Note 2. Data labeled “Typ” is not to be used for design purposes but is intended as an indication of the device’s potential performance.

Note 3. The formulas given are for the typical characteristics only at +25°C.

Note 4. To calculate total supply current at loads other than 50pF:

$$I_T(C_L) = I_T(50pF) + (C_L - 50)\ V_{fk}$$

where: I_T is in µA (per package), C_L in pF, V = (V_{DD} − V_{SS}) in volts, f in kHz is input frequency, and k = 0.001 x the number of exercised gates per package.

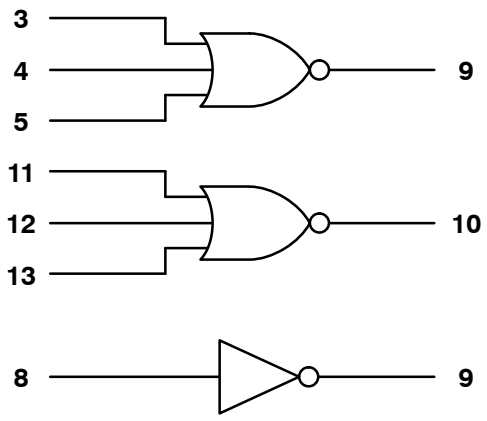
Switching Characteristics: (C_L = 50pF, T_A = +25°C, Note 2)

Parameter	Symbol	V_{DD} Vdc	Min	Typ	Max	Unit
Output Rise Time	t_{TLH}					
t_{TLH} = (3.0ns/pf) C_L + 30ns		5.0	–	180	360	ns
t_{TLH} = (1.5ns/pf) C_L + 15ns		10	–	90	180	ns
t_{TLH} = (1.1ns/pf) C_L + 10ns		15	–	65	130	ns
Output Fall Time	t_{THL}					
t_{THL} = (3.0ns/pf) C_L + 30ns		5.0	–	100	200	ns
t_{THL} = (1.5ns/pf) C_L + 15ns		10	–	50	100	ns
t_{THL} = (1.1ns/pf) C_L + 10ns		15	–	40	80	ns
Propagation Delay Time	t_{PLH}, t_{PHL}					
t_{PLH}, t_{PHL} = (1.7ns/pf) C_L + 30ns		5.0	–	115	230	ns
t_{PLH}, t_{PHL} = (0.66ns/pf) C_L + 22ns		10	–	55	110	ns
t_{PLH}, t_{PHL} = (0.50ns/pf) C_L + 15ns		15	–	40	80	ns

Note 2. Data labeled “Typ” is not to be used for design purposes but is intended as an indication of the device’s potential performance.

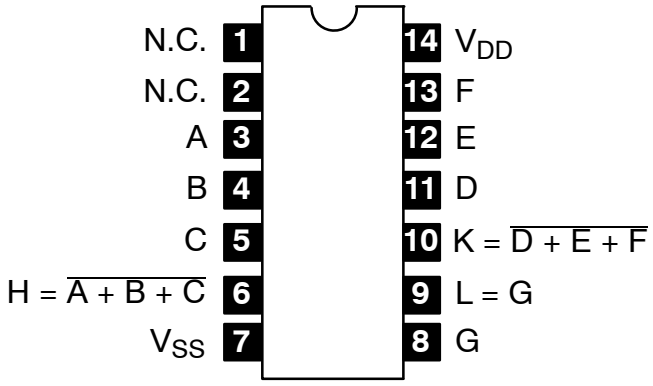
Note 3. The formulas given are for the typical characteristics only at +25°C.

Logic Diagram



V_{DD} = Pin14
V_{SS} = Pin7

Pin Connection Diagram



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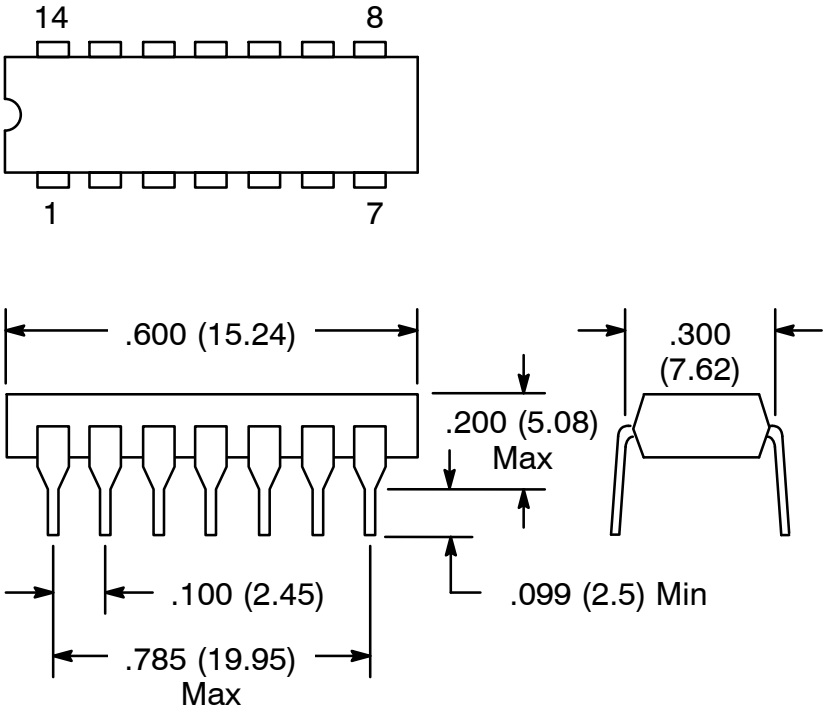

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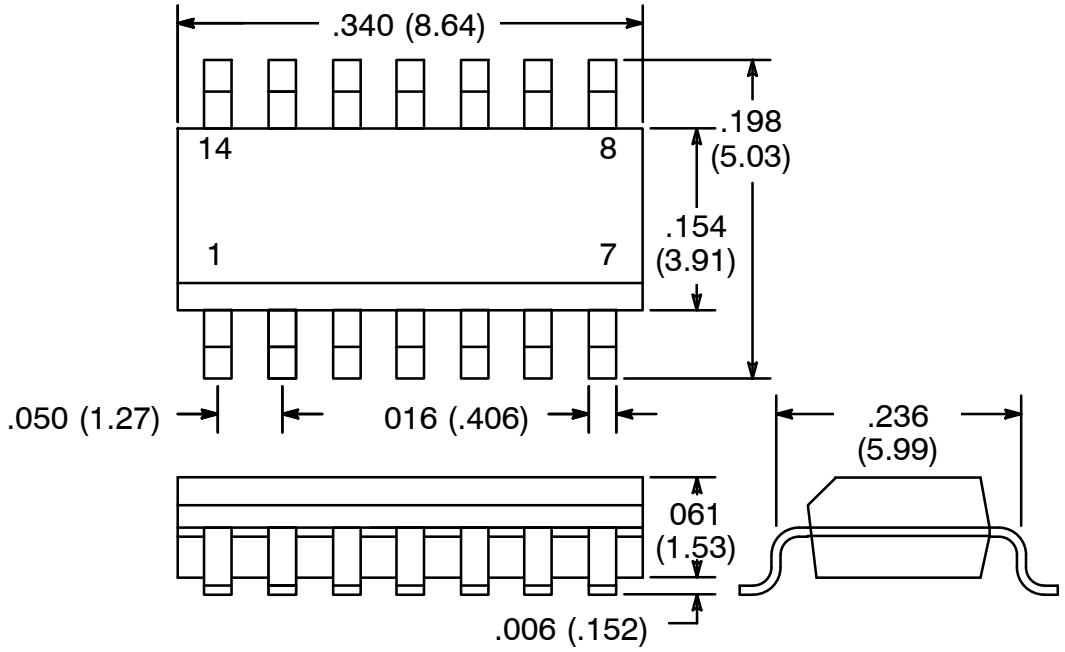

NOTE: Pin1 on Beveled Edge