TC4423A/TC4424A/TC4425A

3A Dual High-Speed Power MOSFET Drivers

Features

- High Peak Output Current: 4.5A (typ)
- Wide Input Supply Voltage Operating Range:
  - 4.5V to 18V
- High Capacitive Load Drive Capability:
  - 1800 pF in 12 ns
- Short Delay Times: 40 ns (typ)
- Matched Rise/Fall Times
- Low Supply Current:
  - With Logic '1' Input – 1.0 mA (Max)
  - With Logic '0' Input – 150 µA (Max)
- Low Output Impedance: 2.5Ω (typ)
- Latch-Up Protected: Will Withstand 1.5A Reverse Current
- Logic Input Will Withstand Negative Swing Up To 5V
- Pin compatible with the TC4423/TC4424/TC4425 and TC4426A/TC4427A/TC4428A devices
- Space-saving 8-Pin 150 mil body SOIC and 8-Pin 6x5 DFN Packages

Applications

- Switch Mode Power Supplies
- Pulse Transformer Drive
- Line Drivers
- Direct Drive of Small DC Motors

General Description

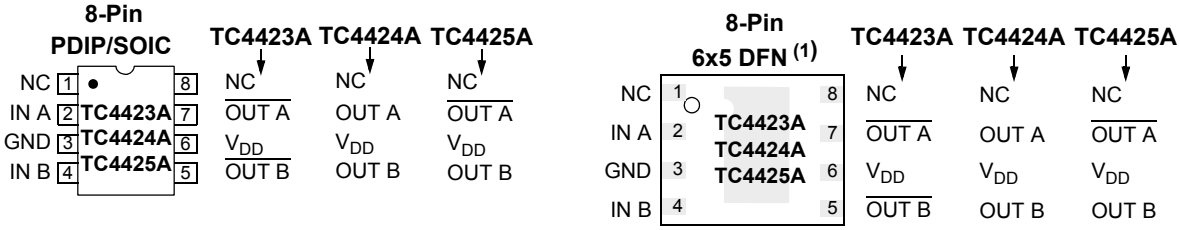
The TC4423A/TC4424A/TC4425A devices are a family of dual-output 3A buffers/MOSFET drivers. These devices are improved versions of the earlier TC4423/TC4424/TC4425 dual-output 3A driver family. This improved version features higher peak output current drive capability, lower shoot-throught current, matched rise/fall times and propagation delay times. The TC4423A/TC4424A/TC4425A devices are pin-compatible with the existing TC4423/TC4424/TC4425 family. An 8-pin SOIC package option has been added to the family. The 8-pin DFN package option offers increased power dissipation capability for driving heavier capacitive or resistive loads.

The TC4423A/TC4424A/TC4425A MOSFET drivers can easily charge and discharge 1800 pF gate capacitance in under 20 ns, provide low enough impedances in both the on and off states to ensure the MOSFET's intended state will not be affected, even by large transients.

The TC4423A/TC4424A/TC4425A inputs may be driven directly from either TTL or CMOS (2.4V to 18V). In addition, the 300 mV of built-in hysteresis provides noise immunity and allows the device to be driven from slow rising or falling waveforms.

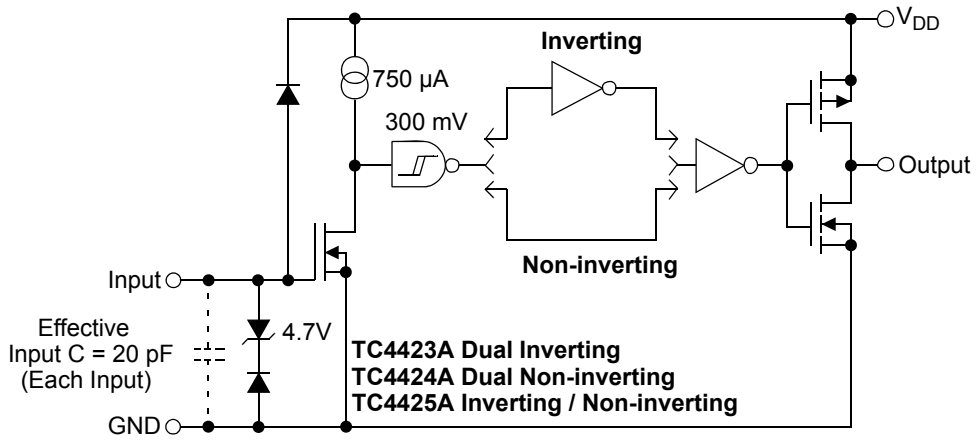
The TC4423A/TC4424A/TC4425A dual-output 3A MOSFET driver family is offerd with a -40°C to +125°C temperature rating, making it usful in any wide temperature range application.

Package Types



Note 1: Exposed pad of the DFN package is electrically isolated.

Functional Block Diagram(1)



Note 1: Unused inputs should be grounded.

1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings †

Supply Voltage .....+20V
Input Voltage, IN A or IN B .....(V_{DD} + 0.3V) to (GND – 5V)

† **Notice:** Stresses above those listed under "Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational sections of this specification is not intended. Exposure to maximum rating conditions for extended periods may affect device reliability.

DC CHARACTERISTICS (NOTE 2)

Electrical Specifications: Unless otherwise indicated, T_A = +25°C, with 4.5V ≤ V_{DD} ≤ 18V.

Parameters	Sym	Min	Typ	Max	Units	Conditions
Input						
Logic '1', High Input Voltage	V_{IH}	2.4	1.5	—	V	
Logic '0', Low Input Voltage	V_{IL}	—	1.3	0.8	V	
Input Current	I_{IN}	–1	—	1	µA	0V ≤ V_{IN} ≤ V_{DD}
Input Voltage	V_{IN}	-5	—	V_{DD}+0.3	V	
Output						
High Output Voltage	V_{OH}	V_{DD} – 0.025	—	—	V	DC Test
Low Output Voltage	V_{OL}	—	—	0.025	V	DC Test
Output Resistance, High	R_{OH}	—	2.2	3.0	Ω	I_{OUT} = 10 mA, V_{DD} = 18V
Output Resistance, Low	R_{OL}	—	2.8	3.5	Ω	I_{OUT} = 10 mA, V_{DD} = 18V
Peak Output Current	I_{PK}	—	4.5	—	A	10V≤ V_{DD} ≤18V **(Note 2)**
Latch-Up Protection Withstand Reverse Current	I_{REV}	—	>1.5	—	A	Duty cycle ≤ 2%, t ≤ 300 µsec.
Switching Time (Note 1)						
Rise Time	t_R	—	12	21	ns	Figure 4-1, Figure 4-2, C_L = 1800 pF
Fall Time	t_F	—	12	21	ns	Figure 4-1, Figure 4-2, C_L = 1800 pF
Delay Time	t_{D1}	—	40	48	ns	Figure 4-1, Figure 4-2, C_L = 1800 pF
Delay Time	t_{D2}	—	41	48	ns	Figure 4-1, Figure 4-2, C_L = 1800 pF
Power Supply						
Supply Voltage	V_{DD}	4.5	—	18	V	
Power Supply Current	I_S	—	1.0	2.0	mA	V_{IN} = 3V (Both inputs)
	I_S	—	0.15	0.25	mA	V_{IN} = 0V (Both inputs)

Note 1: Switching times ensured by design.
2: Tested during characterization, not production tested.

DC CHARACTERISTICS (OVER OPERATING TEMPERATURE RANGE)

Electrical Specifications: Unless otherwise indicated, operating temperature range with 4.5V ≤ V_{DD} ≤ 18V.

Parameters	Sym	Min	Typ	Max	Units	Conditions
Input						
Logic '1', High Input Voltage	V_{IH}	2.4	—	—	V	
Logic '0', Low Input Voltage	V_{IL}	—	—	0.8	V	
Input Current	I_{IN}	–10	—	+10	µA	0V ≤ V_{IN} ≤ V_{DD}
Output						
High Output Voltage	V_{OH}	V_{DD} – 0.025	—	—	V	
Low Output Voltage	V_{OL}	—	—	0.025	V	
Output Resistance, High	R_{OH}	—	3.1	6	Ω	I_{OUT} = 10 mA, V_{DD} = 18V
Output Resistance, Low	R_{OL}	—	3.7	7	Ω	I_{OUT} = 10 mA, V_{DD} = 18V
Switching Time (Note 1)						
Rise Time	t_R	—	20	31	ns	Figure 4-1, Figure 4-2, C_L = 1800 pF
Fall Time	t_F	—	22	31	ns	Figure 4-1, Figure 4-2, C_L = 1800 pF
Delay Time	t_{D1}	—	50	66	ns	Figure 4-1, Figure 4-2, C_L = 1800 pF
Delay Time	t_{D2}	—	50	66	ns	Figure 4-1, Figure 4-2, C_L = 1800 pF
Power Supply						
Power Supply Current	I_S	— —	2.0 0.2	3.0 0.3	mA	V_{IN} = 3V (Both inputs) V_{IN} = 0V (Both inputs)

Note 1: Switching times ensured by design.

TEMPERATURE CHARACTERISTICS

Electrical Specifications: Unless otherwise noted, all parameters apply with 4.5V ≤ V_{DD} ≤ 18V.

Parameters	Sym	Min	Typ	Max	Units	Conditions
Temperature Ranges						
Specified Temperature Range (V)	T_A	–40	—	+125	°C	
Maximum Junction Temperature	T_J	—	—	+150	°C	
Storage Temperature Range	T_A	–65	—	+150	°C	
Package Thermal Resistances						
Thermal Resistance, 8L-6x5 DFN	θ_{JA}	—	33.2	—	°C/W	Typical four-layer board with vias to ground plane
Thermal Resistance, 8L-PDIP	θ_{JA}	—	125	—	°C/W	
Thermal Resistance, 8L-SOIC	θ_{JA}	—	155	—	°C/W	

2.0 TYPICAL PERFORMANCE CURVES

Note: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore outside the warranted range.

Note: Unless otherwise indicated, T_A = +25C with 4.5V <= V_{DD} <= 18V.

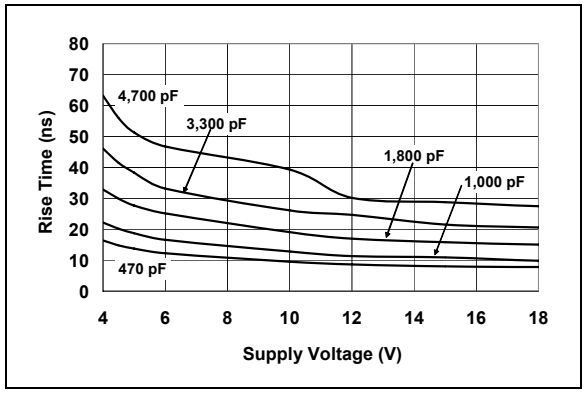


FIGURE 2-1: *Rise Time vs. Supply Voltage.*

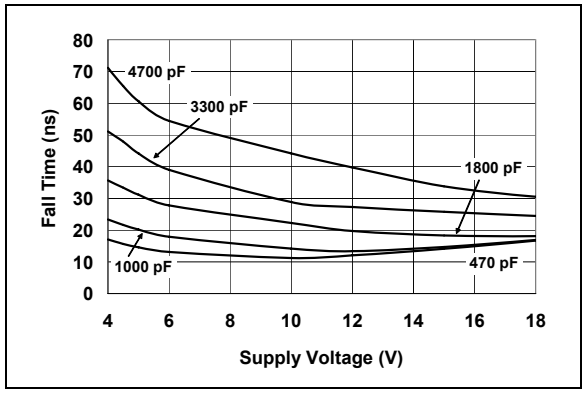


FIGURE 2-4: *Fall Time vs. Supply Voltage.*

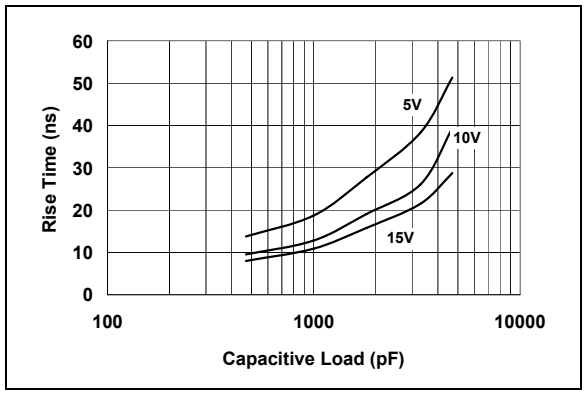


FIGURE 2-2: *Rise Time vs. Capacitive Load.*

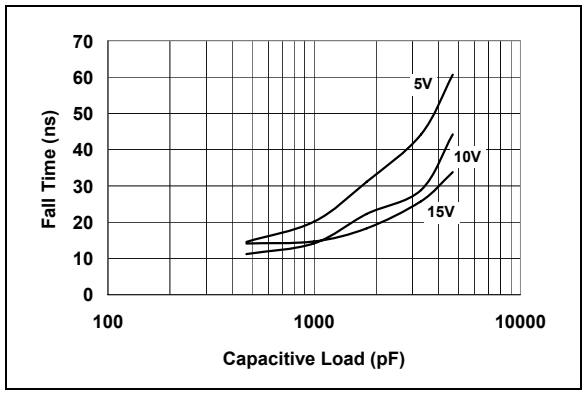


FIGURE 2-5: *Fall Time vs. Capacitive Load.*

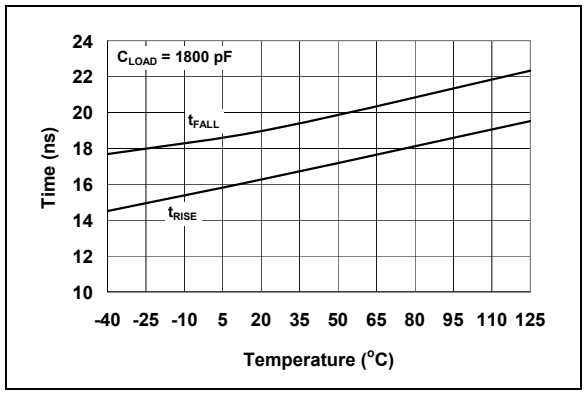


FIGURE 2-3: *Rise and Fall Times vs. Temperature.*

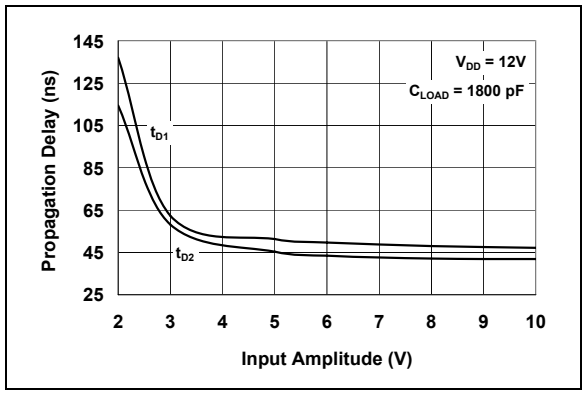


FIGURE 2-6: *Propagation Delay vs. Input Amplitude.*

Typical Performance Curves (Continued)

Note: Unless otherwise indicated, T_A = +25C with 4.5V <= V_{DD} <= 18V.

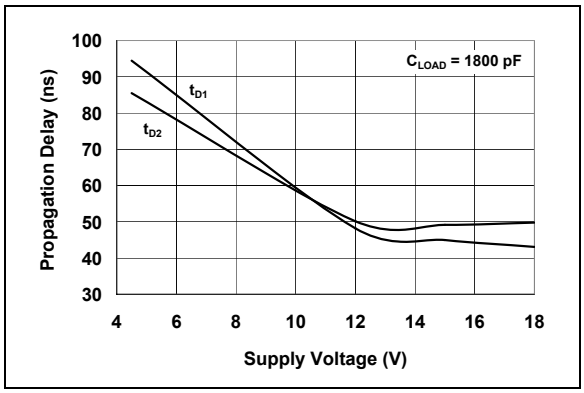


FIGURE 2-7: *Propagation Delay Time vs. Supply Voltage.*

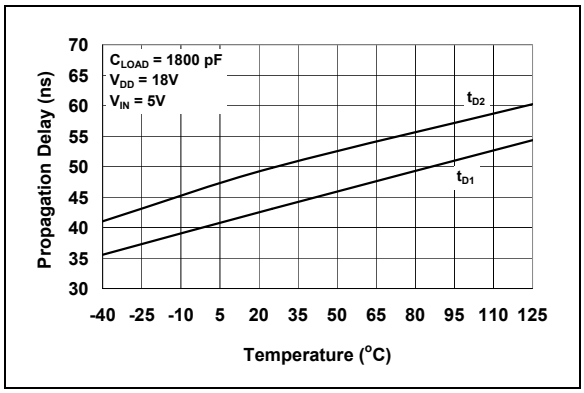


FIGURE 2-10: *Propagation Delay Time vs. Temperature.*

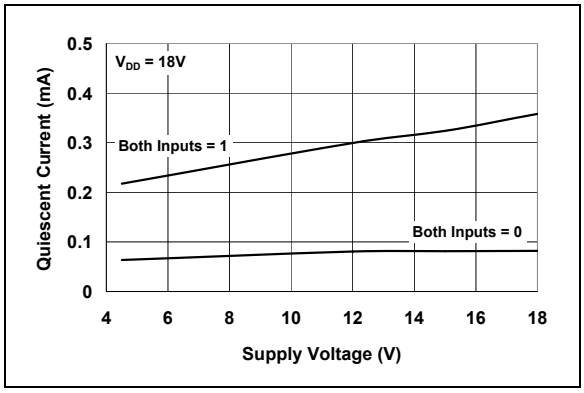


FIGURE 2-8: *Quiescent Current vs. Supply Voltage.*

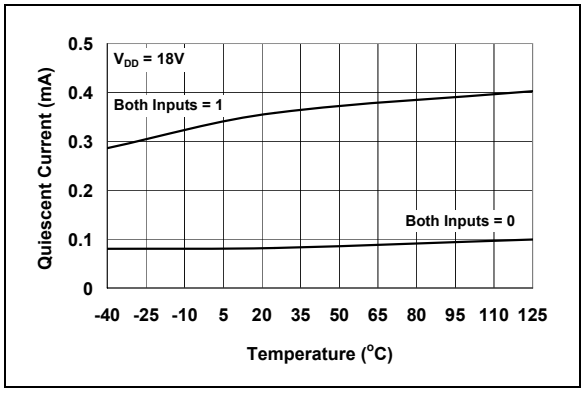


FIGURE 2-11: *Quiescent Current vs. Temperature.*

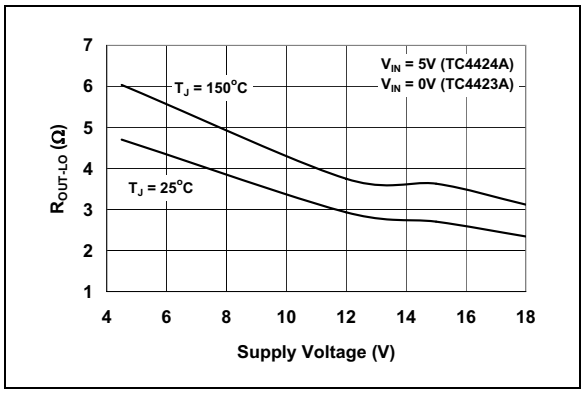


FIGURE 2-9: *Output Resistance (Output Low) vs. Supply Voltage.*

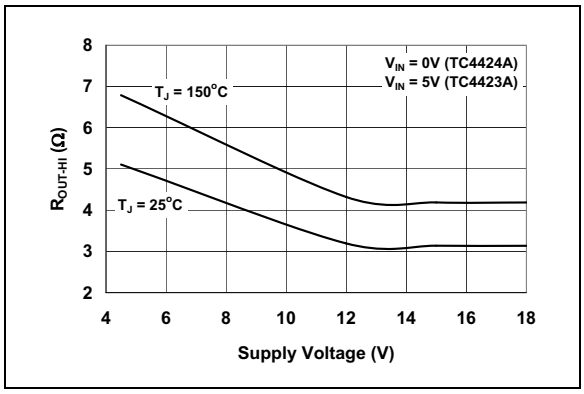


FIGURE 2-12: *Output Resistance (Output High) vs. Supply Voltage.*

Typical Performance Curves (Continued)

Note: Unless otherwise indicated, T_A = +25C with 4.5V <= V_{DD} <= 18V.

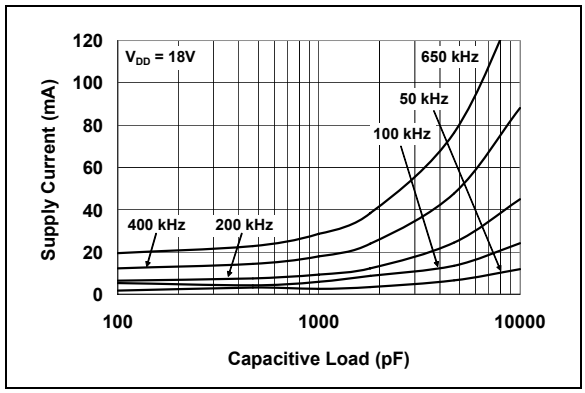


FIGURE 2-13: *Supply Current vs. Capacitive Load.*

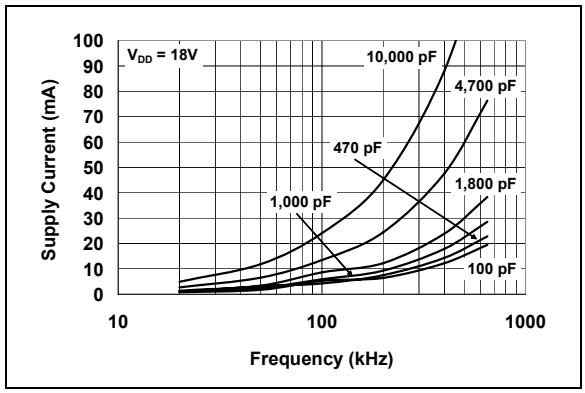


FIGURE 2-16: *Supply Current vs. Frequency.*

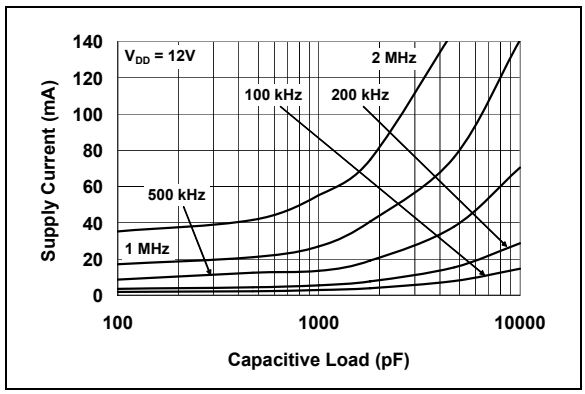


FIGURE 2-14: *Supply Current vs. Capacitive Load.*

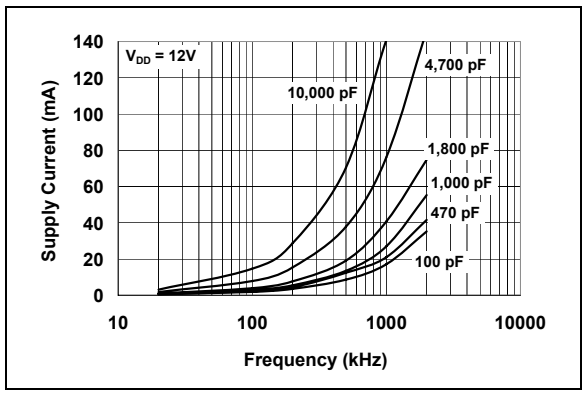


FIGURE 2-17: *Supply Current vs. Frequency.*

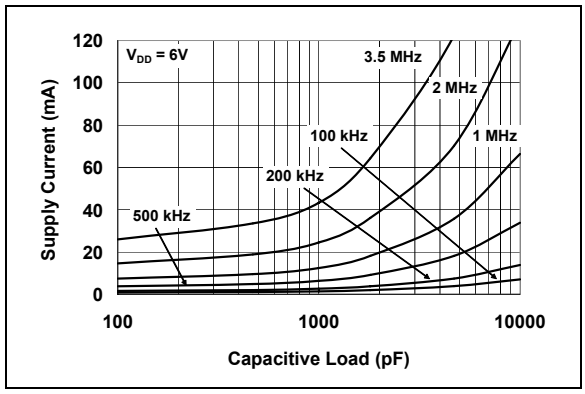


FIGURE 2-15: *Supply Current vs. Capacitive Load.*

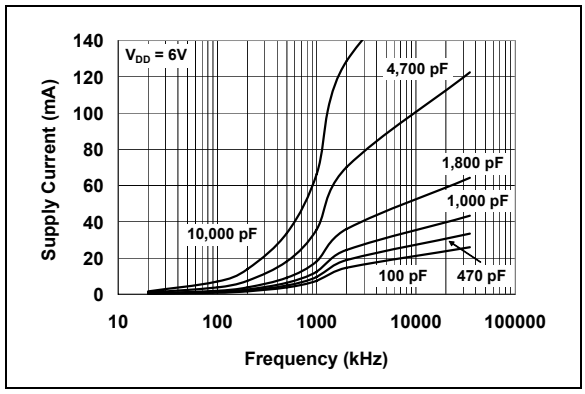
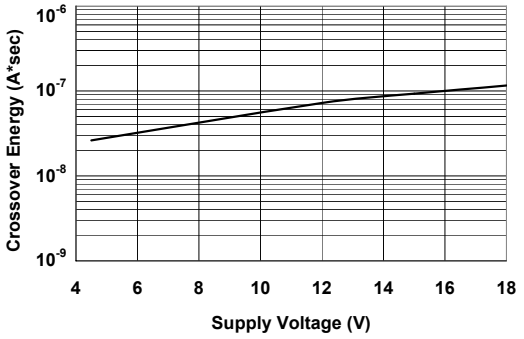


FIGURE 2-18: *Supply Current vs. Frequency.*

Typical Performance Curves (Continued)

Note: Unless otherwise indicated, T_A = +25C with 4.5V <= V_{DD} <= 18V.



Note: The values on this graph represents the loss seen by both drivers in a package during one complete cycle. For a single driver, divide the stated values by 2. For a single transition of a single driver, divide the stated value by 4.

FIGURE 2-19: Crossover Energy vs. Supply Voltage.

3.0 PIN DESCRIPTIONS

The descriptions of the pins are listed in Table 3-1.

TABLE 3-1: PIN FUNCTION TABLE (1)

8-Pin PDIP, SOIC	8-Pin DFN	Symbol	Description
1	1	NC	No Connection
2	2	IN A	Input A
3	3	GND	Ground
4	4	IN B	Input B
5	5	OUT B	Output B
6	6	V_{DD}	Supply Input
7	7	OUT A	Output A
8	8	NC	No Connection
—	PAD	NC	Exposed Metal Pad

Note 1: Duplicate pins must be connected for proper operation.

3.1 Inputs A and B

Inputs A and B are TTL/CMOS compatible inputs that control outputs A and B, respectively. These inputs have 300 mV of hysteresis between the high and low input levels, allowing them to be driven from slow rising and falling signals, and to provide noise immunity.

3.2 Outputs A and B

Outputs A and B are CMOS push-pull outputs that are capable of sourcing and sinking 3A peaks of current (V_{DD} = 18V). The low output impedance ensures the gate of the external MOSFET will stay in the intended state even during large transients. These outputs also have a reverse current latch-up rating of 1.5A.

3.3 Supply Input (V_{DD})

V_{DD} is the bias supply input for the MOSFET driver and has a voltage range of 4.5V to 18V. This input must be decoupled to ground with a local ceramic capacitor. This bypass capacitor provides a localized low-impedance path for the peak currents that are to be provided to the load.

3.4 Ground (GND)

Ground is the device return pin. The ground pin should have a low-impedance connection to the bias supply source return. High peak currents will flow out the ground pin when the capacitive load is being discharged.

3.5 Exposed Metal Pad

The exposed metal pad of the DFN package is not internally connected to any potential. Therefore, this pad can be connected to a ground plane or other copper plane on a printed circuit board to aid in heat removal from the package.

4.0 APPLICATIONS INFORMATION

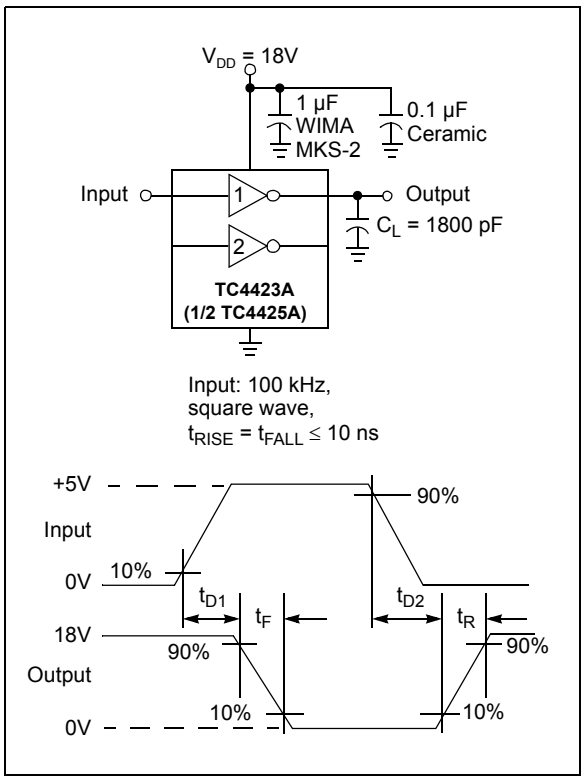


FIGURE 4-1: *Inverting Driver Switching Time.*

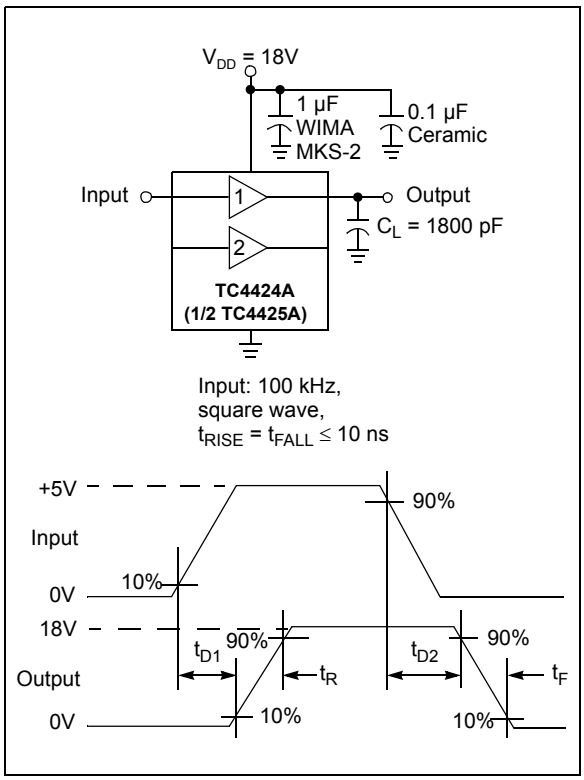
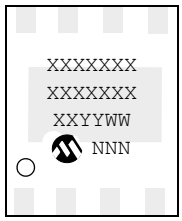


FIGURE 4-2: *Non-inverting Driver Switching Time.*

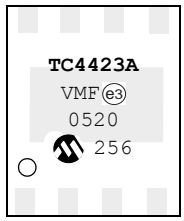
5.0 PACKAGING INFORMATION

5.1 Package Marking Information (Not to Scale)

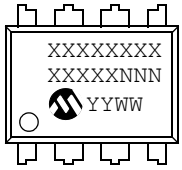
8-Lead DFN



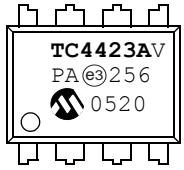
Example:



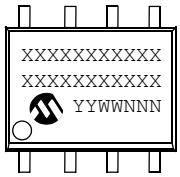
8-Lead PDIP (300 mil)



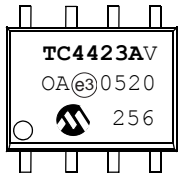
Example:



8-Lead SOIC (150 mil)



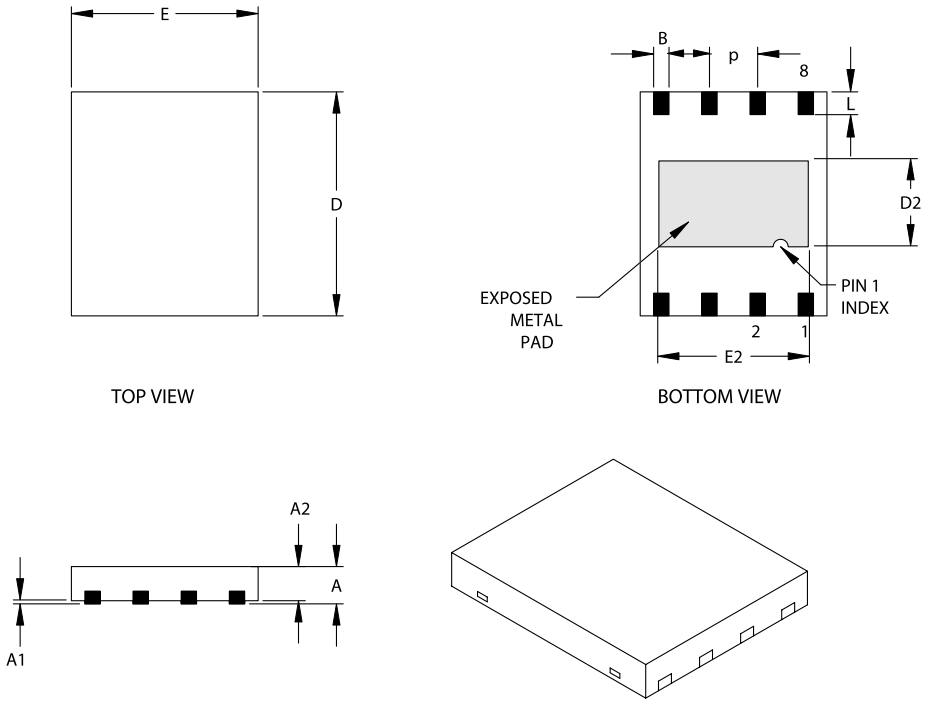
Example:



Legend:	XX...X	Customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week ‘01’)
	NNN	Alphanumeric traceability code
	(e3)	Pb-free JEDEC designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package.

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.

8-Lead Plastic Dual-Flat, No-Lead Package (MF) 6x5 mm Body (DFN-S) – Saw Singulated

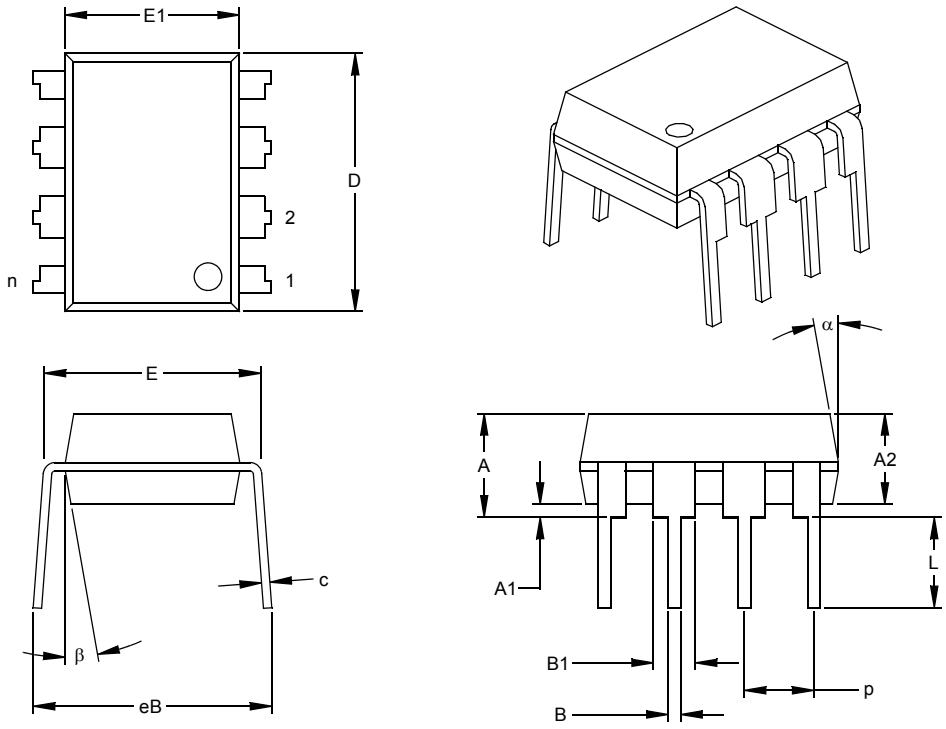


Units		INCHES			MILLIMETERS*		
Dimension Limits		MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		8			8	
Pitch	p		.050 BSC			1.27 BSC	
Overall Height	A	.033	.035	.037	0.85	0.90	0.95
Package Thickness	A2	.031	.035	.037	0.80	0.89	0.95
Standoff	A1	.000	.0004	.002	0.00	0.01	0.05
Base Thickness	A3	.007	.008	.009	0.17	0.20	0.23
Overall Length	E	.195	.197	.199	4.95	5.00	5.05
Exposed Pad Length	E2	.152	.157	.163	3.85	4.00	4.15
Overall Width	D	.234	.236	.238	5.95	6.00	6.05
Exposed Pad Width	D2	.089	.091	.093	2.25	2.30	2.35
Lead Width	B	.014	.016	.019	0.35	0.40	0.47
Lead Length	L	.024		.026	0.60		0.65

Notes:
JEDEC Equivalent: M0-220
Drawing No. C04-122

Revised 11/3/03

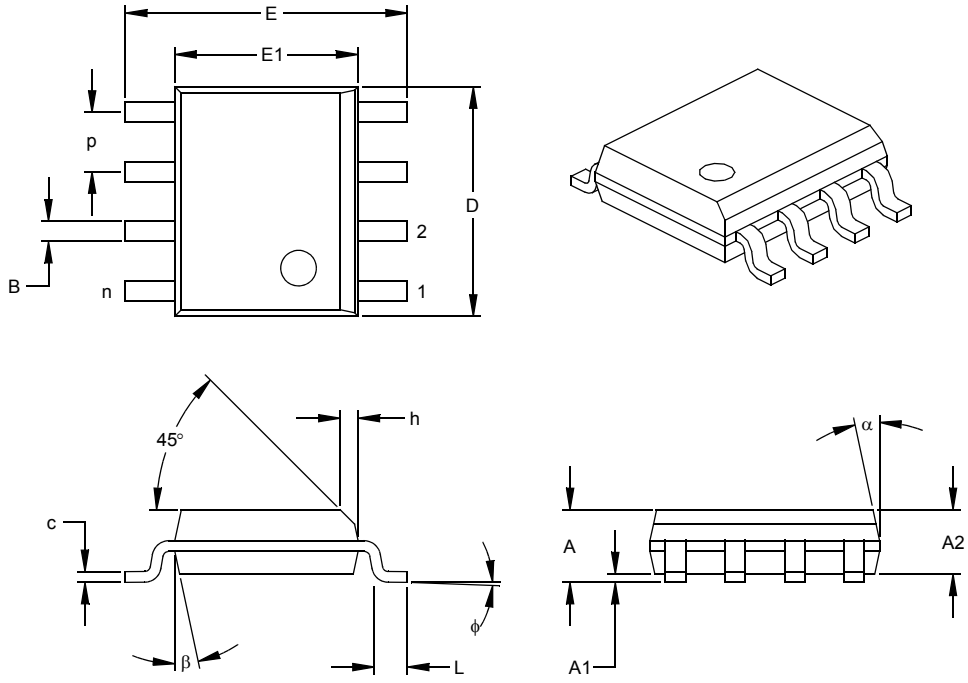
8-Lead Plastic Dual In-line (PA) – 300 mil Body (PDIP)



Units		INCHES*			MILLIMETERS		
Dimension Limits		MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		8			8	
Pitch	p		.100			2.54	
Top to Seating Plane	A	.140	.155	.170	3.56	3.94	4.32
Molded Package Thickness	A2	.115	.130	.145	2.92	3.30	3.68
Base to Seating Plane	A1	.015			0.38		
Shoulder to Shoulder Width	E	.300	.313	.325	7.62	7.94	8.26
Molded Package Width	E1	.240	.250	.260	6.10	6.35	6.60
Overall Length	D	.360	.373	.385	9.14	9.46	9.78
Tip to Seating Plane	L	.125	.130	.135	3.18	3.30	3.43
Lead Thickness	c	.008	.012	.015	0.20	0.29	0.38
Upper Lead Width	B1	.045	.058	.070	1.14	1.46	1.78
Lower Lead Width	B	.014	.018	.022	0.36	0.46	0.56
Overall Row Spacing §	eB	.310	.370	.430	7.87	9.40	10.92
Mold Draft Angle Top	α	5	10	15	5	10	15
Mold Draft Angle Bottom	β	5	10	15	5	10	15

* Controlling Parameter
§ Significant Characteristic
Notes:
Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010” (0.254mm) per side.
JEDEC Equivalent: MS-001
Drawing No. C04-018

8-Lead Plastic Small Outline (OA) – Narrow, 150 mil Body (SOIC)



Units		INCHES*			MILLIMETERS		
Dimension Limits		MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		8			8	
Pitch	p		.050			1.27	
Overall Height	A	.053	.061	.069	1.35	1.55	1.75
Molded Package Thickness	A2	.052	.056	.061	1.32	1.42	1.55
Standoff §	A1	.004	.007	.010	0.10	0.18	0.25
Overall Width	E	.228	.237	.244	5.79	6.02	6.20
Molded Package Width	E1	.146	.154	.157	3.71	3.91	3.99
Overall Length	D	.189	.193	.197	4.80	4.90	5.00
Chamfer Distance	h	.010	.015	.020	0.25	0.38	0.51
Foot Length	L	.019	.025	.030	0.48	0.62	0.76
Foot Angle	ϕ	0	4	8	0	4	8
Lead Thickness	c	.008	.009	.010	0.20	0.23	0.25
Lead Width	B	.013	.017	.020	0.33	0.42	0.51
Mold Draft Angle Top	α	0	12	15	0	12	15
Mold Draft Angle Bottom	β	0	12	15	0	12	15

***** Controlling Parameter

§ Significant Characteristic

Notes:

Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010” (0.254mm) per side.

JEDEC Equivalent: MS-012

Drawing No. C04-057

APPENDIX A: REVISION HISTORY

Revision A (June 2006)

- Original Release of this Document.

NOTES:

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

PART NO.	X	XX	XXX
Device	Temperature Range	Package	Tape & Reel

Device:	TC4423A:	3A Dual MOSFET Driver, Inverting
	TC4424A:	3A Dual MOSFET Driver, Non-Inverting
	TC4425A:	3A Dual MOSFET Driver, Complementary
Temperature Range:	V =	-40°C to +125°C
Package: *	MF =	Dual, Flat, No-Lead (6x5 mm Body), 8-lead
	MF713 =	Dual, Flat, No-Lead (6x5 mm Body), 8-lead (Tape and Reel)
	OA =	Plastic SOIC (150 mil Body), 8-Lead
	OA713 =	Plastic SOIC (150 mil Body), 8-Lead (Tape and Reel)
	PA =	Plastic DIP, (300 mil body), 8-lead

* All package offerings are Pb Free (Lead Free)

Examples:

a) TC4423AVOA: 3A Dual Inverting MOSFET Driver, 8LD SOIC package.

b) TC4423AVPA: 3A Dual Inverting MOSFET Driver, 8LD PDIP package.

c) TC4423AVMF: 3A Dual Inverting MOSFET Driver, 8LD DFN package.

a) TC4424AVOA713: 3A Dual Non-Inverting, MOSFET Driver, 8LD SOIC package, Tape and Reel.

b) TC4424AVPA: 3A Dual Non-Inverting, MOSFET Driver, 8LD PDIP package.

a) TC4425AVOA: 3A Dual Complementary, MOSFET Driver, 8LD SOIC package.

b) TC4425AVPA: 3A Dual Complementary, MOSFET Driver, 8LD PDIP package.

NOTES:

Note the following details of the code protection feature on Microchip devices:

- Microchip products meet the specification contained in their particular Microchip Data Sheet.
- Microchip believes that its family of products is one of the most secure families of its kind on the market today, when used in the intended manner and under normal conditions.
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