Introduction

This application note provides detailed information and PCB design guidelines on implementing a 1-port Power over Ethernet (PoE) system, based on Microsemi's™ 1-channel PoE Manager, the PD69101. Using this application note, a PCB designer can integrate PoE capabilities into an Ethernet switch.

The PD69101 is designed to implement all real time functions as specified in the IEEE 802.3af-2003 and IEEE802.3at-2009 standard including detection, classification and port status monitoring. The PD69101 is designed to detect and disable disconnected ports, using the DC disconnection method, as specified in the standard.

This application note is to be used in conjunction with application note *AN-184, Designing a 1 Port PoE System Using PD69101, Catalogue Number 06-0079-080*.

Applicable Documents

- IEEE 802.3af-2003 standard, DTE Power via MDI
- IEEE802.3at-2009 standard, DTE Power via MDI
- PD69101 Data Sheet, Catalogue Number 06-0076-058
- Microsemi Application Note AN-184 Catalogue Number 06-0079-080 Designing a 1-port PoE System (802.3af/802.3at Compliant)

Approach

To properly integrate the PD69101 PoE Manager into a new circuit or adapt an existing one, it is essential to follow the presented guidelines. The information sets out limitations and restrictions imposed by isolation demands of the circuit, as well as circuit layout recommendations for optimal operation.

Isolation and Termination

According to the IEEE 802.3af and IEEE802.3at standards, certain isolation requirements need to be met in all PoE equipment. In addition, EMI limitations should be considered, as specified in the FCC and European EN regulations.

These requirements are taken into account by PoE switch vendors while designing the switch circuitry. However, when a PoE Manager is integrated into a switch, special design considerations must be met, due to the unique combination of data and power circuitries.

The following paragraphs define these requirements and provide recommendations for their implementation, so as to assist designers in meeting those requirements and in integrating the Microsemi's PoE Chip Set and the daughter boards.

Isolation

As specified in the IEEE PoE standards, 1500 VAC rms isolation is required between the switch's main board circuitry, including protective and frame ground, and the Media Dependent Interface (MDI). Figure 1 illustrates the overall isolation requirements.

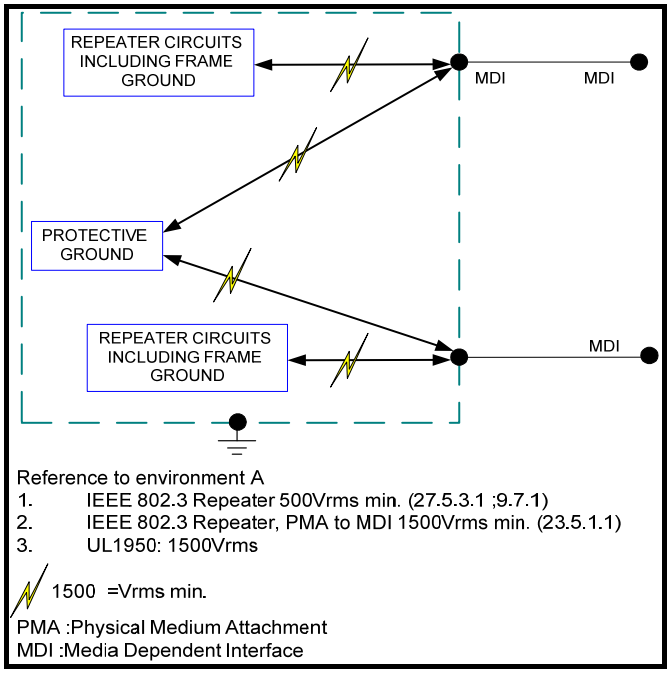

Figure 1: Isolation Requirements Scheme

Meeting Requirements

Hi-voltage Isolation

- For a switch with no PoE circuitry: isolation requirements between the physical inputs and the data connectors are met by using an isolated AC/DC power supply and isolated pulse transformers (see Figure 2).
- When integrating a PoE circuitry into a switch, the output power may be supplied through the central tap of the pulse transformer's secondary side

(unless power is provided over the spare pairs). This connectivity can bypass the pulse transformer's isolation, if the PoE ground or DC input is connected to the switch's circuitry/ground.

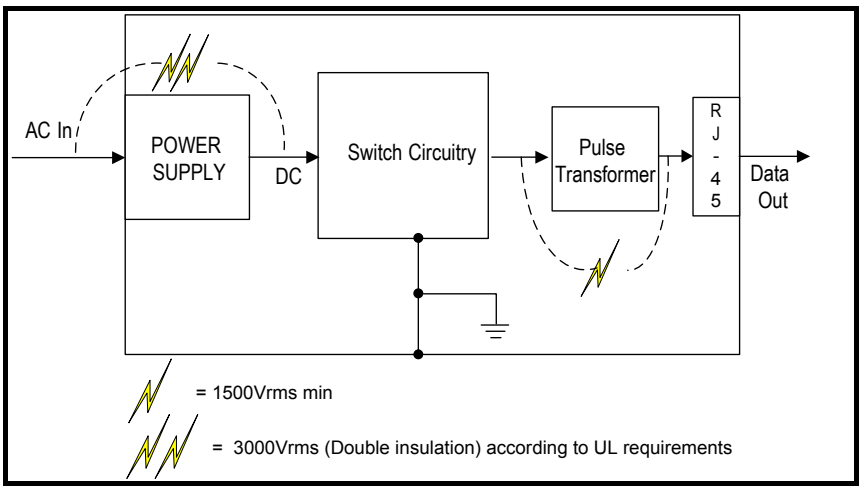

Figure 2: Standard Switch Circuitry

To comply with the above isolation requirements, the PoE Managers must be isolated in regards to all other switch circuitries. One of the following methods is used:

- A separate DC input for the switch and the PoE circuitry and isolated serial communication between the PoE circuitry and the switch circuitry (see Figure 3).
- A single DC input (separate power supplies) for both the switch and PoE circuit; additional or integrated isolated DC-DC circuitry for the switch input and isolated serial communication port between the PoE circuitry and the switch's circuitry (see Figure 4).

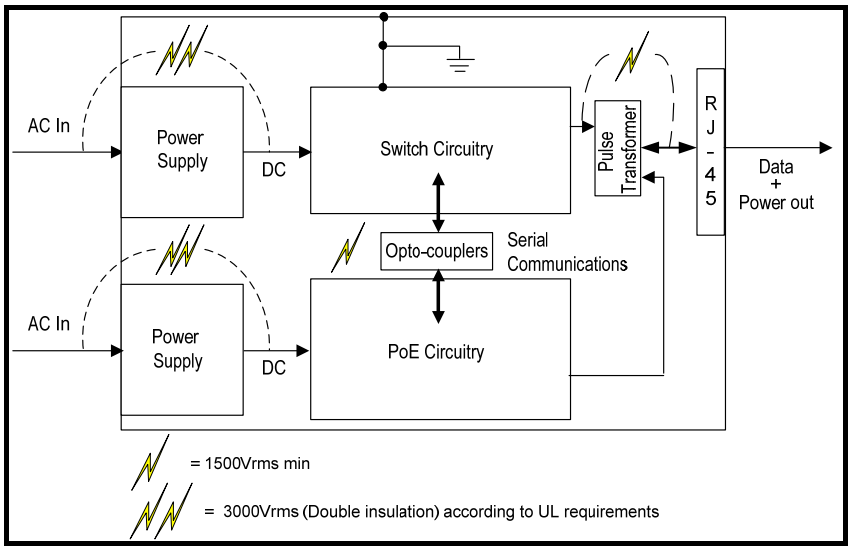

Figure 3: Switch Circuitry with Two DC Sources

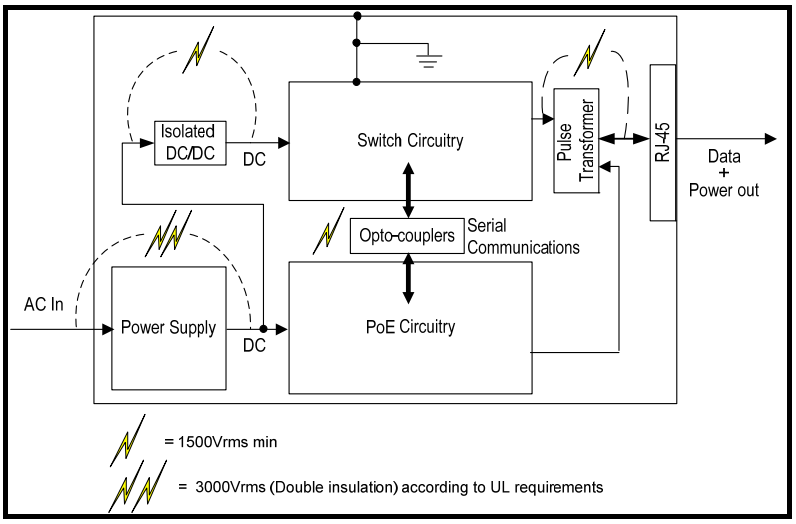

Figure 4: Switch Circuitry with a Single DC Source

To maintain 1500 Vrms isolation between two adjacent layers of a NEMA FR-4 multi-layer PCB, a minimum of 15 mils isolation thickness is recommended to provide a safe margin for hi-pot requirements.

PoE Output Ports Filtering and Terminations

A switch normally creates a noisy environment. To meet EMI requirements, high filtering and line terminations may be needed when connecting the PoE circuit outputs to the switch circuitry (see Figure 5). Note that in most PoE systems, it is recommended to use 0 Ohm resistors for R1 and R2. However, certain systems may benefit from 75 Ohm resistors. It is recommended that filtering provisions are made. Note that in quiet PoE systems the EMI filter can be replaced (bypassed) using R3 and R4.

A circuitry for the recommended filter includes:

- A common mode choke for conducted EMI performances (such as ICE CS01 series)
- Output differential cap filter for radiated EMI performances
- Y-capacitive/resistive network to chassis

Since each system is a unique EMI case, this circuit is a good starting point for EMI suppression.

Note For best EMI performance and to avoid additional noise accumulated on the lines between the filter and the port connectors, it is recommended to place this circuitry on the switch's main board, located as close as possible to the port connectors.

As specified in the IEEE PoE standards, PoE output power can be supplied over the data pairs, or the spare pairs. Figure 6 illustrates both methods in showing an MDI-X (or Auto MDI-X) connection associated with the switch.

Isolating the Stacked Modular Jack Assembly

The IEEE PoE standards require 1500 Vrms isolation between PoE voltages and frame ground (EGND). Notice that RJ-45 jack assemblies have a metal cover that almost reaches to the PCB surface.

Proper traces clearance (at least 80 mils) must be maintained between EGND traces for the RJ-45 modular jack assembly metal covering and adjacent circuit paths and components. To prevent 1500 Vrms isolation violation, provide layout clearances of PoE traces on the top layer, in the vicinity of the RJ-45 connector assemblies.

PoE technology involves voltages as high as 57 VDC. Thus, plan adjacent traces for 100 V operational creepage. Maintain operational creepage to prevent breakdown between traces carrying these potentials.

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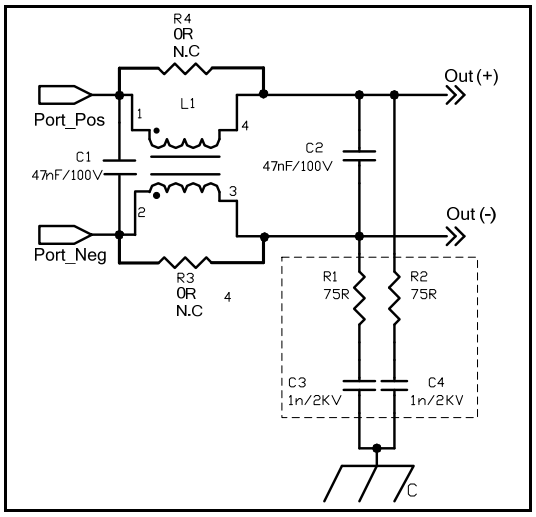

Figure 5: Recommended EMI Filter

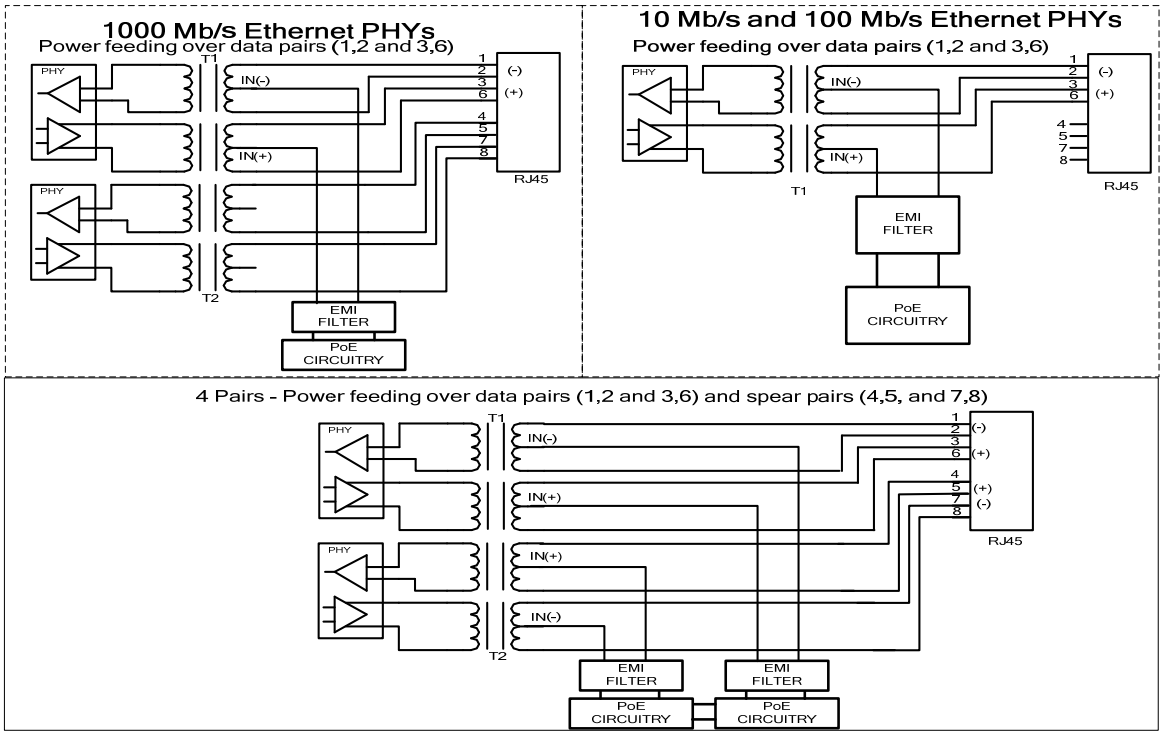

Figure 6: Output Ports Design Details

Layout Guidelines

Microsemi's PD69101 PoE Manager simplifies the integration of PoE-circuitry, based on the IEEE PoE standards, into switches. The pin-out arrangement is configured for optimal PCB routing. Microsemi recommendations for proper PCB layout are as follows:

Figure 7 describes the various circuits and elements surrounding the PD69101 PoE Manager in a block diagram. This block diagram includes the following peripheral elements, identified by numbers:

- 3.3 V and 5 V voltage source (VAUX3P3, VAUX5) (1)
- Sense resistor for current measurement (2)
- Output capacitor – used for filtering (3)

- Protection diode against reverse polarity (4)
- Immunity provision diode (5)

For details on the interconnection circuitry of the PD69101, refer to the application notes listed in the "Applicable Documents" section.

The circuitry provided is intended to facilitate the design of a switch when integrating a PoE capability into it.

Locating PoE Circuitry in a Switch

To minimize the length of high current traces as well as RFI pick-up, place the PoE circuitry as close as possible to the switch's pulse transformers. The circuit can be fully integrated into the switch's PCB, or it can easily be placed on top of the switch using a daughter board PoE application.

Ground and Power Planes

As the Chip Set PoE solution (PD69101) is a mixed-signal (analog and digital) circuitry, special care must be taken when routing the ground and power signals lines. Ground planes are crucial for proper operation and should be designed in accordance with the following guidelines. Observe the following guidelines.

- Separate analog and digital grounds, with a gap of at least 20 mils.
- Due to thermal constraints, the analog ground plane (AGND) must be the first layer after the component side (top layer). The AGND is utilized to transfer the heat generated by the PD69101 (see Thermal Pad Definition and Design)
- If separate layers are used for different grounds or power, try not to overlap the planes; this is done to minimize noise transfer from layer to layer.
- Earth ground is used to tie in the metal frame of the RJ-45 connectors. Route this ground separately and connect it to the switch's metal chassis/enclosure as specified in the isolation requirements (refer to Isolation).
- To prevent ground loop currents, use only a single connection point only between the digital and analog grounds. Make this connection at the "star point" of PD69101 as shown in Figure 7.
- A number of separate grounding areas are essential in the design, to minimize noise effects from the heavy currents flowing to the port. Several separate ground areas are established to concentrate sensitive circuits, apart from the main grounding surfaces.
- To connect various digital ground points (DGND), extend the surface under pins 17 to 24 and pins 1 to 3 of the PD69101 Manager.
- The Rsense resistor for each PoE Manager is connected to the local "star point" on the analog ground (AGND). To achieve this, use a 12 mil diameter power via.
- The Rsense resistor "star point" connection for the PD69101 is the focal interconnection point for the digital and analog grounds (see Figure 7)
- Leave space for ceramic 1 nF bypass capacitors (Cb) between the analog and digital layers near the PoE Manager. The capacitors form low impedance paths for digital driving signals.
- Good design practice is to leave appropriate spacing (provision for) for two parallel and inversed Schottky diodes between the analog and digital layers near PoE Manager. The diodes form low impedance paths for highly energized signals running between analog and digital layers and enhance circuit immunity.
- The power plane for the Vmain input must be designed to carry 2 A continuous current, based on full 2-port capacity in case of a 4-pairs application and 1 A for a 2-pairs application. Minimize DC power losses on this plane by using a wide copper land.

Current Flow Through the PoE Application

The port's current flows in a DC disconnect application is as follows:

- Coming from the switch's power supply to the line transformer center tap

- From the center tap through the switch's RJ45 to the PD side
- The current from the PD flows through the RJ45 and through the line transformer to the PoE circuitry.
- From the analog ground (AGND) back to the switch's power supply

Note The port's heavy current goes directly to the PD side without going through the PoE Managers.

Specific Component Placement

Peripheral Components

To prevent heat transfer among various components, the following gaps should be maintained:

- Leave an open gap in the ground plan to isolate the heat transfer.
- The spacing between the sense resistors to the PD69101 should be as short as possible for accurate operation

PD69012 PoE Manager and Peripherals

- The side of the PD69101 that includes pins 17 to 24 and pins 1 to 3 functions as communication and control pins for the Manager; that side should face the digital ground.
- Locate bypass capacitors for the PoE Manager operating voltages close to the relevant pins. In cases where two bypass capacitors are placed on the same line:
  - Locate the lower value capacitor closest to the pin on the same layer
  - The higher value capacitor can be located at a more distant location

Conductor Routing

General Guidelines

Conductor (or printed lands) routing is to be performed as practiced in general layout guidelines:

- Conductors that deliver a digital signal are to be routed above the digital ground plane.
- Avoid routing analog signals above the digital GND as much as possible.
- The signal PORT_SENSE is layout sensitive.

Specific Requirements for Sensitive Signals

Issues that require special design considerations:

- Route the PORT_SENSE (pin 10) to AGND and connect a trace from QGND to the local PoE Manager “star point” (AGND). Connect the PD69101 AGND (pin 7) directly to the local PoE Manager “star point” by individual traces.
- Place the 4.7 µF and 1 µF bypass capacitors (item-1 in Figure 7) from VAUX3P3 and VAUX5 to AGND as close as possible to the respective pins. Its conductors to VAUX3P3, VAUX5 and pin 7 should be as short as possible.
- Connect the IREF resistor (connects to pin 12), used for current reference, directly to QGND (pin 11).
- PD69101 port incorporates a current sense resistor. For proper power management and control, these lines are to be laid out in such a way that measured current is not impeded by excessive path resistance. To achieve this, use a single common point to aggregate the current flow to the analog ground (AGND) layer. This point is referred to as the local PoE Manager "star point". It is critical to design the total layout path (traces resistance from PORT_SENSE pin to the AGND star point) using an accurate resistance value, since an incorrect resistance value results in current measurement error and un-reliable power management. Parasitic resistance added by the layout traces must be planned for value of ~5 mΩ (at room temperature). The total resistance from PORT_SENSE pin to the AGND star point should be ~505 mΩ.

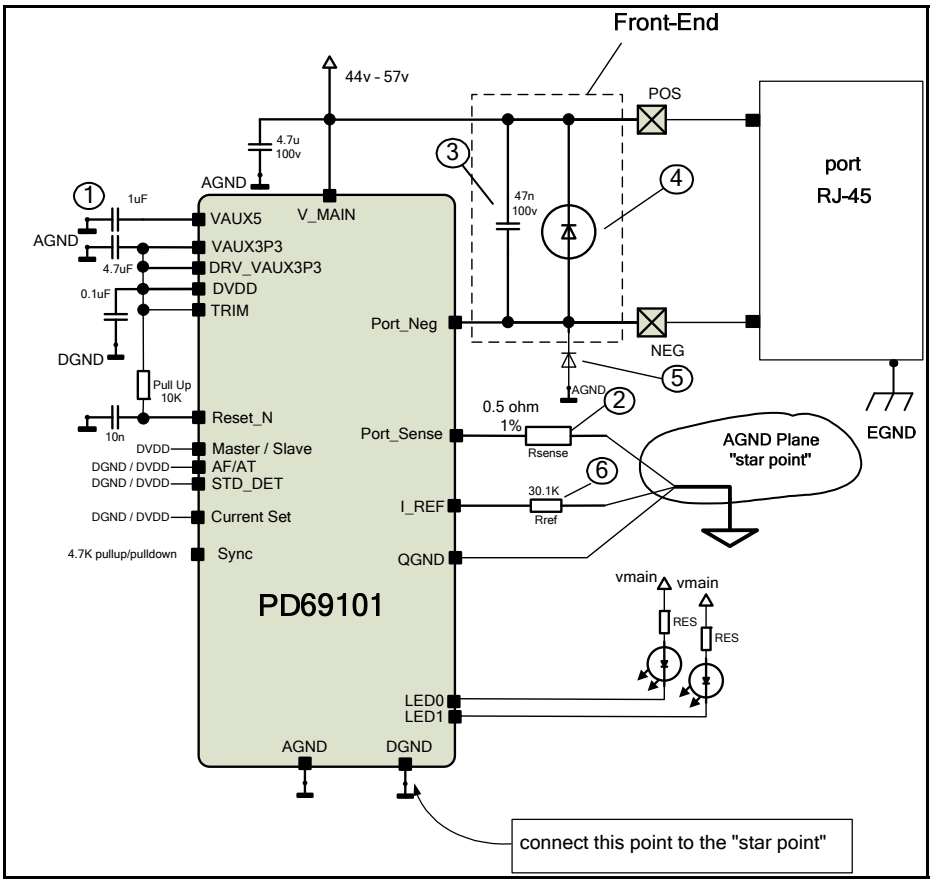

Figure 7: Component Identification for PD69101 Circuitry

Port Outputs

For robust design, the port output traces are to be 45-mil wide so as to handle maximum current and port power. However to obtain maximum 10° C copper rise, minimum width for traces is set in accordance with the layer location and copper thickness:

- For 2-ounce copper, external layer: 15 mils
- For 2-ounce copper, internal layer: 20 mils
- For one-ounce copper, external layer: 25 mils
- For one-ounce copper, internal layer: 30 mils
- For 1/2-ounce copper, external layer: 30 mils
- For 1/2-ounce copper, internal layer: 55 mils (20° C copper rise)

The port output traces must be short and parallel to each other, to reduce RFI coupling and to keep the series resistance low.

Output Ports Interconnections

The PoE ports outputs must be connected to the switch's pulse transformers as shown in Figure 6. The common mode choke is used to reduce RFI noise. A 'Bob-Smith' termination (resistor-capacitor) to chassis ground is optional.

Place the circuit as close as possible to the pulse transformer.

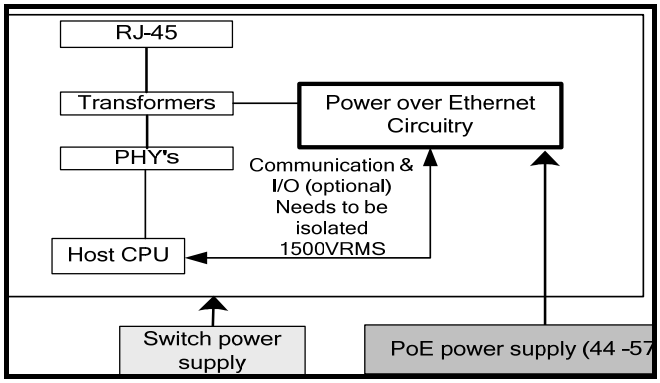

Figure 8: Block Diagram - PoE Circuitry inside the Switch

Thermal Pad Definition and Design

The PD69101 utilizes a thermal dissipation exposed pad in a 24-lead QFN package. The package is molded in such a way that the lead frame is exposed at the bottom surface of the package.

Direct soldering of the exposed pad to a copper land provides an efficient thermal path.

In multilayer board designs, thermal vias connect the exposed pad to the internal copper planes thermally.

Requirements

The PCB design should consider the exposed pad of the PD69101, which is used for thermal cooling of the package. The PCB should be designed as shown in Figure 9. The PD69101 pad is soldered to a dedicated area on the PCB.

This contact area is composed of a 12 vias array, each penetrating and thermally connecting to large ground areas in the PCB at various planes, for efficient heat dissipation.

To ensure optimum thermal transfer through the thermal vias to internal planes or to the reverse side of the PCB, the vias system **should not** be used as used in web construction techniques. Web construction for PCB vias is a standard technique used to facilitate soldering, by designing the via to achieve high thermal resistance. This is not desirable for heat dissipation from the PD69101 package.

Connect the vias used under the PD69101 package internally connected to the planes, using a continuous connection surrounding the diameter.

Thermal Pad Design

The PD69101 is packaged in a 24 QFN type package with an exposed pad. This exposed pad is a metal substrate on the bottom of the package.

The attachment process for exposed pad package is equivalent to standard surface mount packages.

See Figure 13 and Figure 14 (CS & PS) for a design layout of the recommended contact pad.

For proper heat dissipation, the following footprint / layout guidelines must be followed:

- Connect all thermal vias to the AGND area under the PD69101
- To allow for the lowest possible heat resistance, the AGND copper area must be the first layer under the PoE Manager.

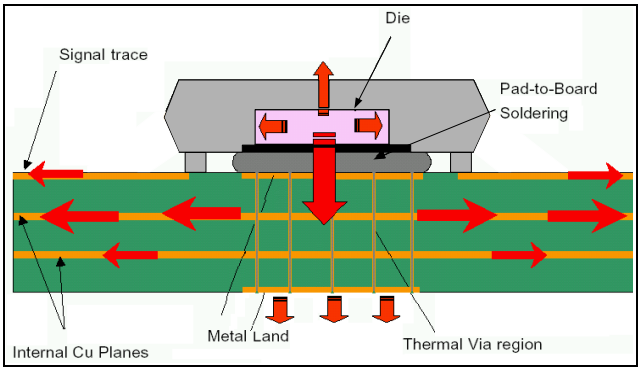

Figure 9: Heat Dissipation in PC

Via diameter should be approximately 0.3 mm with 1-ounce copper barrel plating. Solder flow into the vias from the component side may result in voids during the solder process and this must be avoided.

If copper plating does not plug the vias, apply stencil print solder paste onto the printed circuit side. This provides sufficient solder paste filling those vias to avoid the above mentioned voids.

Figure 14 and Figure 15 show the associated, solder printing paste masks (CS & PS). The solder printing paste mask openings are lined-up in respect to the 3 x 4 thermal via array.

Since large solder printing paste metal mask openings may result in poor release, the opening should be subdivided as shown in these figures.

For a nominal package standoff of 0.1 mm, a solder paste metal mask stencil thickness of 5 mils should be considered.

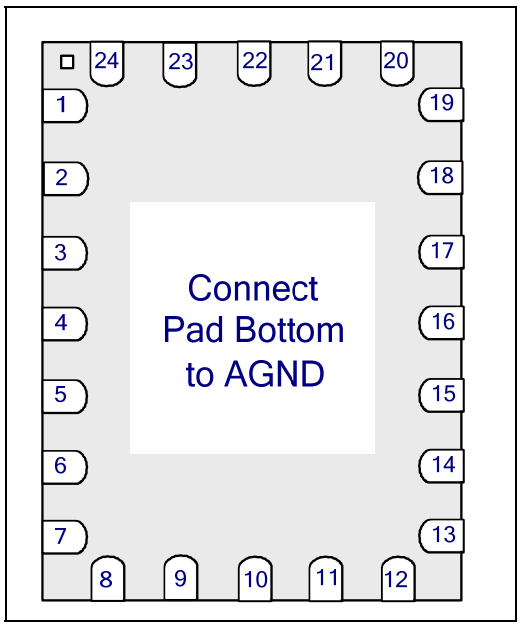

Figure 10: PD69101 TOP View

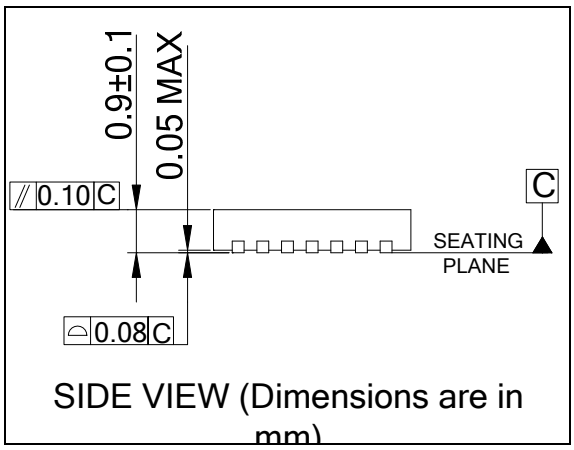

Figure 12: PD69101 Side View

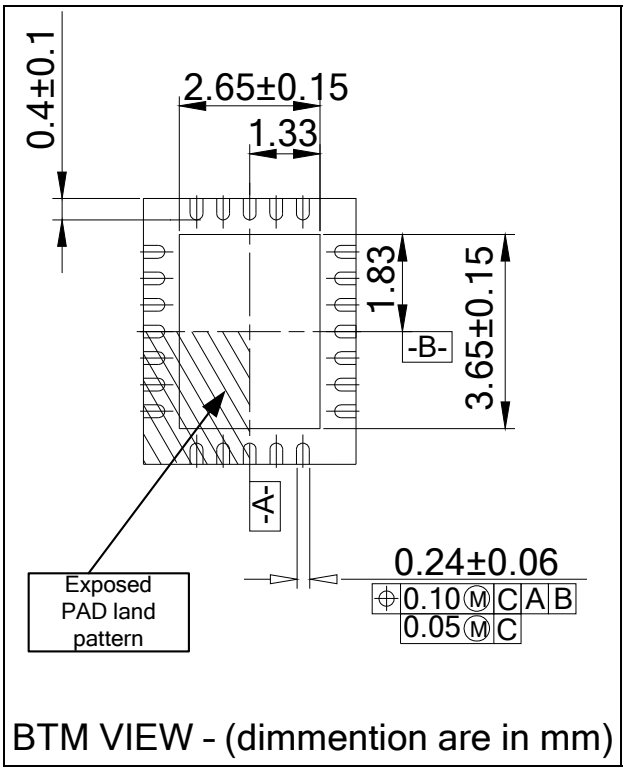

Figure 11: Recommended PCB Layout- Thermal Pad Footprint (CS)

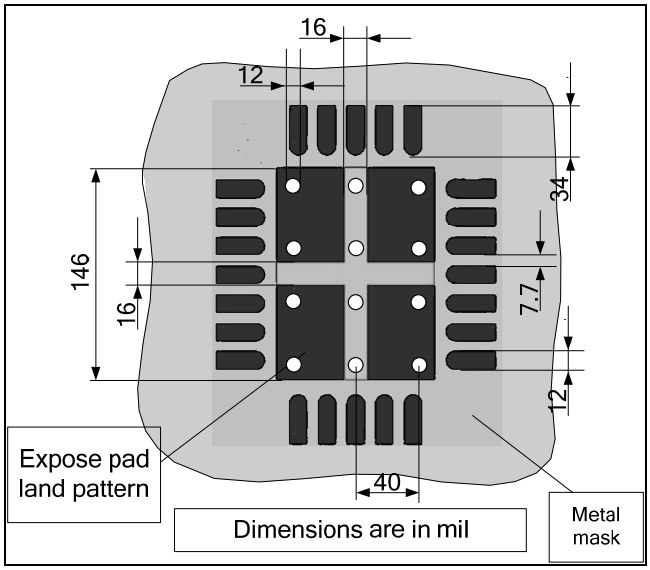

Figure 13 : Recommended Solder Printing Paste Mask Apertures (CS)

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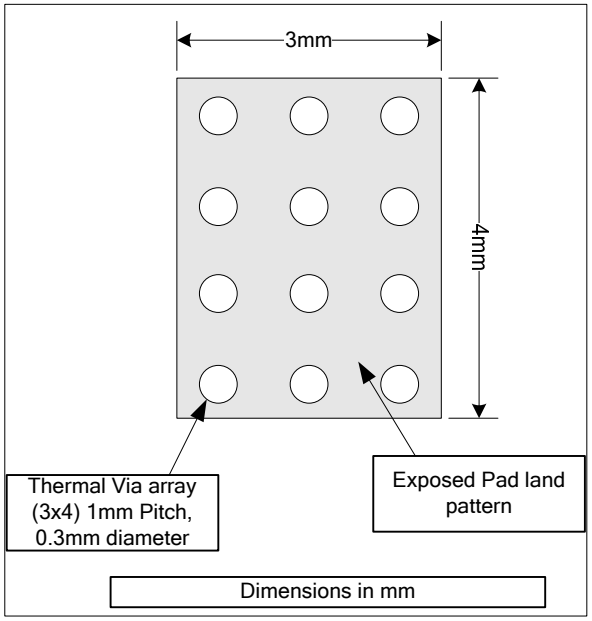

Figure 14: Recommended PCB layout for Thermal Pad Array Footprint (PS)

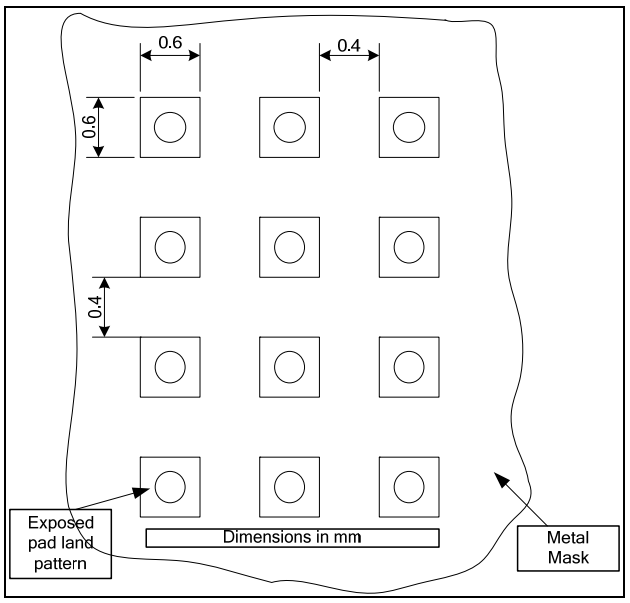

Figure 16: Recommended Solder Printing Paste Mask Apertures (PS)

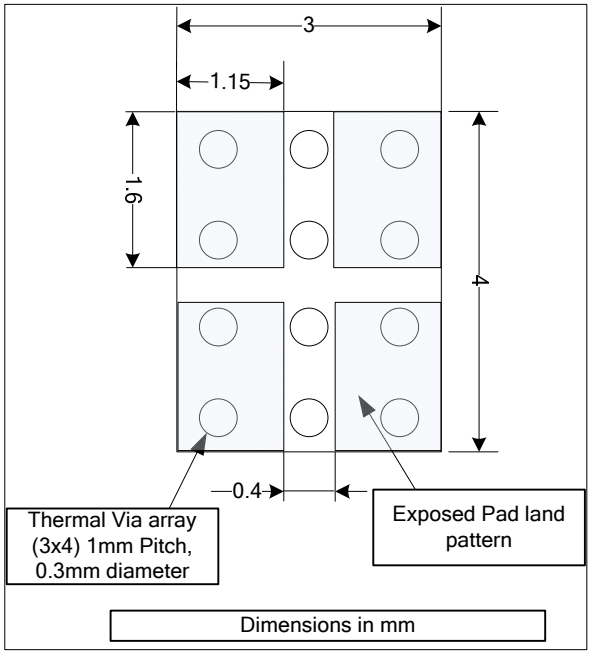

Figure 15: Recommended Solder Printing Paste Mask Apertures (CS)

Revision History

Revision Level / Date	Para. Affected	Description
0.1 / 31 May. 08		Initial release
0.2 / 31 June. 08	Whole document	General modifications as a result of development
0.3 / 31 August. 08	Overhaul maintenance	Figures 2, 3 and 4 replaced
0.4 / 25 November. 08	P1, P9	Figures 10, 11 and 12 replaced, draft 3.0 modified to draft 3.2
0.5 / 25 April 10		

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