

## IRS2308(S)PbF

### HALF-BRIDGE DRIVER

#### Features

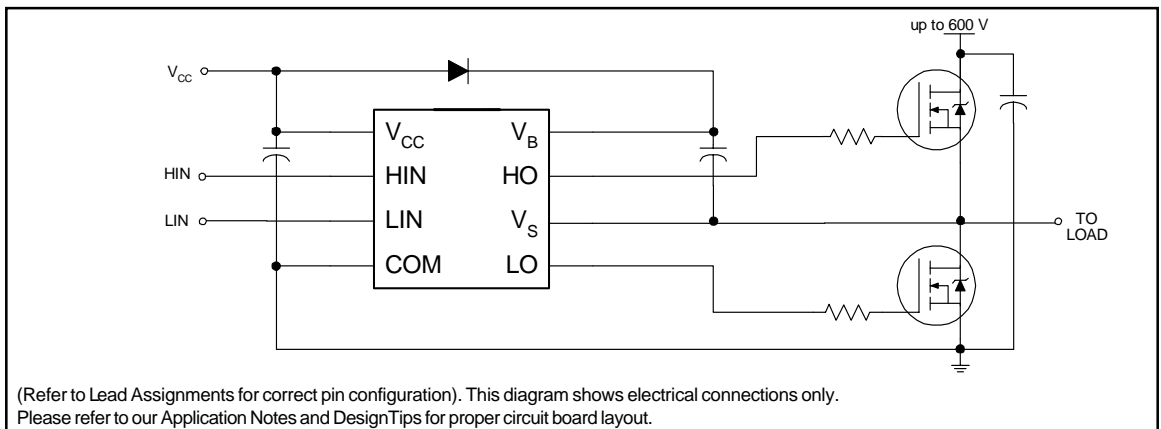
- Floating channel designed for bootstrap operation
- Fully operational to +600 V
- Tolerant to negative transient voltage, dV/dt immune
- Gate drive supply range from 10 V to 20 V
- Undervoltage lockout for both channels
- 3.3 V, 5 V, and 15 V input logic compatible
- Cross-conduction prevention logic
- Matched propagation delay for both channels
- Outputs in phase with inputs
- Logic and power ground +/- 5 V offset.
- Internal 540 ns deadtime
- Lower di/dt gate driver for better noise immunity
- RoHS compliant

#### Description

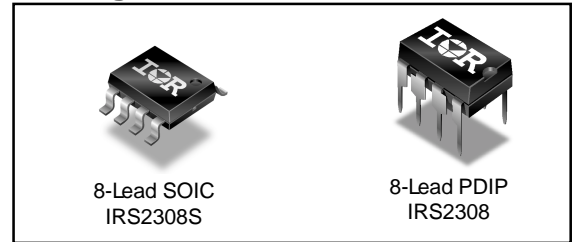
The IRS2308/IRS23084 are high voltage, high speed power MOSFET and IGBT drivers with dependent high-side and low-side referenced output channels. Proprietary HVIC and latch immune CMOS technologies enable ruggedized monolithic construction. The logic input

is compatible with standard CMOS or LSTTL output, down to 3.3 V logic. The output drivers feature a high pulse current buffer stage designed for minimum driver cross-conduction. The floating channel can be used to drive an N-channel power MOSFET or IGBT in the high-side configuration which operates up to 600 V.

#### Typical Connection



#### Packages



#### Feature Comparison

Part	Input logic	Cross-conduction prevention logic	Deadtime (ns)	Ground Pins	ton/t <sub>off</sub> (ns)
2106	HIN/LIN	no	none	COM	220/200
21064				V <sub>ss</sub> /COM	
2108				COM	
21084	HIN/LIN	yes	Internal 540	V <sub>ss</sub> /COM	220/200
2109	IN/SD	yes	Programmable 540 - 5000	COM	
21094			Internal 540	V <sub>ss</sub> /COM	750/200
2304	HIN/LIN	yes	Internal 100	COM	160/140
2308	HIN/LIN	yes	Internal 540	COM	220/200

## Absolute Maximum Ratings

Absolute maximum ratings indicate sustained limits beyond which damage to the device may occur. All voltage parameters are absolute voltages referenced to COM. The thermal resistance and power dissipation ratings are measured under board mounted and still air conditions.

Symbol	Definition	Min.	Max.	Units	
V <sub>B</sub>	High-side floating absolute voltage	-0.3	625	V	
V <sub>S</sub>	High-side floating supply offset voltage	V <sub>B</sub> - 25	V <sub>B</sub> + 0.3		
V <sub>HO</sub>	High-side floating output voltage	V <sub>S</sub> - 0.3	V <sub>B</sub> + 0.3		
V <sub>CC</sub>	Low-side and logic fixed supply voltage	-0.3	25		
V <sub>LO</sub>	Low-side output voltage	-0.3	V <sub>CC</sub> + 0.3		
V <sub>IN</sub>	Logic input voltage (HIN & LIN )	V <sub>SS</sub> - 0.3	V <sub>CC</sub> + 0.3		
dV <sub>S</sub> /dt	Allowable offset supply voltage transient	—	50	V/ns	
P <sub>D</sub>	Package power dissipation @ T <sub>A</sub> ≤ +25 °C	(8 lead PDIP)	—	1.0	W
		(8 lead SOIC)	—	0.625	
R <sub>thJA</sub>	Thermal resistance, junction to ambient	(8 lead PDIP)	—	125	°C/W
		(8 lead SOIC)	—	200	
T <sub>J</sub>	Junction temperature	—	150	°C	
T <sub>S</sub>	Storage temperature	-50	150		
T <sub>L</sub>	Lead temperature (soldering, 10 seconds)	—	300		

## Recommended Operating Conditions

The input/output logic timing diagram is shown in Fig. 1. For proper operation the device should be used within the recommended conditions. The V<sub>S</sub> and V<sub>SS</sub> offset rating are tested with all supplies biased at a 15 V differential.

Symbol	Definition	Min.	Max.	Units
V <sub>B</sub>	High-side floating supply absolute voltage	V <sub>S</sub> + 10	V <sub>S</sub> + 20	V
V <sub>S</sub>	High-side floating supply offset voltage	Note 1	600	
V <sub>HO</sub>	High-side floating output voltage	V <sub>S</sub>	V <sub>B</sub>	
V <sub>CC</sub>	Low-side and logic fixed supply voltage	10	20	
V <sub>LO</sub>	Low-side output voltage	0	V <sub>CC</sub>	
V <sub>IN</sub>	Logic input voltage	COM	V <sub>CC</sub>	
T <sub>A</sub>	Ambient temperature	-40	125	°C

Note 1: Logic operational for V<sub>S</sub> of -5 V to +600 V. Logic state held for V<sub>S</sub> of -5 V to -V<sub>BS</sub>. (Please refer to the Design Tip DT97-3 for more details).

## Dynamic Electrical Characteristics

V<sub>BIAS</sub> (V<sub>CC</sub>, V<sub>BS</sub>) = 15 V, V<sub>SS</sub> = COM, C<sub>L</sub> = 1000 pF, T<sub>A</sub> = 25 °C, DT = V<sub>SS</sub> unless otherwise specified.

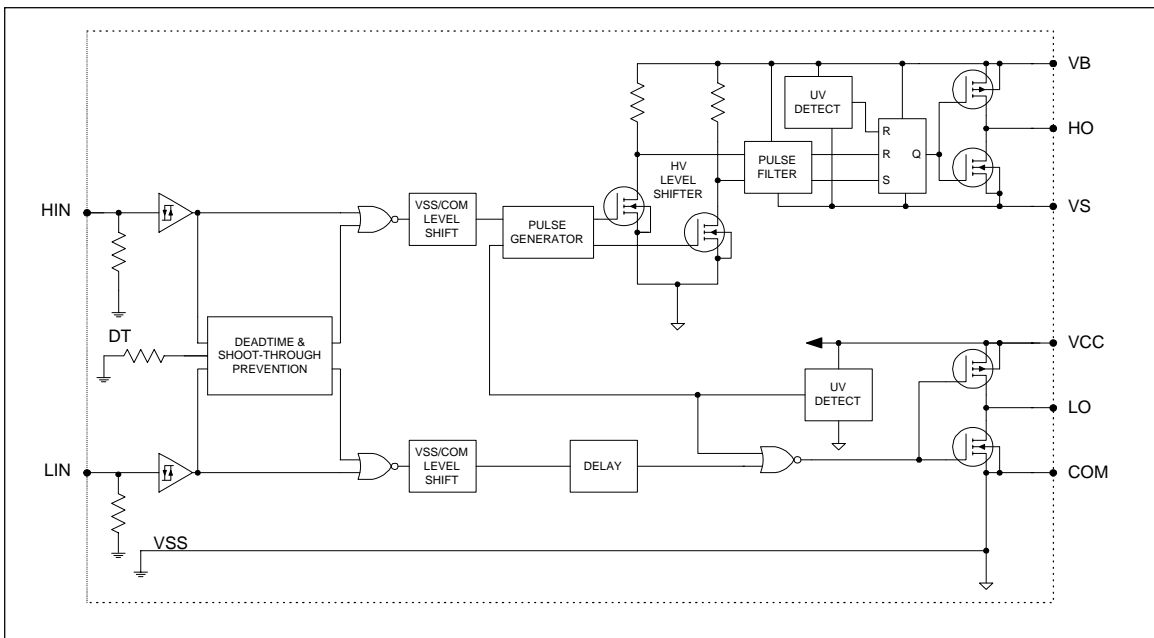
Symbol	Definition	Min.	Typ.	Max.	Units	Test Conditions
t <sub>on</sub>	Turn-on propagation delay	—	220	300	ns	V <sub>S</sub> = 0 V
t <sub>off</sub>	Turn-off propagation delay	—	200	280		V <sub>S</sub> = 0 V or 600 V
MT	Delay matching   t <sub>on</sub> - t <sub>off</sub>	—	0	46		
t <sub>r</sub>	Turn-on rise time	—	100	220		V <sub>S</sub> = 0 V
t <sub>f</sub>	Turn-off fall time	—	35	80		
DT	Deadtime: LO turn-off to HO turn-on(DT <sub>LO-HO</sub> ) & HO turn-off to LO turn-on (DT <sub>HO-LO</sub> )	400	540	680		
MDT	Deadtime matching =   DT <sub>LO-HO</sub> - DT <sub>HO-LO</sub>	—	0	60		

## Static Electrical Characteristics

V<sub>BIAS</sub> (V<sub>CC</sub>, V<sub>BS</sub>) = 15 V, V<sub>SS</sub> = COM, DT = V<sub>SS</sub> and T<sub>A</sub> = 25 °C unless otherwise specified. The V<sub>IL</sub>, V<sub>IH</sub>, and I<sub>IN</sub> parameters are referenced to V<sub>SS</sub>/COM and are applicable to the respective input leads: HIN and LIN. The V<sub>O</sub>, I<sub>O</sub>, and R<sub>on</sub> parameters are referenced to COM and are applicable to the respective output leads: HO and LO.

Symbol	Definition	Min.	Typ.	Max.	Units	Test Conditions
V <sub>IH</sub>	Logic "1" input voltage for HIN & LIN	2.5	—	—	V	V <sub>CC</sub> = 10 V to 20 V I <sub>O</sub> = 2 mA
V <sub>IL</sub>	Logic "0" input voltage for HIN & LIN	—	—	0.8		
V <sub>OH</sub>	High level output voltage, V <sub>BIAS</sub> - V <sub>O</sub>	—	0.05	0.2		
V <sub>OL</sub>	Low level output voltage, V <sub>O</sub>	—	0.02	0.1		
I <sub>LK</sub>	Offset supply leakage current	—	—	50	μA	V <sub>B</sub> = V <sub>S</sub> = 600 V
I <sub>QBS</sub>	Quiescent V <sub>BS</sub> supply current	20	60	150	mA	V <sub>IN</sub> = 0 V or 5 V
I <sub>QCC</sub>	Quiescent V <sub>CC</sub> supply current	0.4	1.0	1.6		
I <sub>IN+</sub>	Logic "1" input bias current	—	5	20	μA	HIN = 5 V, LIN = 5 V
I <sub>IN-</sub>	Logic "0" input bias current	—	1	5		HIN = 0 V, LIN = 0 V
V <sub>CCUV+</sub> V <sub>B SUV+</sub>	V <sub>CC</sub> and V <sub>BS</sub> supply undervoltage positive going threshold	8.0	8.9	9.8	V	
V <sub>CCUV-</sub> V <sub>B SUV-</sub>	V <sub>CC</sub> and V <sub>BS</sub> supply undervoltage negative going threshold	7.4	8.2	9.0		
V <sub>CCUVH</sub> V <sub>B SUVH</sub>	Hysteresis	0.3	0.7	—		
I <sub>O+</sub>	Output high short circuit pulsed current	97	290	—	mA	V <sub>O</sub> = 0 V, PW ≤ 10 μs
I <sub>O-</sub>	Output low short circuit pulsed current	250	600	—		V <sub>O</sub> = 15 V, PW ≤ 10 μs

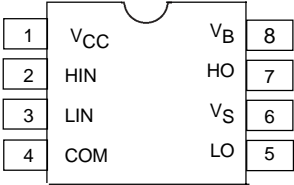
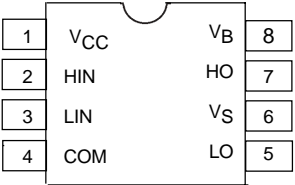
**Functional Block Diagram**



## Lead Definitions

Symbol	Description
HIN	Logic input for high-side gate driver output (HO), in phase
LIN	Logic input for low-side gate driver output (LO), in phase
V <sub>B</sub>	High-side floating supply
HO	High-side gate driver output
V <sub>S</sub>	High-side floating supply return
V <sub>CC</sub>	Low-side and logic fixed supply
LO	Low-side gate driver output
COM	Low-side return

## Lead Assignments

 <p>8 Lead PDIP</p>	 <p>8 Lead SOIC</p>
<b>IRS2308PbF</b>	<b>IRS2308SPbF</b>

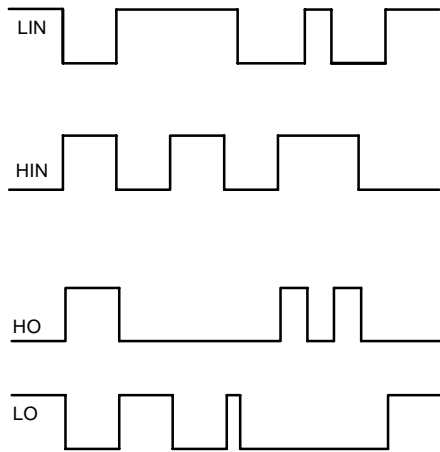


Figure 1. Input/Output Timing Diagram

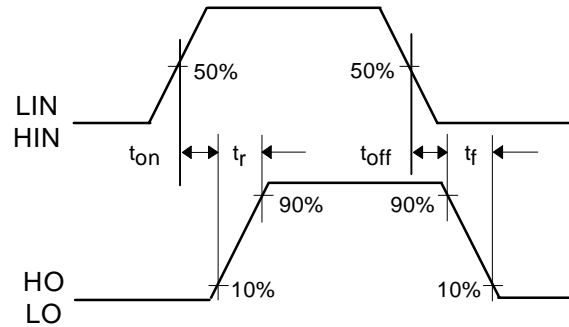


Figure 2. Switching Time Waveform Definitions

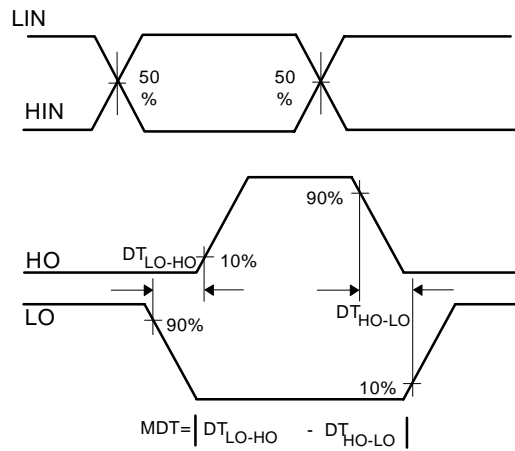
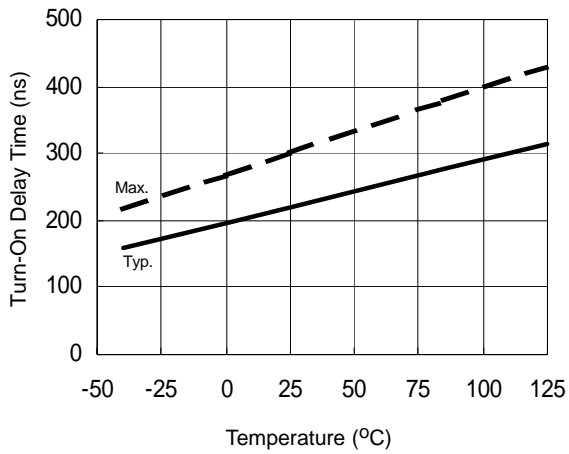
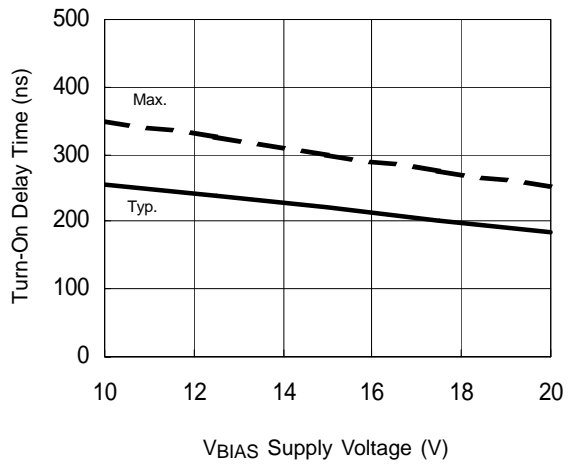


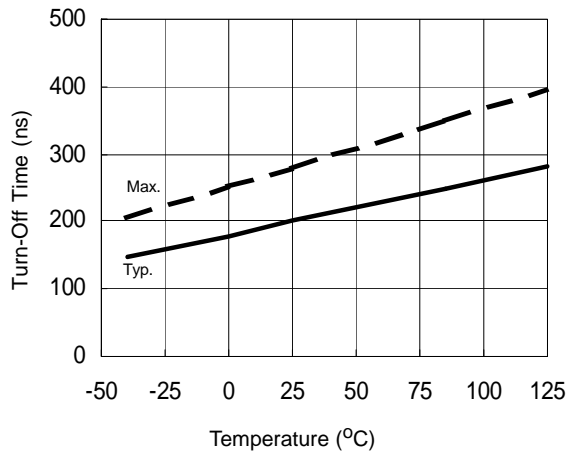
Figure 3. Deadtime Waveform Definitions



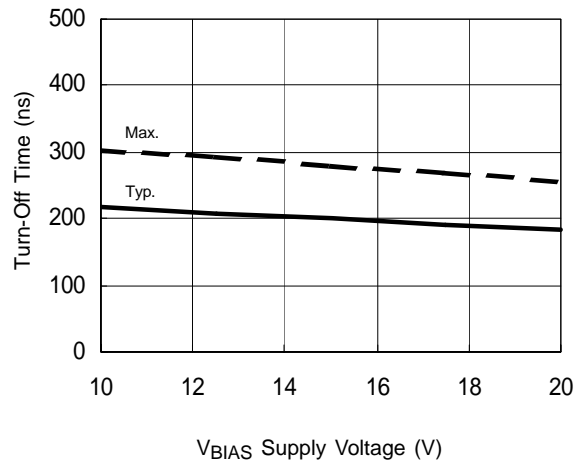
**Figure 4A. Turn-On Time vs. Temperature**



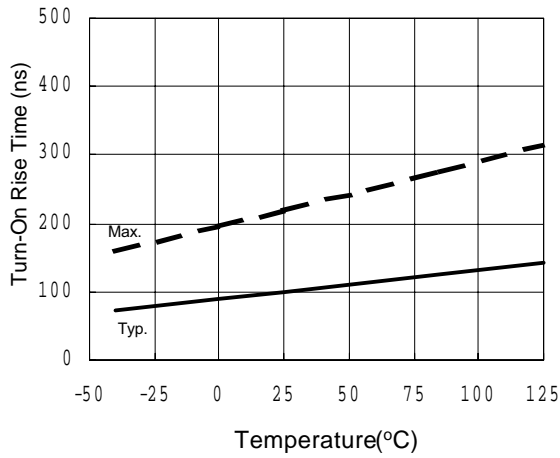
**Figure 4B. Turn-On Time vs. Supply Voltage**



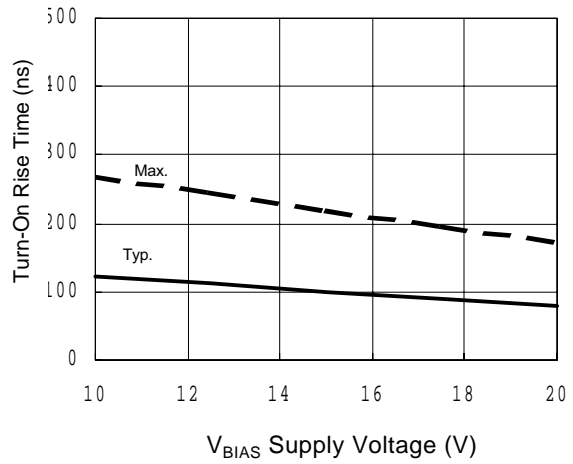
**Figure 5A. Turn-Off Propagation Delay vs. Temperature**



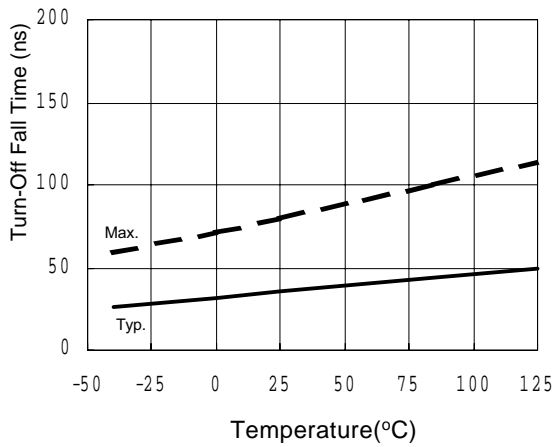
**Figure 5B. Turn-Off Propagation Delay vs. Supply Voltage**



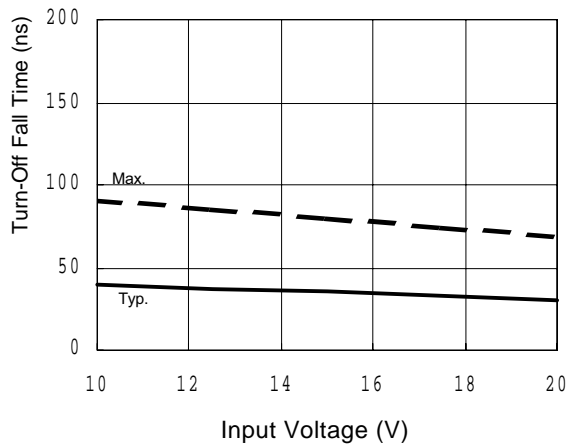
**Figure 6A. Turn-On Rise Time vs. Temperature**



**Figure 6B. Turn-On Rise Time vs. Supply Voltage**

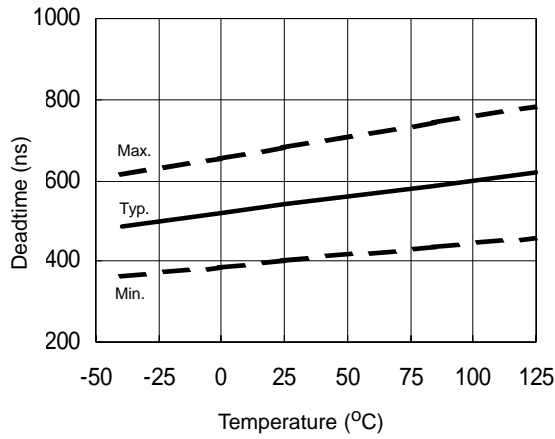


**Figure 7A. Turn-Off Fall Time vs. Temperature**

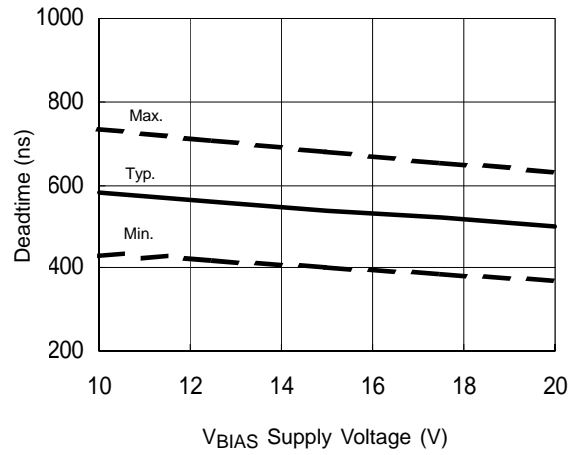


**Figure 7B. Turn-Off Fall Time vs. Supply Voltage**

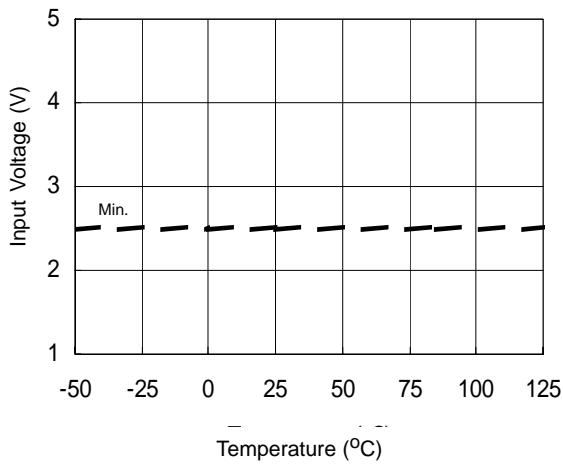




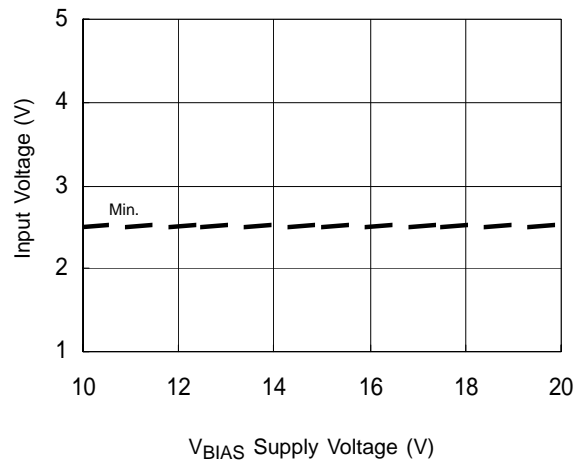
**Figure 8A. Deadtime vs. Temperature**



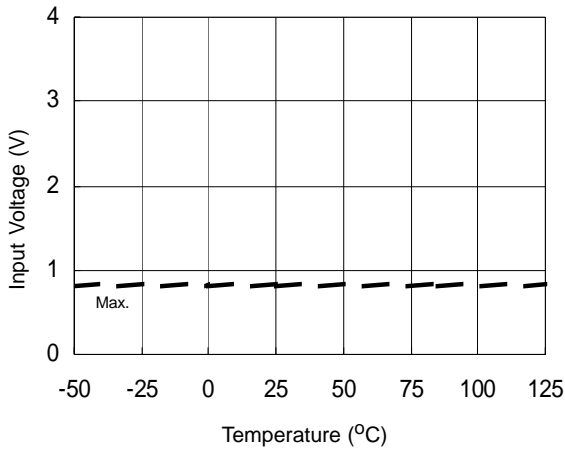
**Figure 8A. Deadtime vs. Supply Voltage**



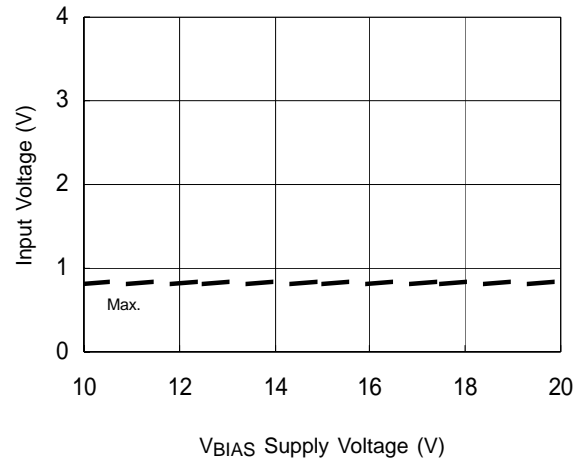
**Figure 9A. Logic "1" Input Voltage vs. Temperature**



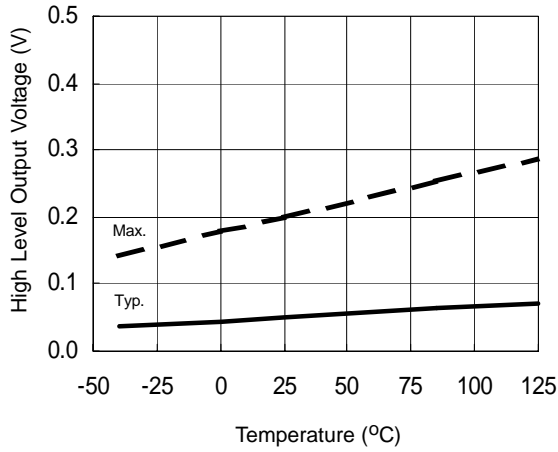
**Figure 9B. Logic "1" Input Voltage vs. Supply Voltage**



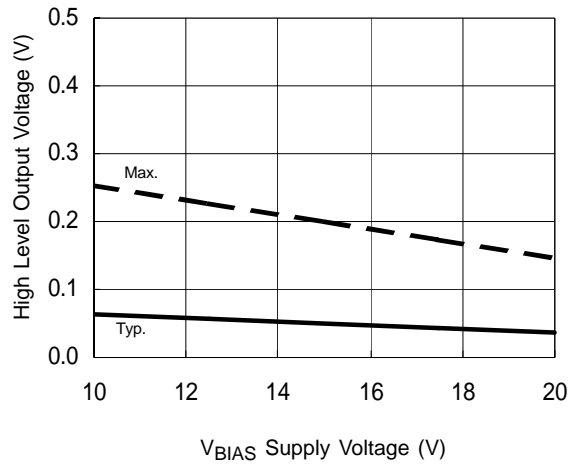
**Figure 10A. Logic "0" Input Voltage vs. Temperature**



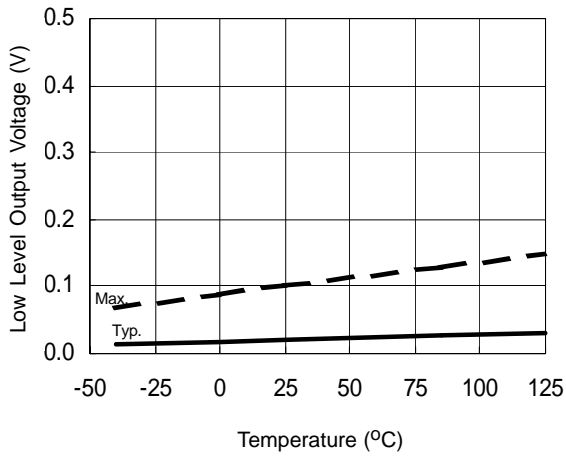
**Figure 10A. Logic "0" Input Voltage vs. Supply Voltage**



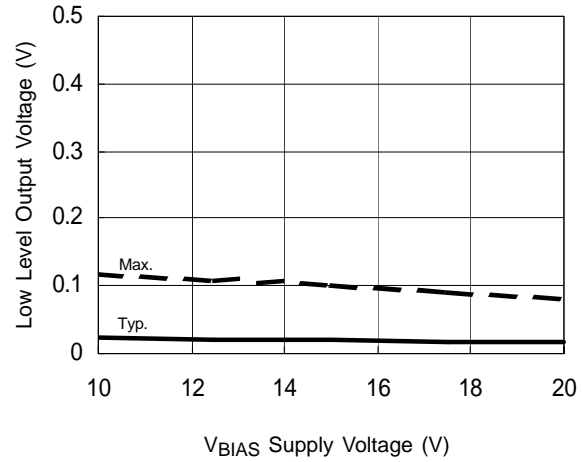
**Figure 11A. High Level Output Voltage vs. Temperature**



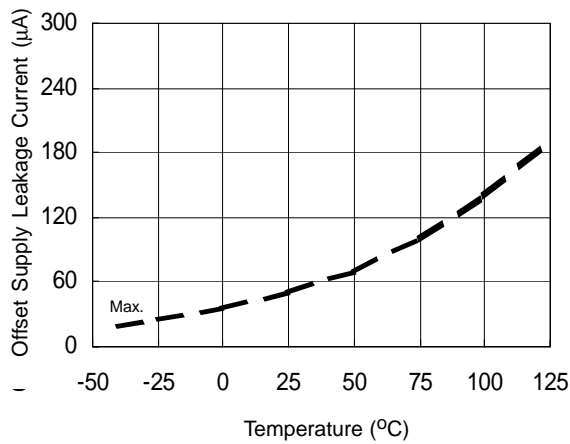
**Figure 11A. High Level Output Voltage vs. Supply Voltage**



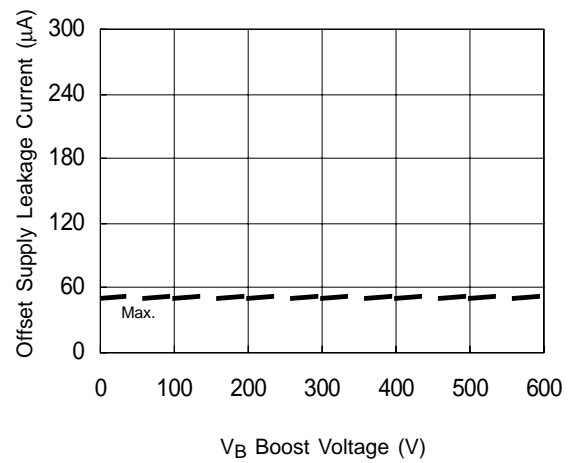
**Figure 12A. Low Level Output Voltage vs. Temperature**



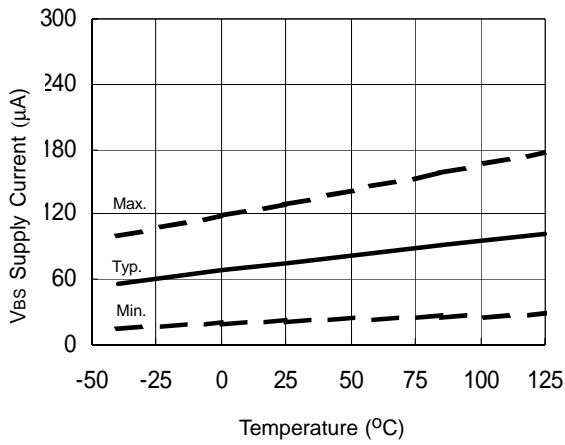
**Figure 12B. Low Level Output Voltage vs. Supply Voltage**



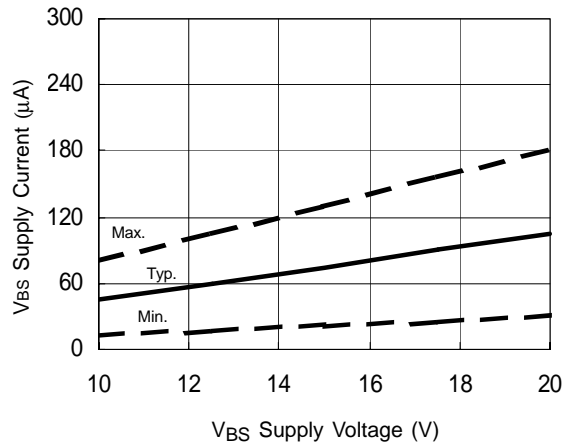
**Figure 13A. Offset Supply Leakage Current vs. Temperature**



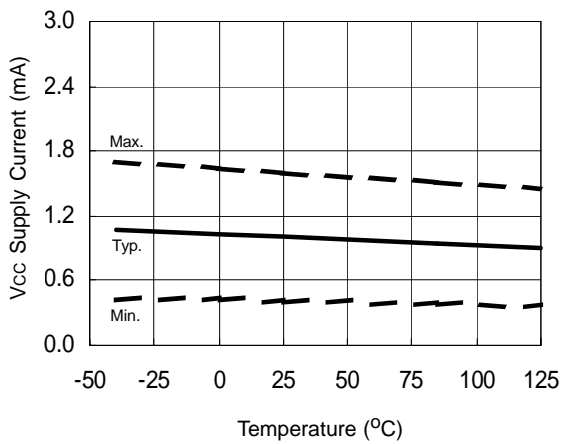
**Figure 13B. Offset Supply Leakage Current vs. Supply Voltage**



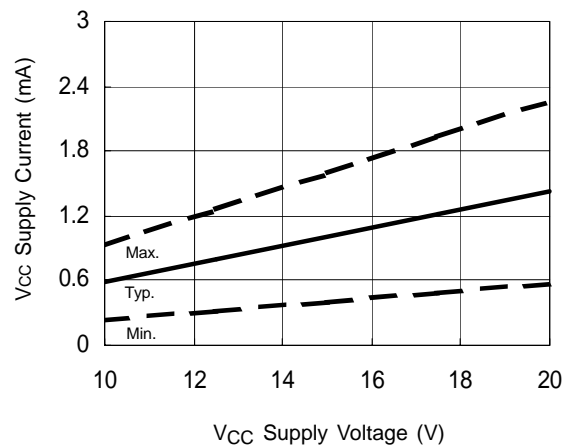
**Figure 14A.  $V_{BS}$  Supply Current vs. Temperature**



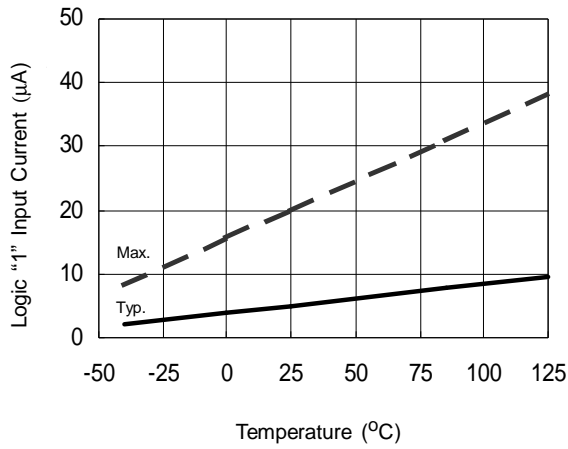
**Figure 14B.  $V_{BS}$  Supply Current vs. Supply Voltage**



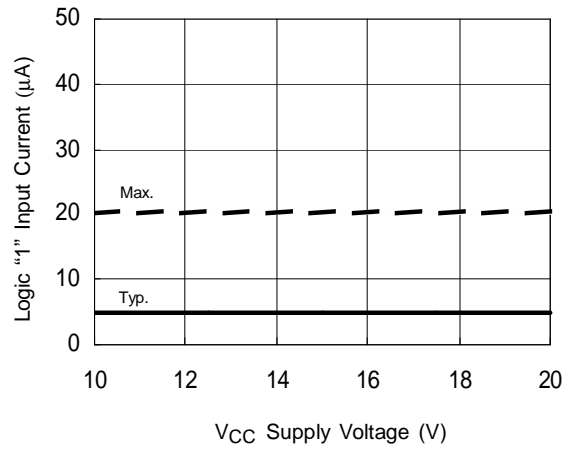
**Figure 15A.  $V_{CC}$  Supply Current vs. Temperature**



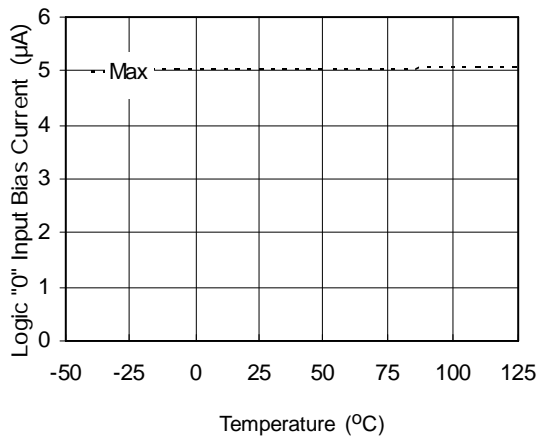
**Figure 14B.  $V_{CC}$  Supply Current vs. Supply Voltage**



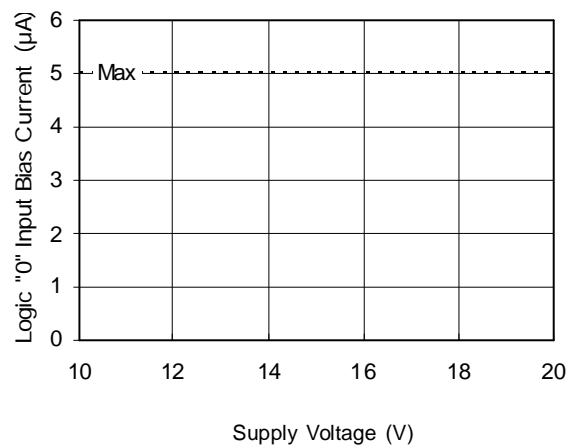
**Figure 16A. Logic "1" Input Current vs. Temperature**



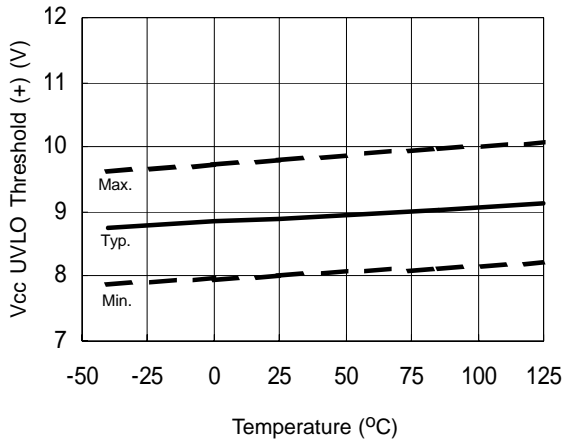
**Figure 16B. Logic "1" Input Current vs. Supply Voltage**



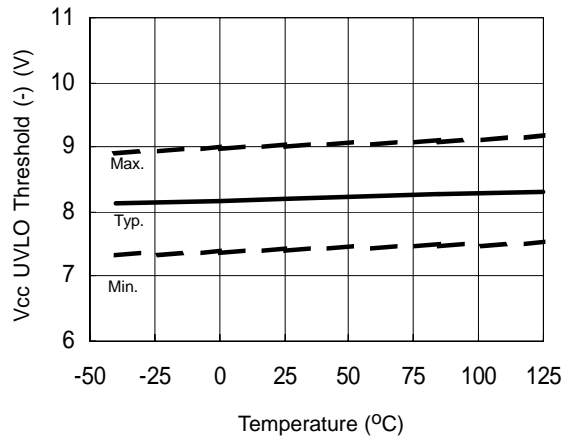
**Figure 17A. Logic "0" Input Bias Current vs. Temperature**



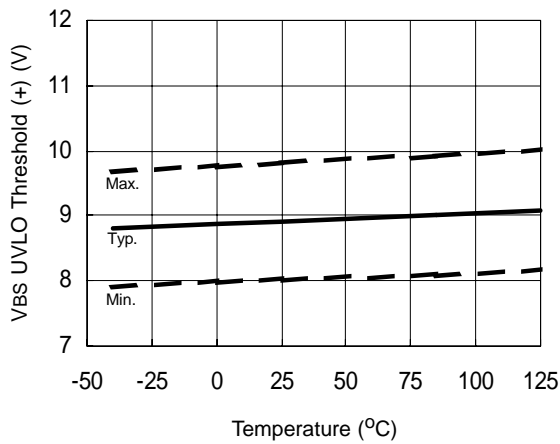
**Figure 17B. Logic "0" Input Bias Current vs. Supply Voltage**



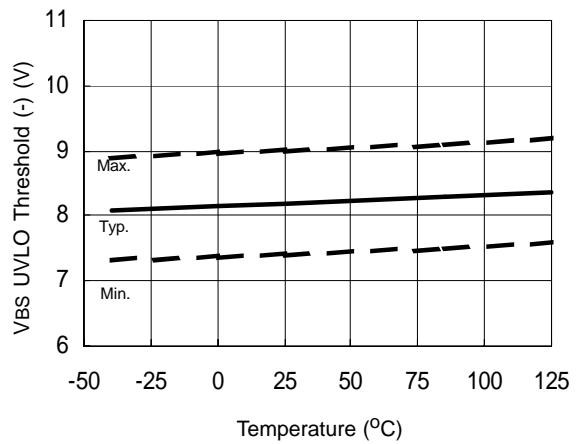
**Figure 18. V<sub>CC</sub> Undervoltage Threshold (+) vs. Temperature**



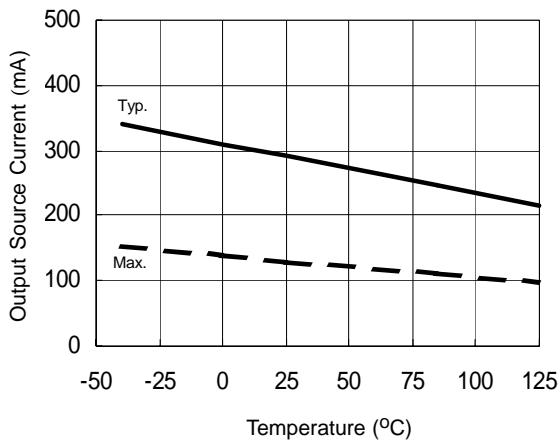
**Figure 19. V<sub>CC</sub> Undervoltage Threshold (-) vs. Temperature**



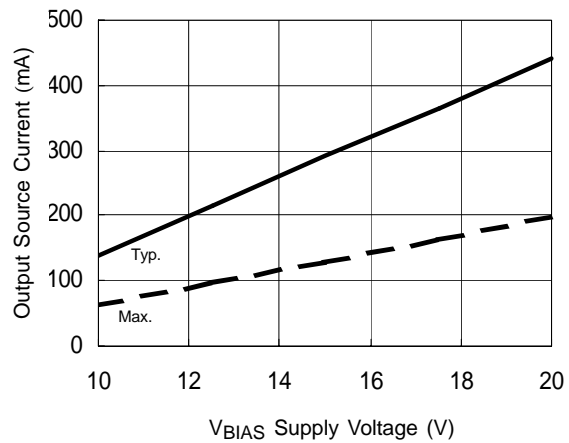
**Figure 20. V<sub>BS</sub> Undervoltage Threshold (+) vs. Temperature**



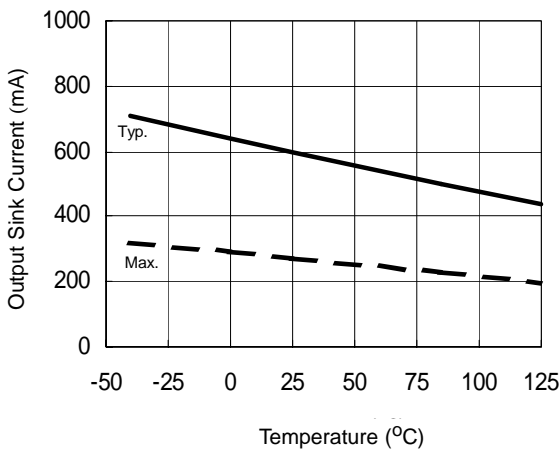
**Figure 21. V<sub>BS</sub> Undervoltage Threshold (-) vs. Temperature**



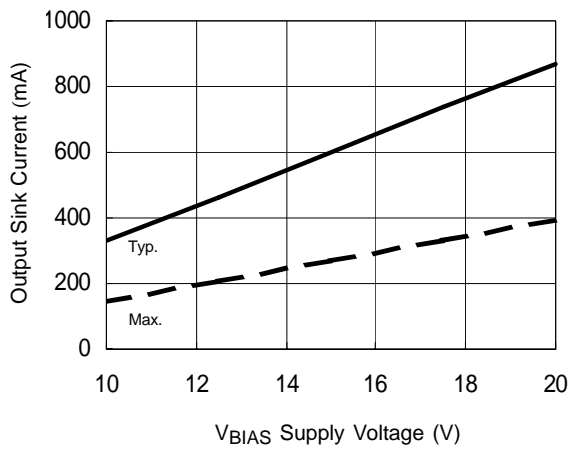
**Figure 22A. Output Source Current vs. Temperature**



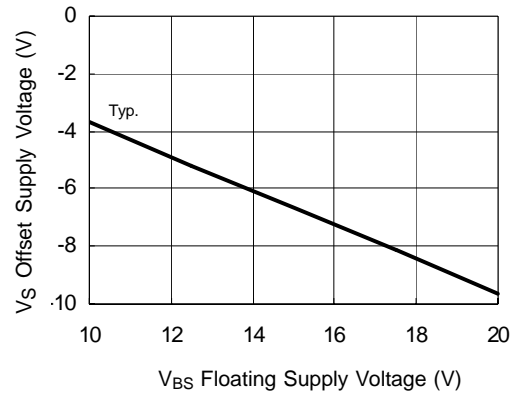
**Figure 22B. Output Source Current vs. Supply Voltage**



**Figure 23A. Output Sink Current vs. Temperature**

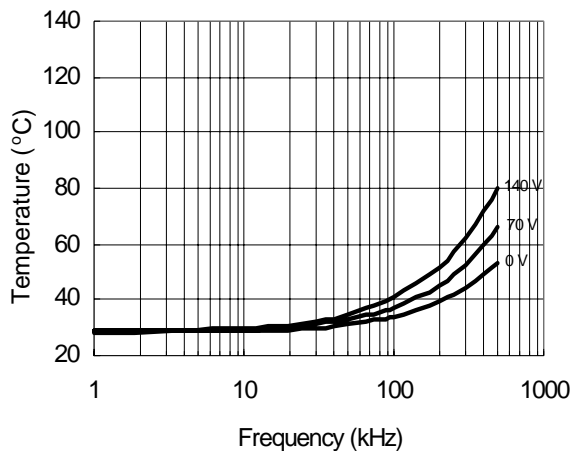


**Figure 23B. Output Sink Current vs. Supply Voltage**

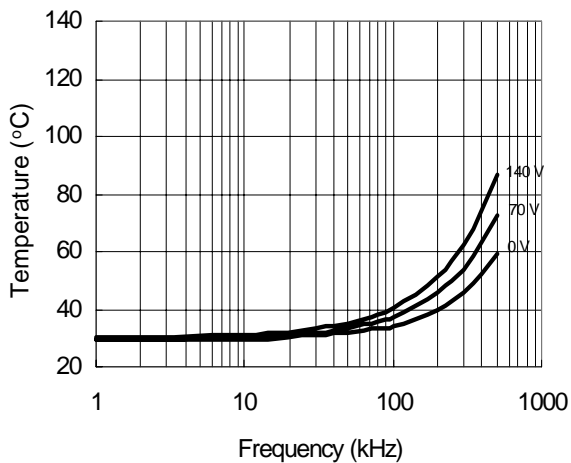


**Figure 24. Maximum V<sub>S</sub> Negative Offset vs. Supply Voltage**

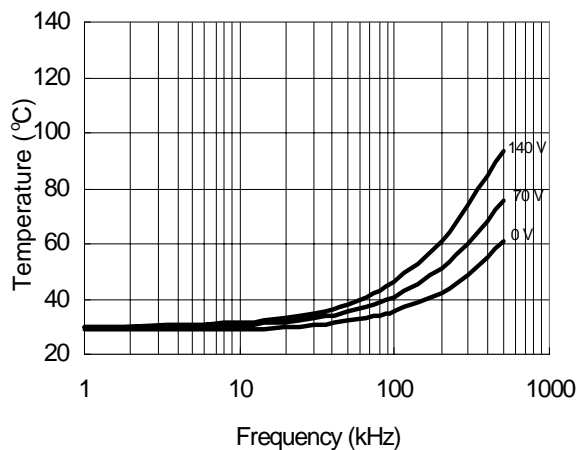




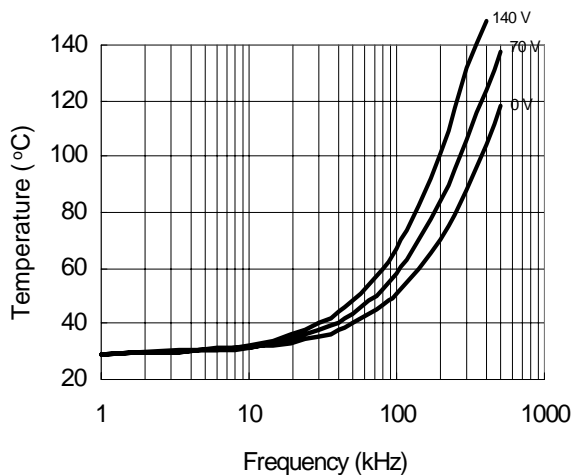
**Figure 25. IRS2308 vs. Frequency (IRFBC20),  
 $R_{gate}=33\Omega, V_{CC}=15\text{ V}$**



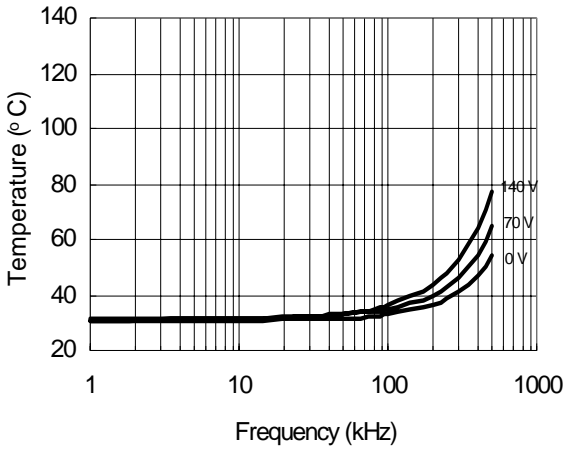
**Figure 26. IRS2308 vs. Frequency (IRFBC30),  
 $R_{gate}=22\Omega, V_{CC}=15\text{ V}$**



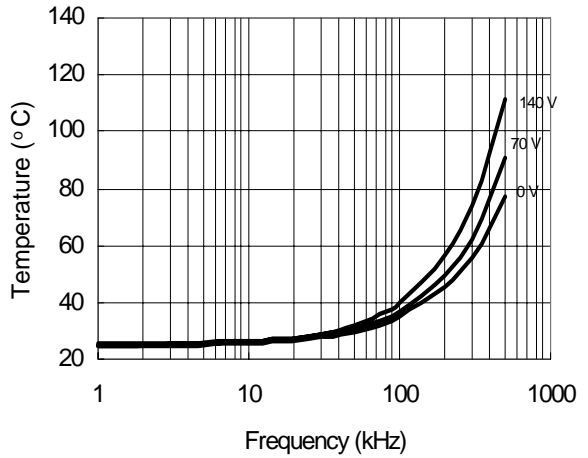
**Figure 27. IRS2308 vs. Frequency (IRFBC40),  
 $R_{gate}=15\Omega, V_{CC}=15\text{ V}$**



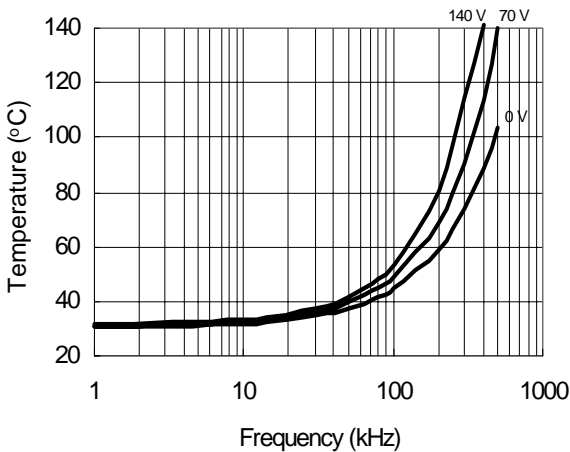
**Figure 28. IRS2308 vs. Frequency (IRFPE50),  
 $R_{gate}=10\Omega, V_{CC}=15\text{ V}$**



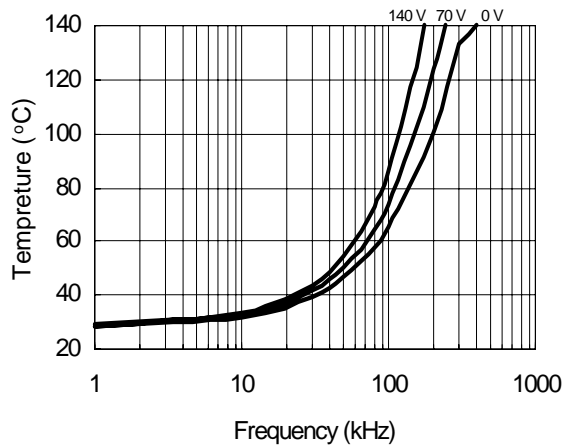
**Figure 29. IRS2308S vs. Frequency (IRFBC20),**  
 $R_{gate}=33\Omega, V_{CC}=15\text{ V}$



**Figure 30. IRS2308S vs. Frequency (IRFBC30),**  
 $R_{gate}=22\Omega, V_{CC}=15\text{ V}$

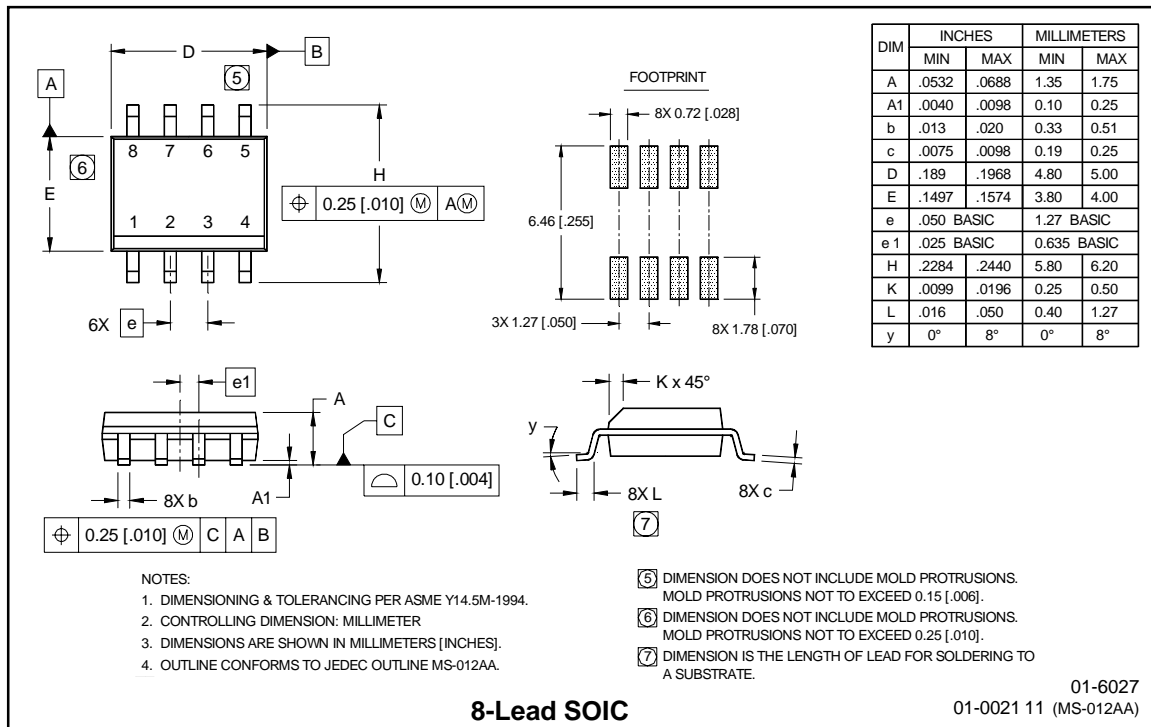
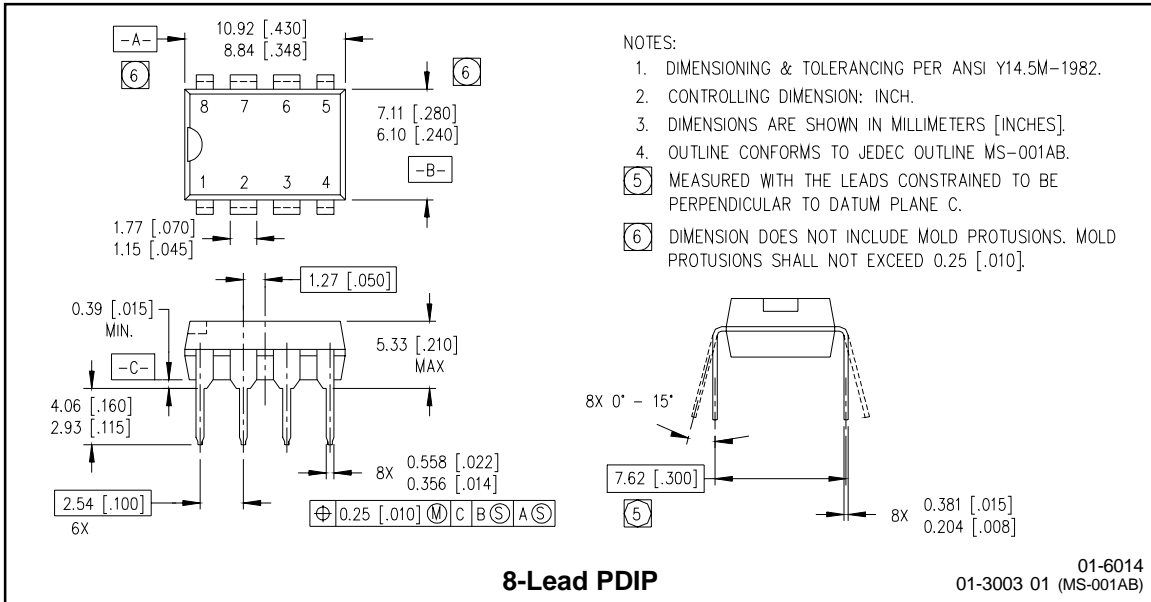


**Figure 31. IRS2308S vs. Frequency (IRFBC40),**  
 $R_{gate}=15\Omega, V_{CC}=15\text{ V}$

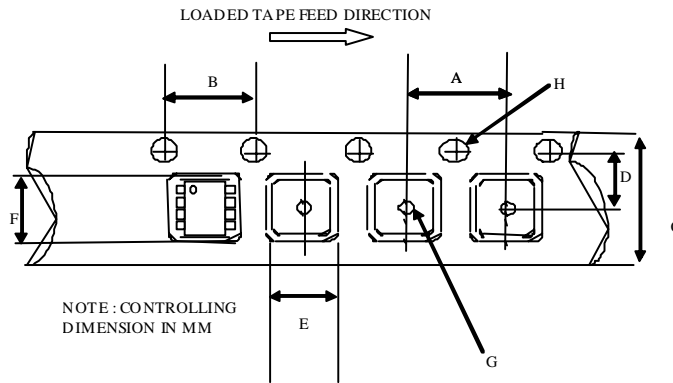


**Figure 32. IRS2308S vs. Frequency (IRFPE50),**  
 $R_{gate}=10\Omega, V_{CC}=15\text{ V}$

## Case outlines

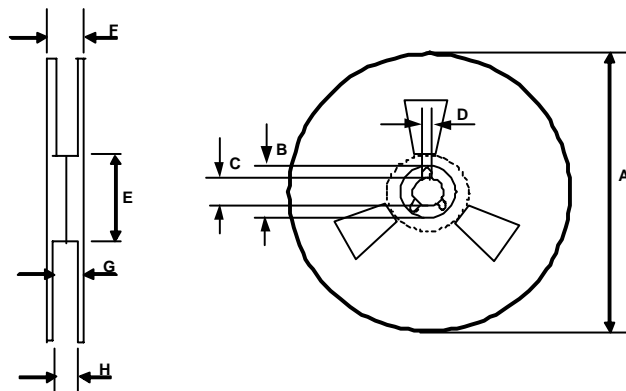


## Tape & Reel 8-Lead SOIC



CARRIER TAPE DIMENSION FOR 8SOICN

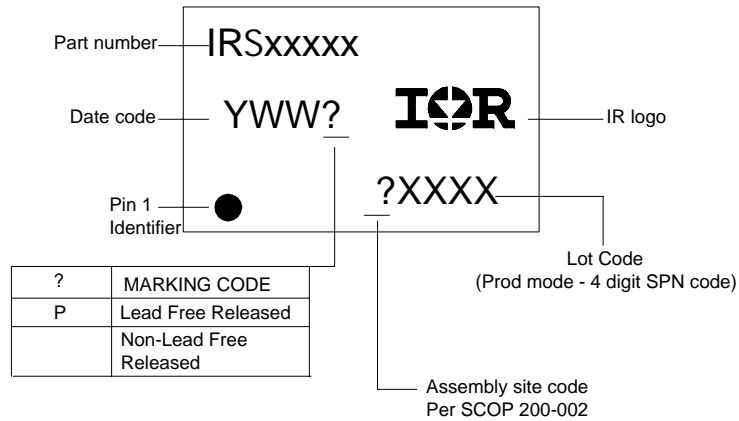
Code	Metric		Imperial	
	Min	Max	Min	Max
A	7.90	8.10	0.311	0.318
B	3.90	4.10	0.153	0.161
C	11.70	12.30	0.46	0.484
D	5.45	5.55	0.214	0.218
E	6.30	6.50	0.248	0.255
F	5.10	5.30	0.200	0.208
G	1.50	n/a	0.059	n/a
H	1.50	1.60	0.059	0.062



REEL DIMENSIONS FOR 8SOICN

Code	Metric		Imperial	
	Min	Max	Min	Max
A	329.60	330.25	12.976	13.001
B	20.95	21.45	0.824	0.844
C	12.80	13.20	0.503	0.519
D	1.95	2.45	0.767	0.096
E	98.00	102.00	3.858	4.015
F	n/a	18.40	n/a	0.724
G	14.50	17.10	0.570	0.673
H	12.40	14.40	0.488	0.566

## LEADFREE PART MARKING INFORMATION



## ORDER INFORMATION

8-Lead PDIP IRS2308PbF  
 8-Lead SOIC IRS2308SPbF  
 8-Lead SOIC Tape & Reel IRS2308STRPbF