International
IOR Rectifier

July 29, 2011

IRS4427PBF

DUAL LOW SIDE DRIVER

Features

- Gate drive supply range from 6 V to 20 V
- CMOS Schmitt-triggered inputs
- 3.3V and 5V logic compatible
- Two independent gate drivers
- Matched propagation delay for both channels
- Outputs in phase with inputs
- Leadfree, RoHS compliant

Typical Applications

- General Purpose Dual Low Side Driver
- DC-DC converters

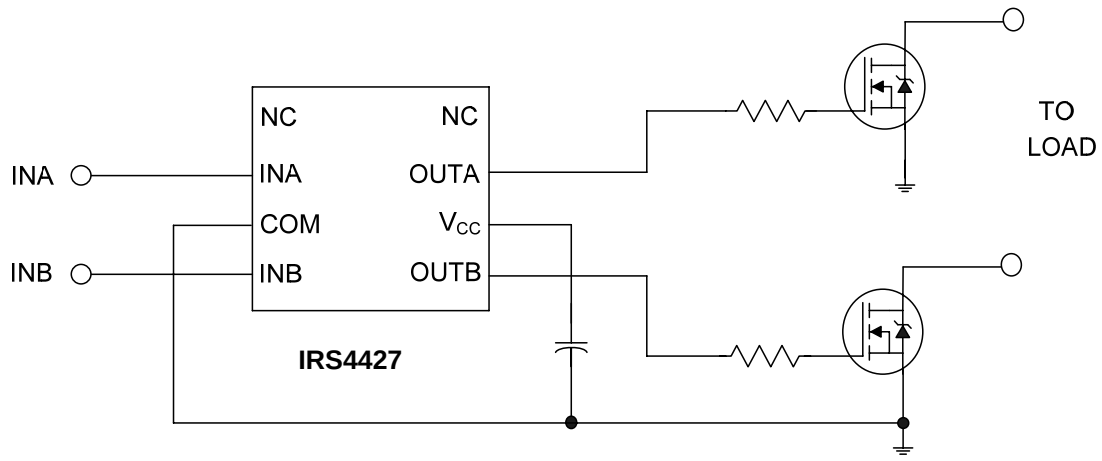
Product Summary

Topology	General Driver
V_{OUT}	6V - 20V
I_{o+} & I_{o-} (typical)	2.3A & 3.3A
t_{on} & t_{off} (typical)	50ns & 50ns

Package Type

PDIP 8

Typical Connection Diagram



(Refer to Lead Assignments for correct pin configuration). This/These diagram(s) show electrical connections only. Please refer to our Application Notes and Design Tips for proper circuit board layout.

Description

The IRS4427 is a low voltage, high speed power MOSFET and IGBT driver. Proprietary latch immune CMOS technologies enable ruggedized monolithic construction. The logic input is compatible with standard CMOS or LSTTL output. The output drivers feature a high pulse current buffer stage designed for minimum driver cross-conduction. Propagation delays between two channels are matched.

Qualification Information†

Qualification Level		Industrial††
		Comments: This family of ICs has passed JEDEC's Industrial qualification. IR's Consumer qualification level is granted by extension of the higher Industrial level.
Moisture Sensitivity Level		Not Applicable (non surface mount package style)
ESD	Machine Model	Class B (per JEDEC standard JESD22-A115)
	Human Body Model	Class 3A (per EIA/JEDEC standard EIA/JESD22-A114)
IC Latch-Up Test		Class I, Level A (per JESD78)
RoHS Compliant		Yes

† Qualification standards can be found at International Rectifier's web site http://www.irf.com/

†† Higher qualification ratings may be available should the user have such requirements. Please contact your International Rectifier sales representative for further information.

Absolute Maximum Ratings

Absolute Maximum Ratings indicate sustained limits beyond which damage to the device may occur. All voltage parameters are absolute voltages referenced to COM. The thermal resistance and power dissipation ratings are measured under board mounted and still air conditions.

Symbol	Definition	Min	Max	Units
V_{CC}	Fixed supply voltage	-0.3	25	V
V_O	Output voltage	-0.3	V_{CC} + 0.3	
V_{IN}	Logic input voltage	-0.3	V_{CC} + 0.3	
P_D	Package power dissipation @ TA ≤ 25°C	—	1	W
Rth_{JA}	Thermal resistance, junction to ambient	—	125	°C/W
T_J	Junction temperature	—	150	°C
T_S	Storage temperature	-55	150	
T_L	Lead temperature (soldering, 10 seconds)	—	300	

Recommended Operating Conditions

For proper operation, the device should be used within the recommended conditions. All voltage parameters are absolute voltages referenced to COM unless otherwise stated in the table. The offset rating is tested with supply of V_{CC} = 15V.

Symbol	Definition	Min	Max	Units
V_{CC}	Fixed supply voltage	6	20	V
V_O	Output voltage	0	V_{CC}	
V_{IN}	Logic input voltage	0	V_{CC}	
T_A	Ambient temperature	-40	125	°C

Static Electrical Characteristics

V_{CC} = 15V, T_A = 25°C unless otherwise specified. The $V_{IN,}$ and I_{IN} parameters are referenced to COM and are applicable to input leads: INA and INB. The V_O and I_O parameters are referenced to COM and are applicable to the output leads: OUTA and OUTB.

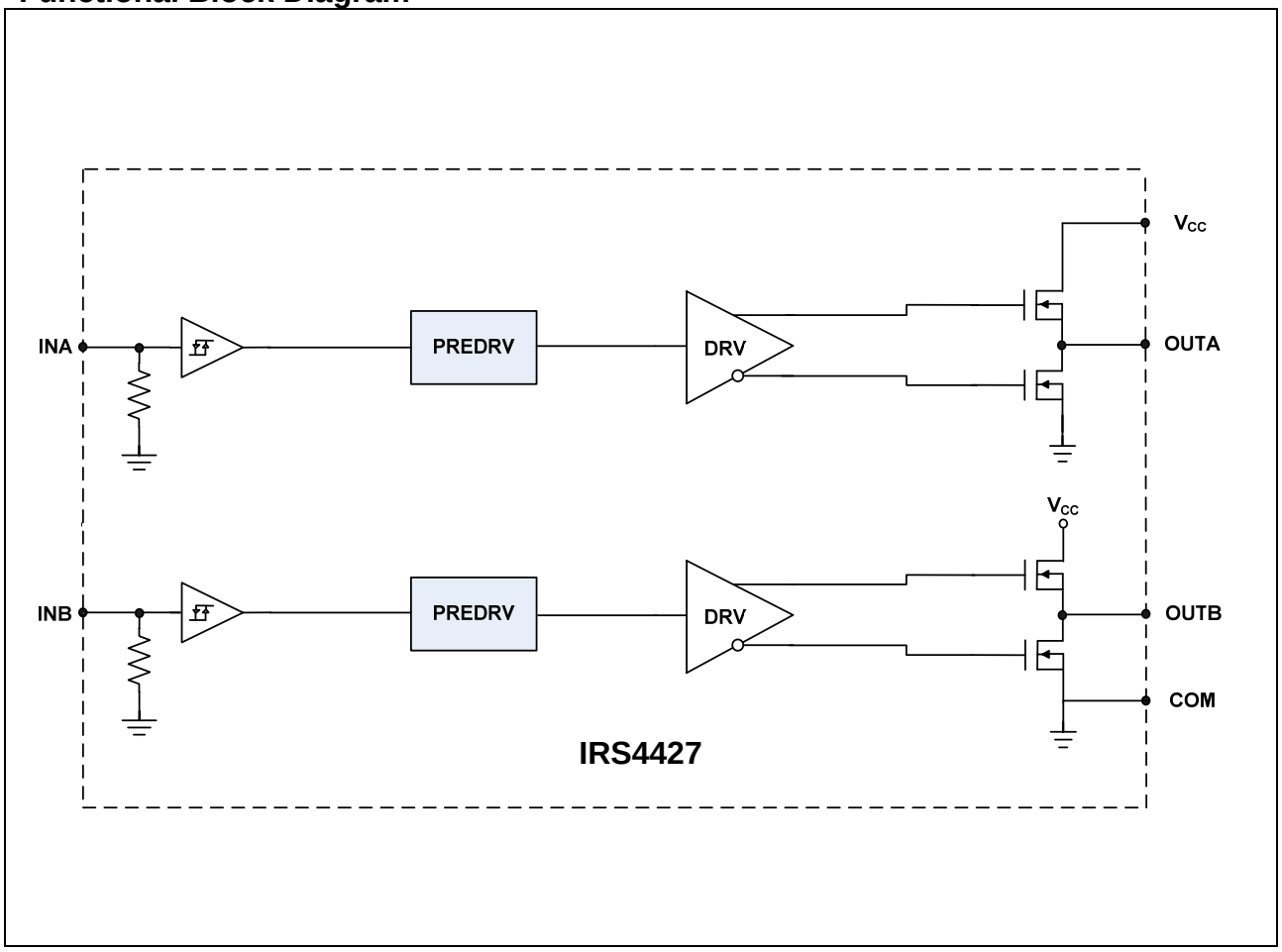
Symbol	Definition	Min	Typ	Max	Units	Test Conditions
V_{IH}	Logic "1" input voltage	2.5	—	—	V	
V_{IL}	Logic "0" input voltage	—	—	0.8	V	
V_{OH}	High level output voltage, V_{BIAS} -V_O	—	—	1.4		I_O = 0 mA
V_{OL}	Low level output voltage, V_O	—	—	0.15		I_O = 20 mA
I_{IN+}	Logic "1" input bias current	—	5	15	µA	V_{IN} = 5V
I_{IN-}	Logic "0" input bias current	-30	-10	—		V_{IN} = 0V
I_{QCC}	Quiescent V_{CC} supply current	—	100	200		V_{IN} = 0V or 5V
I_{O+}	Output high short circuit pulsed current	—	2.3	—	A	V_O = 0V, V_{IN} = 5V
I_{O-}	Output low short circuit pulsed current	—	3.3	—		V_O = 15V, V_{IN} = COM

Dynamic Electrical Characteristics

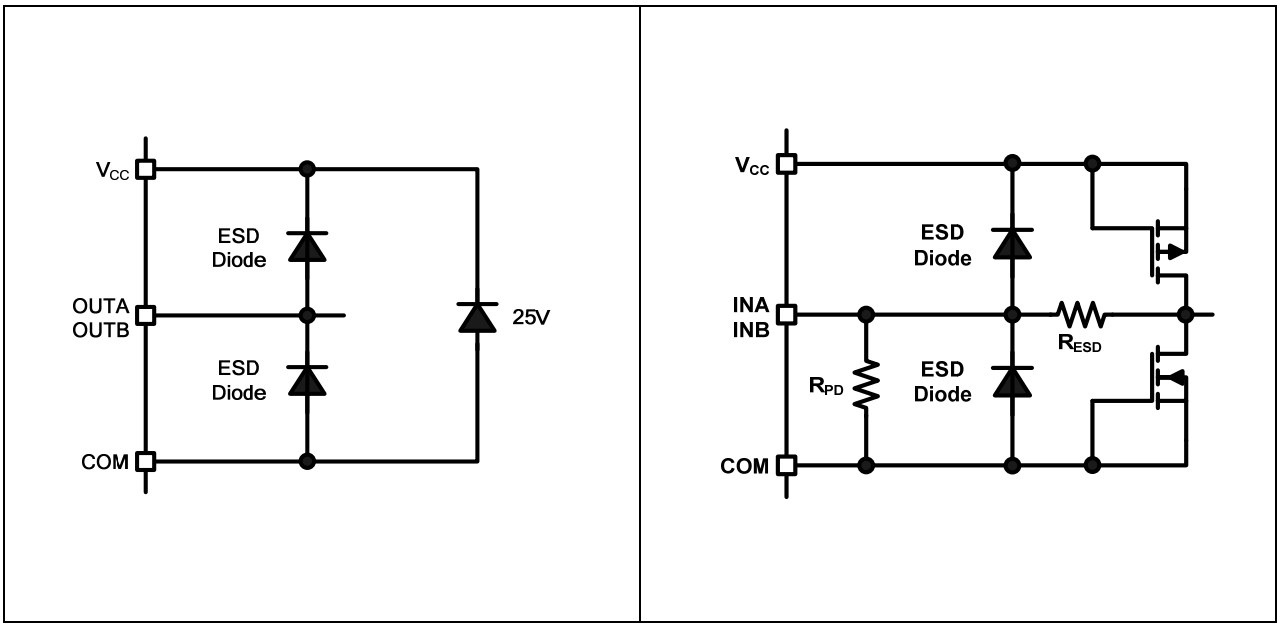
V_{CC} = 15V, T_A = 25°C, and C_L = 1000pF unless otherwise specified.

Symbol	Definition	Min	Typ	Max	Units	Test Conditions
t_{on}	Turn-on propagation delay	—	50	95	ns	Figure 2
t_{off}	Turn-off propagation delay	—	50	95		
t_r	Turn-on rise time	—	25	55		
t_f	Turn-off fall time	—	25	55		

Functional Block Diagram



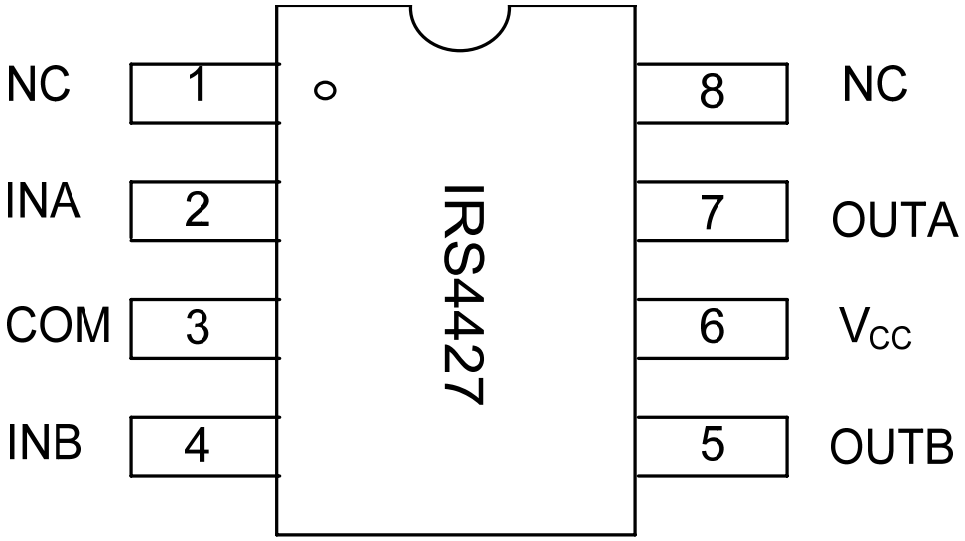
Input/Output Pin Equivalent Circuit Diagrams



Lead Definitions

PIN	Symbol	Description
1	NC	No connection
2	INA	Logic input for gate driver output (OUTA), in phase
3	COM	Ground
4	INB	Logic input for gate driver output (OUTB), in phase
5	OUTB	Gate drive output B
6	V_{CC}	Supply voltage
7	OUTA	Gate drive output A
8	NC	No connection

Lead Assignments



Application Information and Additional Details

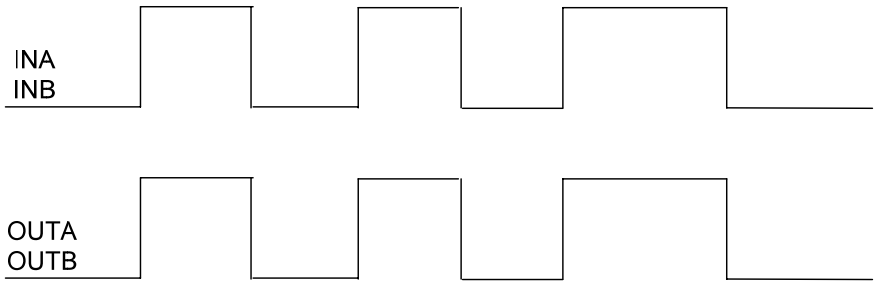


Figure 1: Input/output Timing Diagram

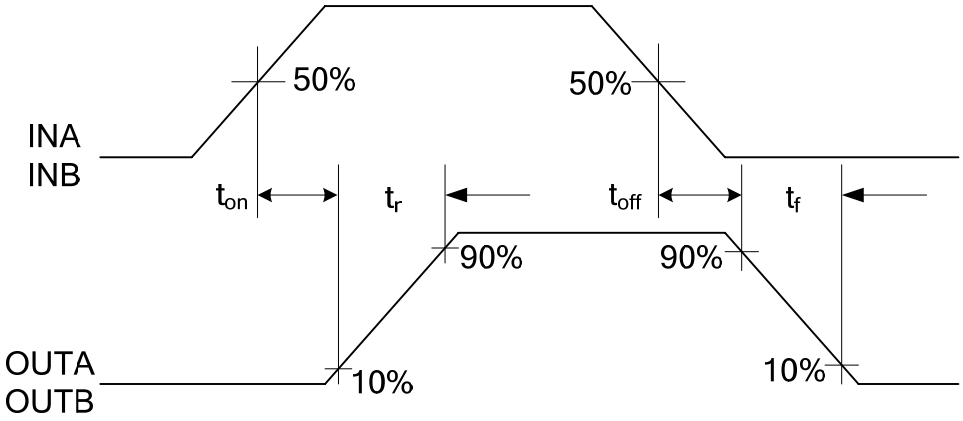


Figure 2: Switching Time Waveform Definitions

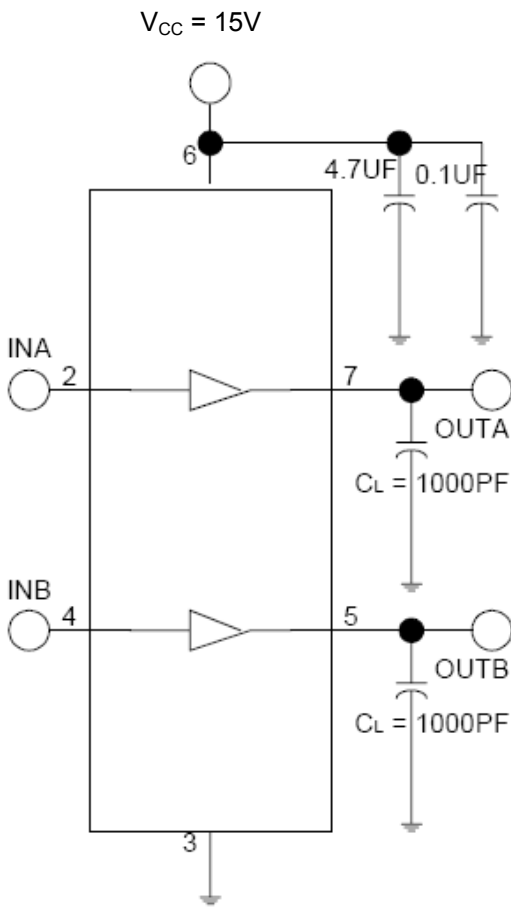
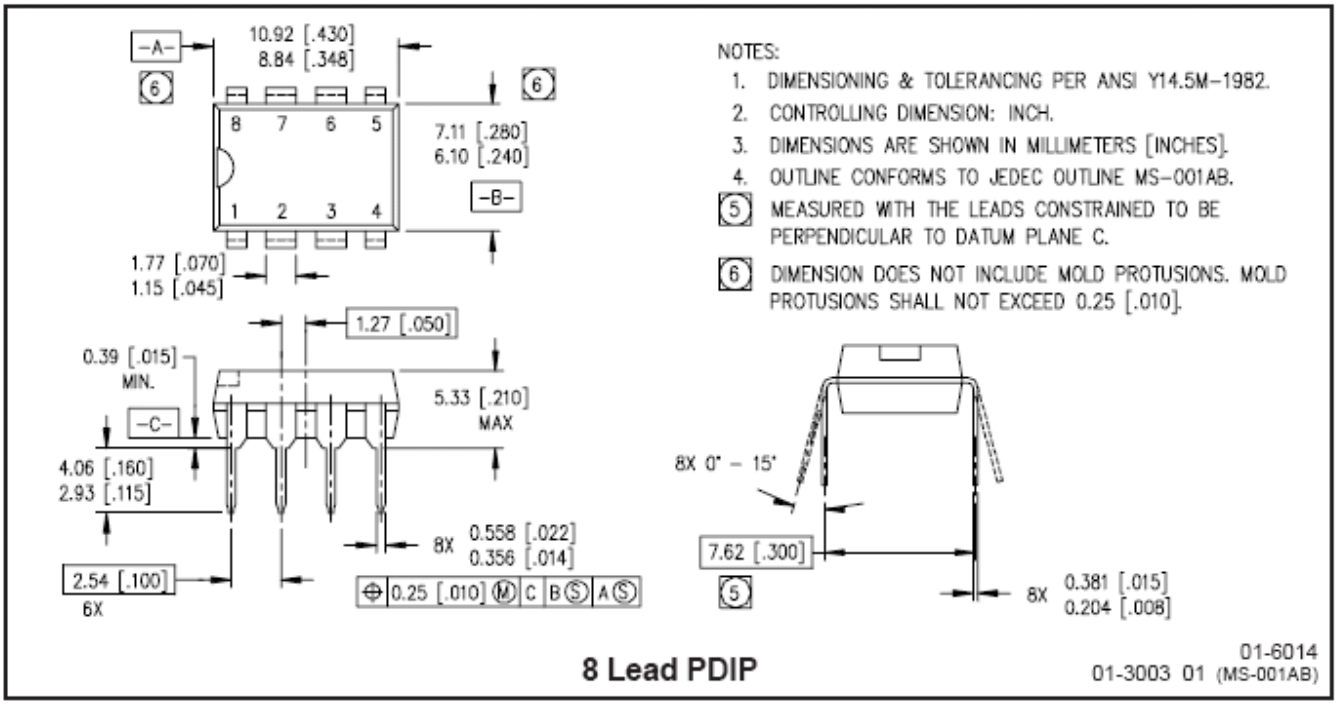
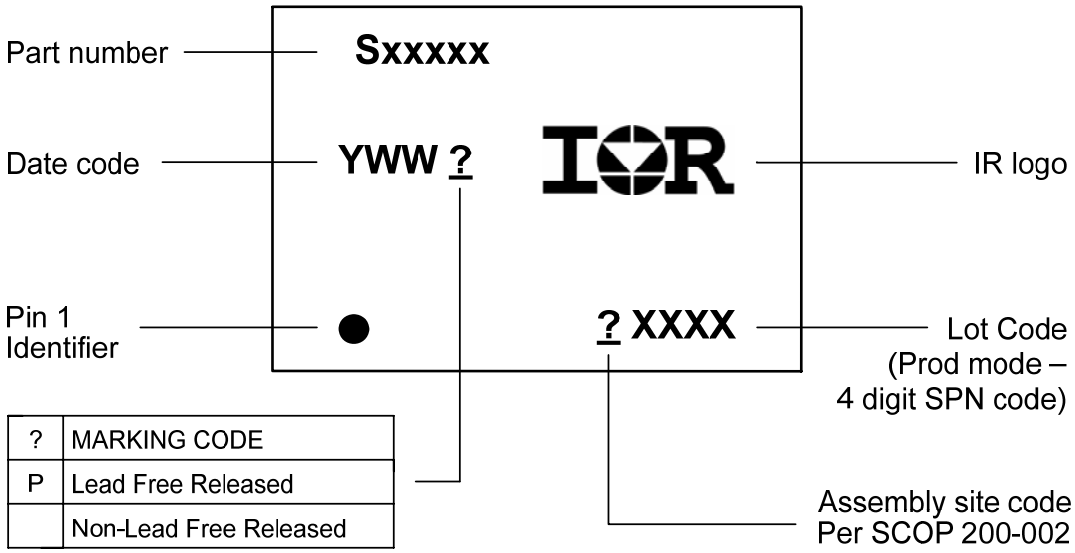


Figure 3: Switching Time Test Circuit

Package Details, PDIP8



Part Marking Information



?	MARKING CODE
P	Lead Free Released
	Non-Lead Free Released

Ordering Information

Base Part Number	Package Type	Standard Pack		Complete Part Number
		Form	Quantity	
IRS4427	PDIP 8	Tube/Bulk	50	IRS4427PBF

For technical support, please contact IR's Technical Assistance Center
http://www.irf.com/technical-info/

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