PCIe® 2.0 Clock Generator with 4 HCSL Outputs for Automotive Applications

Product Features

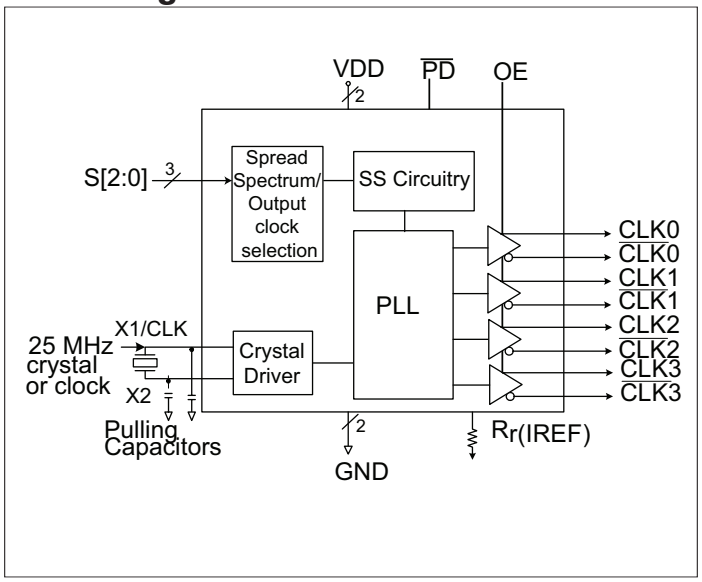
- PCIe® 2.0 complaint
  →Phase jitter - 2.1ps RMS (typ)
- LVDS compatible outputs
- Supply voltage of 3.3V ±5%
- 25MHz crystal or clock input frequency
- HCSL outputs, 0.7V Current mode differential pair
- Jitter 40ps cycle-to-cycle (typ)
- Spread of -0.5%, -1.0%, -1.5%, and no spread
- AEC-Q100 qualified
- Spread Bypass option available
- Spread and frequency selection via external pins
- Packaging: (Pb-free and Green)
  →20-pin, 173-mil wide TSSOP

Description

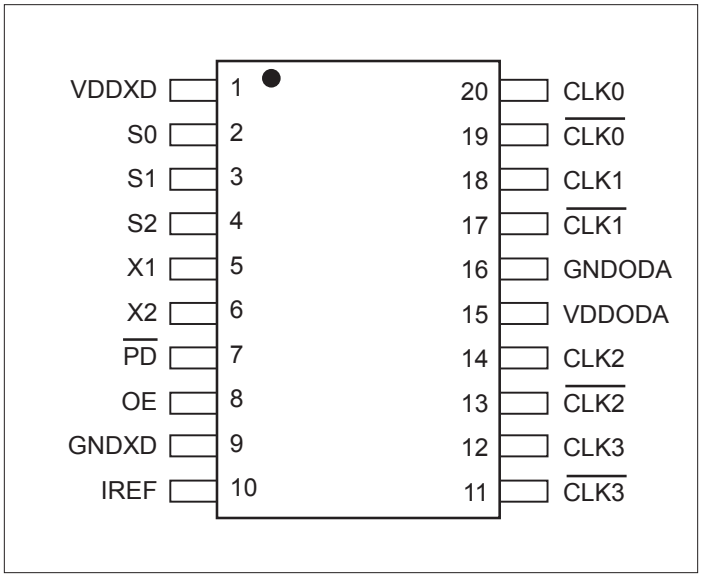
The PI6C557-05Q is a spread spectrum clock generator compliant to PCI Express® 2.0 and Ethernet requirements. The device is used for PC or embedded systems to substantially reduce Electromagnetic Interference (EMI).

The PI6C557-05Q provides four differential (HCSL) or LVDS spread spectrum outputs. The PI6C557-05Q is configured to select spread and clock selection. Using Pericom's patented Phase-Locked Loop (PLL) techniques, the device takes a 25MHz crystal input and produces four pairs of differential outputs (HCSL) at 100MHz and 200MHz clock frequencies. It also provides spread selection of -0.5%, -1.0%, -1.5%, and no spread.

Block Diagram



Pin Configuration



Pin Description

Pin #	Pin Name	I/O Type	Description
1	VDDXD	Power	Connect to a +3.3V source.
2	S0	Input	Spread Spectrum Select pin #0. See Spread Spectrum Selection table. Internal pull-up resistor.
3	S1	Input	Spread Spectrum Select pin #1. See Spread Spectrum Selection table. Internal pull-up resistor.
4	S2	Input	Spread Spectrum Select pin #2. See Spread Spectrum Selection table. Internal pull-up resistor.
5	X1	Input	Crystal connection.
6	X2	Output	Crystal connection.
7	$\overline{PD}$	Input	Power down. Internal pull-up resistor.
8	OE	Input	Output enable. Tri-states output (High=enable outputs); Low=disable outputs). Internal pull-up resistor.
9	GND	Power	Connect to digital circuit ground.
10	IREF	Output	Precision resistor attached to this pin is connected to the internal current reference.
11	$\overline{CLK3}$	Output	Selectable 100/200 MHz Spread Spectrum differential compliment output clock 3.
12	CLK3	Output	Selectable 100/200 MHz Spread Spectrum differential true output clock 3.
13	$\overline{CLK2}$	Output	Selectable 100/200 MHz Spread Spectrum differential compliment output clock 2.
14	CLK2	Output	Selectable 100/200 MHz Spread Spectrum differential true output clock 2.
15	VDDODA	Power	Connect to a +3.3V analog source.
16	GND	Power	Output and Analog circuit ground
17	$\overline{CLK1}$	Output	Selectable 100/200 MHz Spread Spectrum differential compliment output clock 1.
18	CLK1	Output	Selectable 100/200 MHz Spread Spectrum differential true output clock 1.
19	$\overline{CLK0}$	Output	Selectable 100/200 MHz Spread Spectrum differential compliment output clock 0.
20	CLK0	Output	Selectable 100/200 MHz Spread Spectrum differential true output clock 0.

Table 2: Spread Selection Table

S2	S1	S0	Spread %	Spread Type	Output Frequency
0	0	0	-0.5	Down	100
0	0	1	-1.0	Down	100
0	1	0	-1.5	Down	100
0	1	1	No Spread	Not Applicable	100
1	0	0	-0.5	Down	200
1	0	1	-1.0	Down	200
1	1	0	-1.5	Down	200
1	1	1	No Spread	Not Applicable	200

Application Information

Decoupling Capacitors

Decoupling capacitors of 0.01µF or 0.1µF must be connected between each VDD pin and the PCB ground plane and placed as close to the VDD pin as possible.

PI6C557-05Q must be isolated from system power supply noise to perform optimally.

Crystal

Use a 25MHz fundamental mode parallel resonant crystal with less than 30PPM of error across temperature.

Current Source (Iref) Reference Resistor - R_R

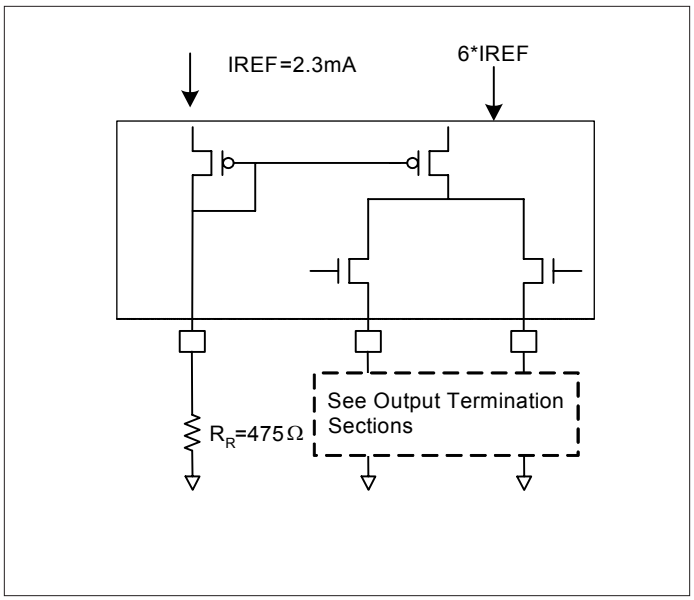
If board target trace impedance is 50-Ohm,
then RR = 475-Ohm providing an IREF of 2.32 mA. The output current (IOH) is 6*IREF.

Output Termination

The PCI-Express differential clock outputs of the PI6C557-05Q are open source drivers and require an external series resistor and a resistor to ground. These resistor values and their allowable locations are shown in detail in the PCI-Express Layout Guidelines section.

The PI6C557-05Q can be configured for LVDS compatible voltage levels. See the LVDS Compatible Layout Guidelines section.

Output Structures



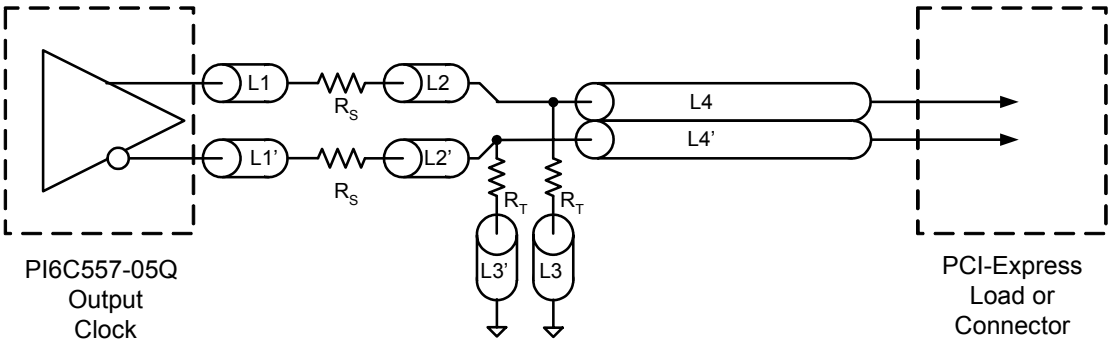
PCI-Express Layout Guidelines

Common Recommendations for Differential Routing	Dimension or Value	Unit
L1 length, route as non-coupled 50-Ohm trace.	0.5 max	inch
L2 length, route as non-coupled 50-Ohm trace.	0.2 max	inch
L3 length, route as non-coupled 50-Ohm trace.	0.2 max	inch
R_S	33	Ohm
R_T	49.9	Ohm

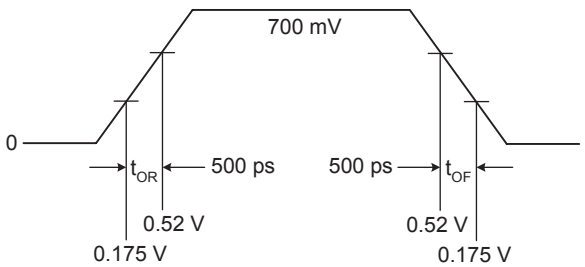
Differential Routing on a Single PCB	Dimension or Value	Unit
L4 length, route as coupled microstrip 100-Ohm differential trace.	2 min to 16 max	inch
L4 length, route as coupled stripline 100-Ohm differential trace.	1.8 min to 14.4 max	inch

Differential Routing to a PCI Express connector	Dimension or Value	Unit
L4 length, route as coupled microstrip 100-Ohm differential trace.	0.25 min to 14 max	inch
L4 length, route as coupled stripline 100-Ohm differential trace.	0.225 min to 12.6 max	inch

PCI-Express Device Routing



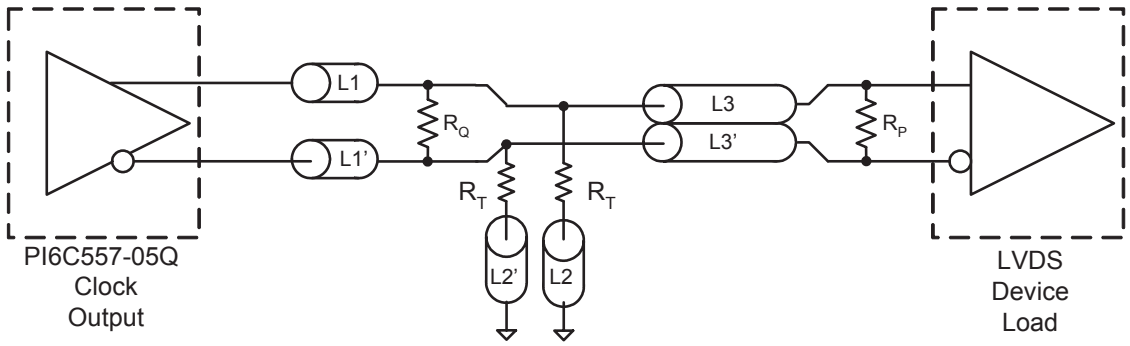
Typical PCI-Express (HCSL) Waveform



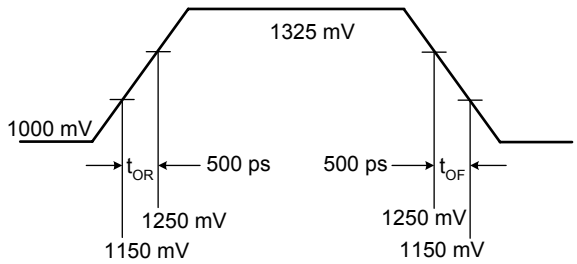
Application Information

LVDS Recommendations for Differential Routing	Dimension or Value	Unit
L1 length, route as non-coupled 50-Ohm trace.	0.5 max	inch
L2 length, route as non-coupled 50-Ohm trace.	0.2 max	inch
R_P	100	Ohm
R_Q	100	Ohm
R_T	150	Ohm
L3 length, route as 100Ω differential trace.		
L3 length, route as 100Ω differential trace.		

LVDS Device Routing



Typical LVDS Waveform



Electrical Specifications

Maximum Ratings

Supply Voltage to Ground Potential	5.5V
All Inputs and Outputs	-0.5V to V_{DD}+0.5V
Ambient Operating Temperature	-40 to +85°C
Storage Temperature	-65 to +150°C
Junction Temperature	150°C
Soldering Temperature	260°C
ESD Protection (Input)	2000 V min (HBM)

Note:
Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Recommended Operation Conditions

Parameter	Min.	Typ.	Max.	Unit
Ambient Operating Temperature	-40		+85	°C
Power Supply Voltage (measured in respect to GND)	3.135		3.465	V

DC Characteristics (V_{DD} = 3.3V ±5%, T_A = -40°C to +85°C)

Symbol	Parameter	Conditions		Min.	Typ.	Max.	Unit
V_{DD}	Supply Voltage			3.135	3.3	3.465	V
V_{IH}	Input High Voltage(1)			2.0		VDD +0.3	V
V_{IL}	Input Low Voltage(1)			GND -0.3		0.8	V
I_{IL}	Input Leakage Current	0 < Vin < VDD	Without input pull-up and pull-downs	-5		5	µA
I_{DD}	Operating Supply Current	R_L = 50Ω, C_L = 2pF @100MHz			105	120	mA
I_{DDOE}		OE = LOW			40	50	mA
I_{DDPD}		No load $\overline{PD}$ = LOW			60	100	µA
C_{IN}	Input Capacitance	Input pin capacitance				7	pF
C_{OUT}	Output Capacitance	Output pin capacitance				6	pF
L_{PIN}	Pin Inductance					5	nH
R_{OUT}	Output Resistance	CLK Outputs		3.0			kΩ

Note:
1. Single edge is monotonic when transitioning through region.

AC Characteristics (V_{DD} = 3.3V ±5%, TA = -40°C to +85°C)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
F_{IN}	Input Frequency			25		MHz
V_{OUT}	Output Frequency	HCSL terminal			200	MHz
		LVDS terminal			100	
V_{OH}	Output High Voltage (1,2)	@VDD = 3.3V	660	700	850	mV
V_{OL}	Output Low Voltage(1,2)		-150	0	27	mV
V_{CPA}	Crossing Point Voltage(1,2)	Absolute	250	350	550	mV
V_{CN}	Crossing Point Voltage(1,2,4)	Variation over all edges			140	mV
J_{CC}	Jitter, Cycle-to-Cycle(1,3)			40	60	ps
J_{RMS}	RMS Jitter	PCIe Gen 2 High Band		2.1	3.1	ps
		PCIe Gen 2 Low Band		0.6	3.0	
MF	Modulation Frequency	Spread Spectrum	30	31.5	33	kHz
t_{OR}	Rise Time(1,2)	From 0.175V to 0.525V	175	332	700	ps
t_{OF}	Fall Time(1,2)	From 0.525V to 0.175V	175	344	700	ps
T_{SKEW}	Skew between outputs	At Crossing Point Voltage			50	ps
$T_{DUTY-CYCLE}$	Duty Cycle(1,3)		45		55	%
T_{OE}	Output Enable Time(5)	All outputs			10	µs
T_{OT}	Output Disable Time(5)	All outputs			10	µs
t_{STABLE}	From power-up to VDD=3.3V	From Power-up VDD=3.3V		3.0		ms

Notes:
1. R_L = 50-Ohm with C_L = 2 pF and R_R
2. Single-ended waveform
3. Differential waveform
4. Measured at the crossing point
5. CLK pins are tri-stated when OE is LOW

Thermal Characteristics

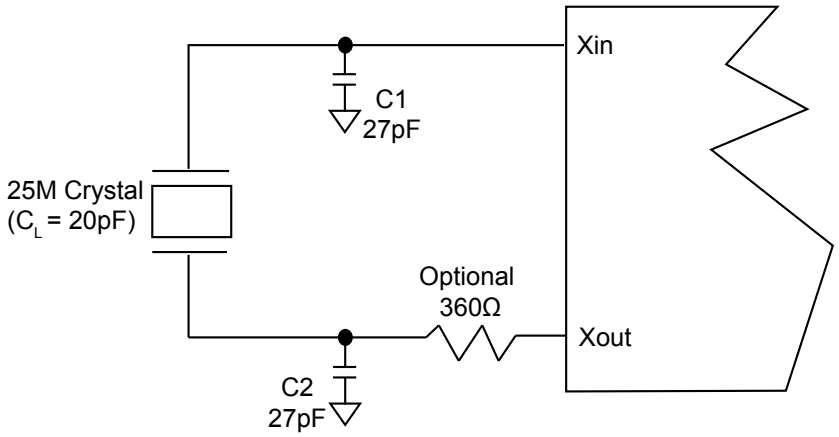
Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
θ_{JA}	Thermal Resistance Junction to Ambient	Still air			93	°C/W
θ_{JC}	Thermal Resistance Junction to Case				20	°C/W

Recomended Crystal Specification

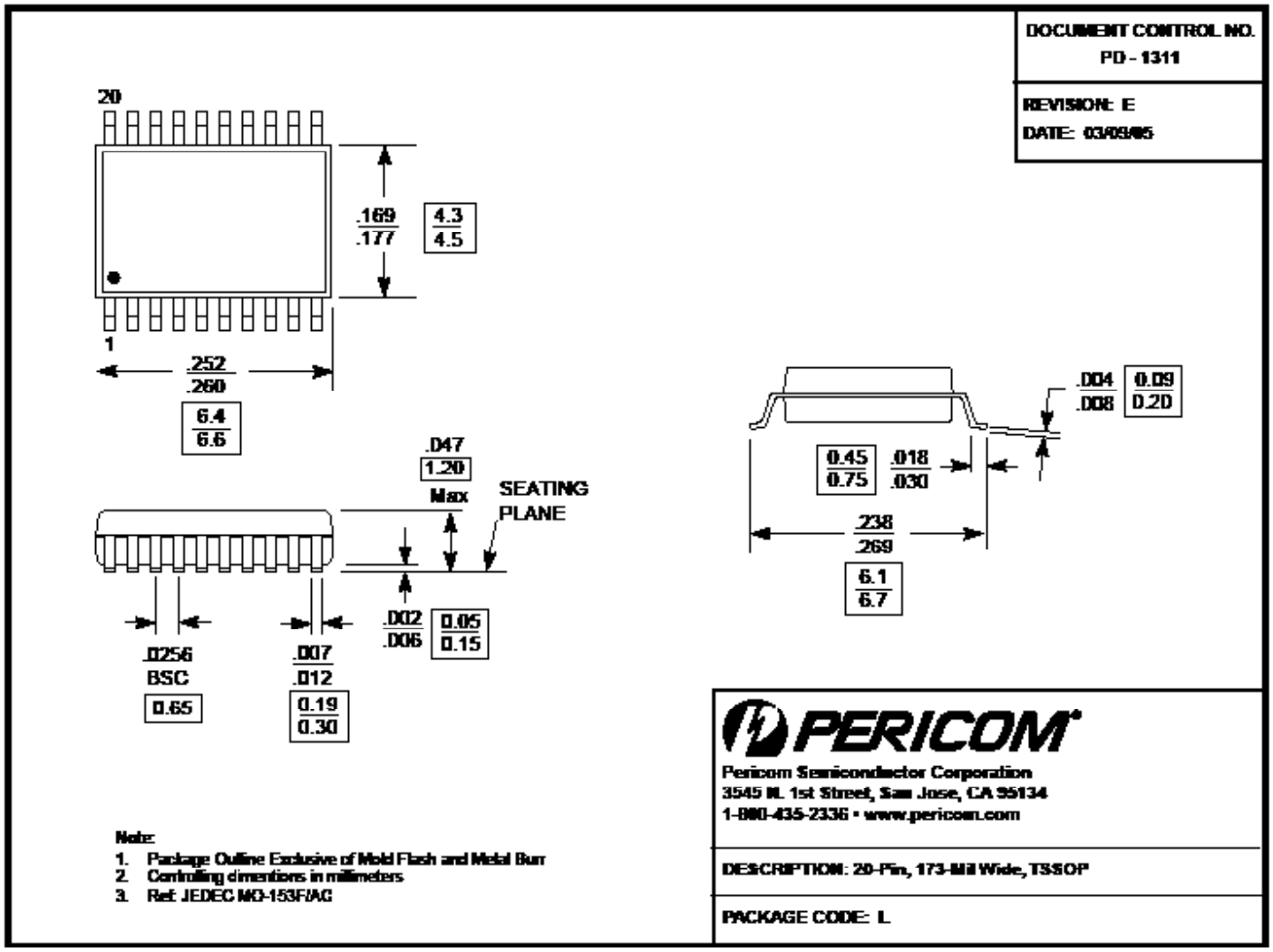
Pericom recommends:
a) FL2500184Q, SMD 3.2x2.5(4P), 25M, CL=20pF, Frequency Tolerance ±15ppm, Stability ±20ppm
(http://www.pericom.com/pdf/datasheets/se/FL.pdfb)

Recommended Crystal Circuit

The following diagram shows PI6C557-05Q crystal circuit connection with a parallel crystal. For the C L=20pF parallel crystal, it is suggested to use C1=27 pF, C2=27 pF in general. C1 and C2 can be adjusted to fine tune to the target ppm of crystal oscillation according to different board layouts. R1=360 ohm is recommended in layout for smaller size crystal drive level adjustment.



Packaging Mechanical: 20-pin TSSOP (L)



Ordering Information[1-3]

Ordering Code	Package Code	PackageType
PI6C557-05QLE	L	Pb-free & Green, 20-Pin TSSOP

Note:

1. Thermal characteristics and package top marking information can be found at http://www.pericom.com/packaging/
2. E = lead-free and green packaging
3. Adding an X suffix = tape/reel