

PCIe® 3.0 Clock Generator with 2 HCSL Outputs

Features

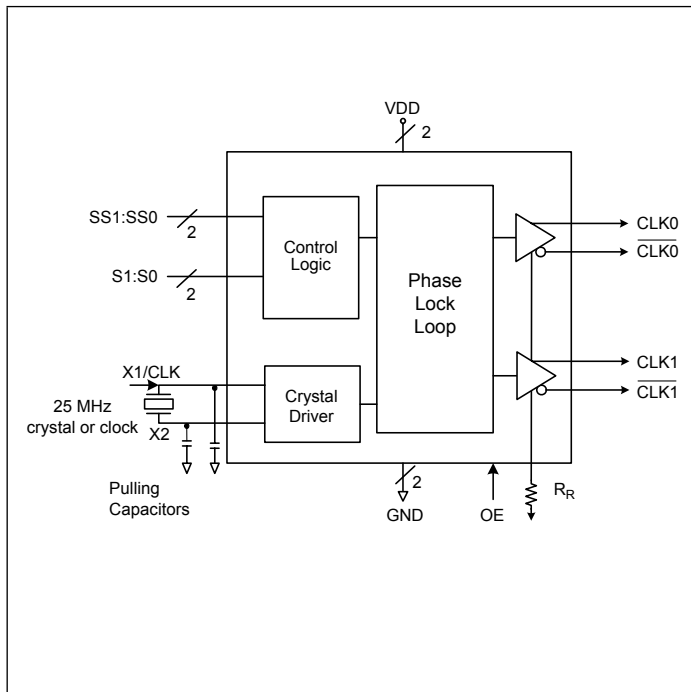
- PCIe® 3.0 compliant
 - PCIe 3.0 Phase jitter - 0.45ps RMS (High Freq. Typ.)
- LVDS compatible outputs
- Supply voltage of 3.3V ±10%
- 25MHz crystal or clock input frequency
- HCSL outputs, 0.8V Current mode differential pair
- Jitter 35ps cycle-to-cycle (typ)
- Spread of -0.5%, -0.75%, and no spread
- Industrial temperature range
- Spread Bypass option available
- Spread and frequency selection via external pins
- Packaging: (Pb-free and Green)
 - 16-pin TSSOP (L16)
 - 16-pin QSOP (Q16)

Description

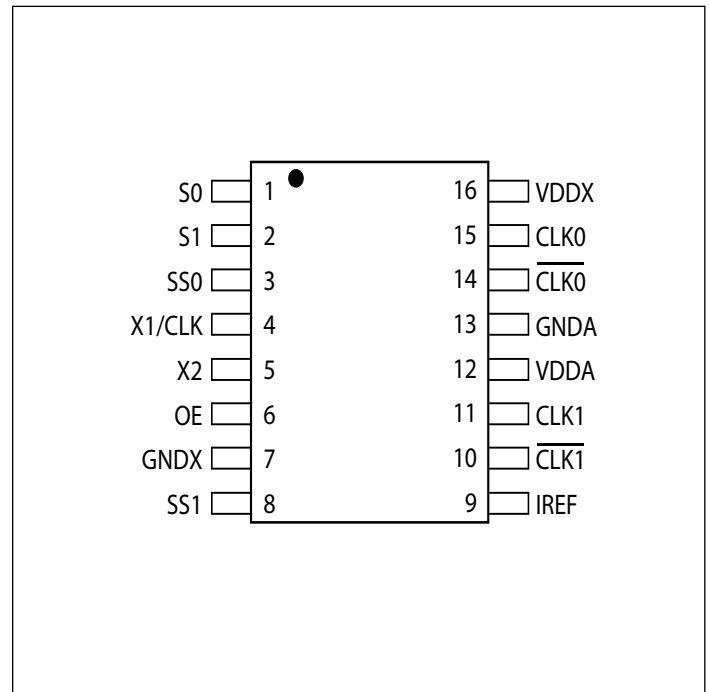
The PI6C557-03B is a spread spectrum clock generator compliant to PCI Express® 3.0 and Ethernet requirements. The device is used for PC or embedded systems to substantially reduce Electro-magnetic Interference (EMI).

The PI6C557-03B provides two differential (HCSL) or LVDS spread spectrum outputs. The PI6C557-03B is configured to select spread and clock selection. Using Pericom's patented Phase-Locked Loop (PLL) techniques, the device takes a 25MHz crystal input and produces two pairs of differential outputs (HCSL) at 25MHz, 100MHz, 125MHz and 200MHz clock frequencies. It also provides spread selection of -0.5%, -0.75%, and no spread.

Block Diagram



Pin Configuration (16-Pin TSSOP)



Pin Description

| Pin # | Pin Name | I/O Type | Description |
|-------|--------------------------|----------|---|
| 1 | S0 | Input | Select pin 0 (Internal pull-up resistor). See Table 1. |
| 2 | S1 | Input | Select pin 1 (Internal pull-up resistor). See Table 1. |
| 3 | SS0 | Input | Spread Select pin 0 (Internal pull-up resistor). See Table 2. |
| 4 | X1/CLK | Input | Crystal or clock input. Connect to a 25MHz crystal or single ended clock. |
| 5 | X2 | Output | Crystal connection. Leave unconnected for clock input. |
| 6 | OE | Input | Output enable. Internal pull-up resistor. |
| 7 | GNDX | Power | Crystal ground pin. |
| 8 | SS1 | Input | Spread Select pin 1 (Internal pull-up resistor). See Table 2. |
| 9 | IREF | Output | Precision resistor attached to this pin is connected to the internal current reference. |
| 10 | $\overline{\text{CLK1}}$ | Output | HCSL compliment clock output |
| 11 | CLK1 | Output | HCSL clock output |
| 12 | VDDA | Power | Connect to a +3.3V source. |
| 13 | GND A | Power | Output and analog circuit ground. |
| 14 | $\overline{\text{CLK0}}$ | Output | HCSL compliment clock output |
| 15 | CLK0 | Output | HCSL clock output |
| 16 | VDDX | Power | Connect to a +3.3V source. |

Table 1: Output Select Table

| S1 | S0 | CLK(MHz) |
|----|----|----------|
| 0 | 0 | 25 |
| 0 | 1 | 100 |
| 1 | 0 | 125 |
| 1 | 1 | 200 |

Table 2: Spread Selection Table

| SS1 | SS0 | Spread |
|-----|-----|------------|
| 0 | 0 | No Spread |
| 0 | 1 | Down -0.5 |
| 1 | 0 | Down -0.75 |
| 1 | 1 | No Spread |

Application Information

Decoupling Capacitors

Decoupling capacitors of $0.01\mu\text{F}$ should be connected between each V_{DD} pin and the ground plane and placed as close to the V_{DD} pin as possible.

Crystal

Use a 25MHz fundamental mode parallel resonant crystal with less than 300PPM of error across temperature.

Crystal Capacitors

C_L = Crystals's load capacitance in pF

Crystal Capacitors (pF) = $(C_L - 8) * 2$

For example, for a crystal with 16pF load caps, the external effective crystal cap would be 16 pF. $(16-8)*2=16$.

Current Source (IREF) Reference Resistor - R_R

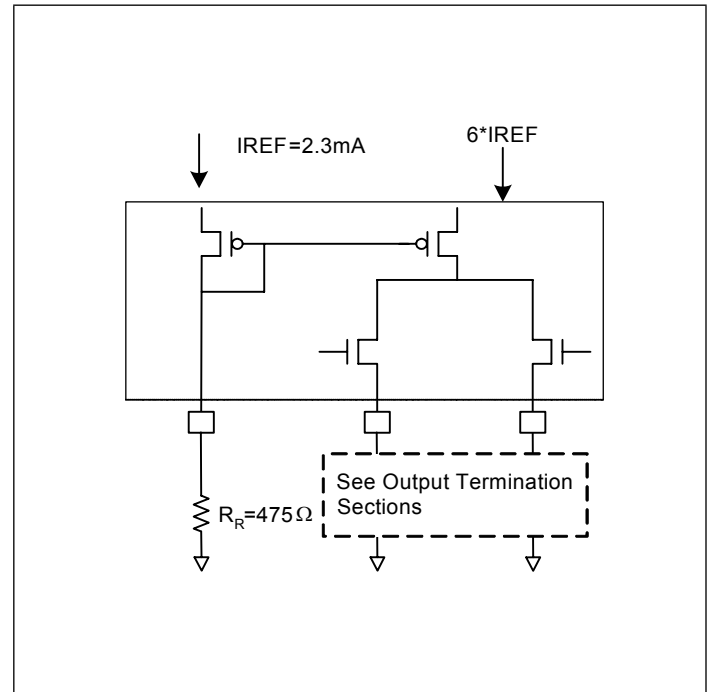
If board target trace impedance is 50Ω , then $R_R = 475\Omega$ providing an IREF of 2.32 mA. The output current (I_{OH}) is $6*IREF$.

Output Termination

The PCI Express differential clock outputs of the PI6C557-03B are open source drivers and require an external series resistor and a resistor to ground. These resistor values and their allowable locations are shown in detail in the PCI Express Layout Guidelines section.

The PI6C557-03B can be configured for LVDS compatible voltage levels. See the LVDS Compatible Layout Guidelines section.

Output Structures



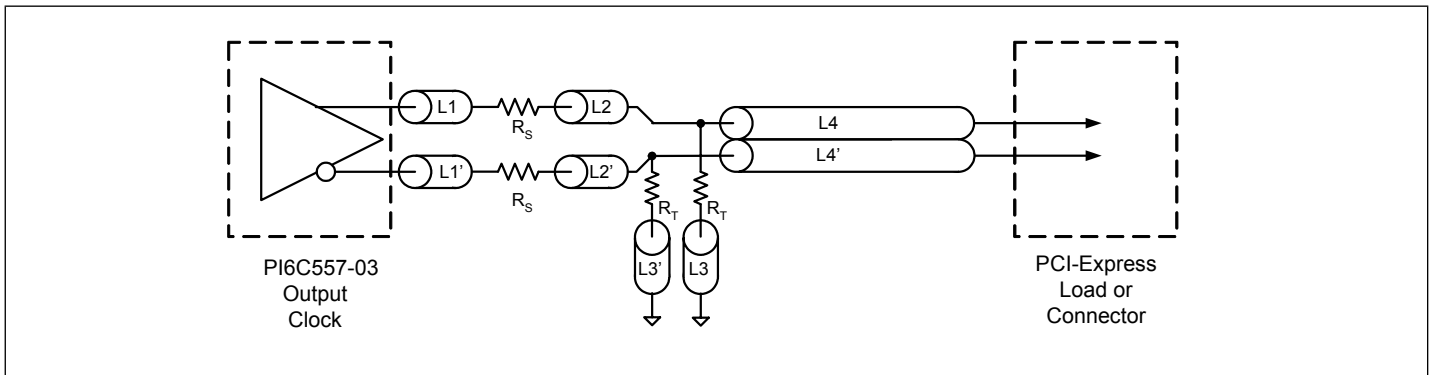
PCI Express Layout Guidelines

| Common Recommendations for Differential Routing | Dimension or Value | Unit |
|---|--------------------|------|
| L1 length, route as non-coupled 50Ω trace. | 0.5 max | inch |
| L2 length, route as non-coupled 50Ω trace. | 0.2 max | inch |
| L3 length, route as non-coupled 50Ω trace. | 0.2 max | inch |
| R_S | 33 | Ω |
| R_T | 49.9 | Ω |

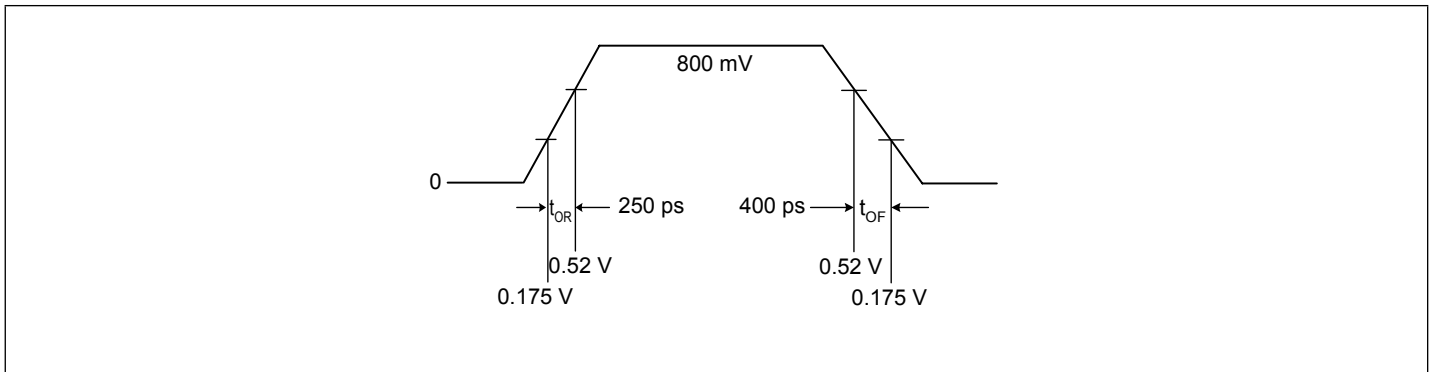
| Differential Routing on a Single PCB | Dimension or Value | Unit |
|---|---------------------|------|
| L4 length, route as coupled microstrip 100Ω differential trace. | 2 min to 16 max | inch |
| L4 length, route as coupled stripline 100Ω differential trace. | 1.8 min to 14.4 max | inch |

| Differential Routing to a PCI Express connector | Dimension or Value | Unit |
|---|-----------------------|------|
| L4 length, route as coupled microstrip 100Ω differential trace. | 0.25 min to 14 max | inch |
| L4 length, route as coupled stripline 100Ω differential trace. | 0.225 min to 12.6 max | inch |

PCI Express Device Routing



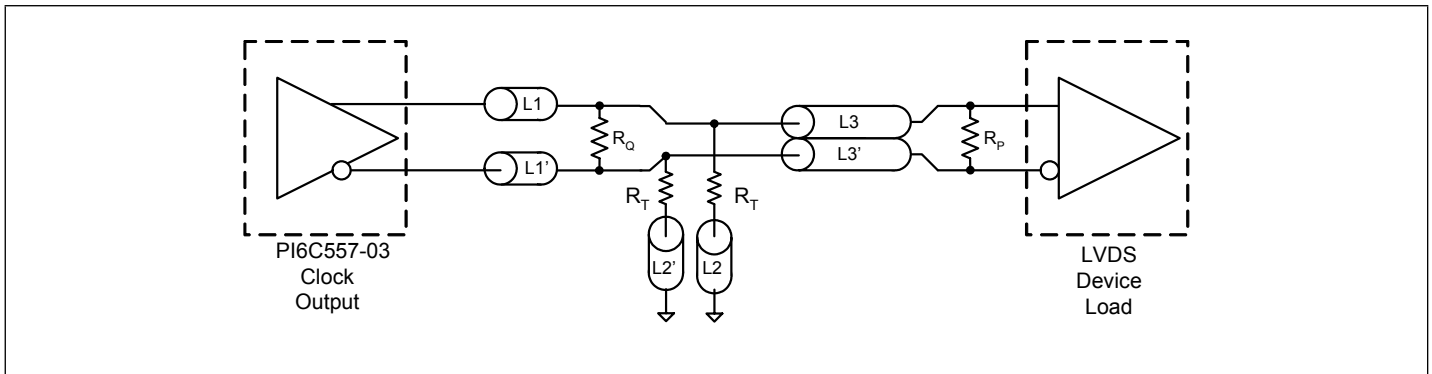
Typical PCI Express (HCSL) Waveform



Application Information

| LVDS Recommendations for Differential Routing | Dimension or Value | Unit |
|---|--------------------|------|
| L1 length, route as non-coupled 50Ω trace. | 0.5 max | inch |
| L2 length, route as non-coupled 50Ω trace. | 0.2 max | inch |
| RP | 100 | Ω |
| RQ | 100 | Ω |
| RT | 150 | Ω |
| L3 length, route as 100Ω differential trace. | | |
| L3 length, route as 100Ω differential trace. | | |

LVDS Device Routing



Maximum Ratings

(Above which useful life may be impaired. For user guidelines, not tested.)

| | |
|--|------------------------|
| Supply Voltage to Ground Potential | 5.5V |
| All Inputs and Outputs | -0.5V to $V_{DD}+0.5V$ |
| Ambient Operating Temperature | -40 to +85°C |
| Storage Temperature | -65 to +150°C |
| Junction Temperature | 150°C |
| Soldering Temperature | 260°C |
| EDS Protection (Input) | 2000 V min (HBM) |

Note:

Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Electrical Specifications

Recommended Operation Conditions

| Parameter | Min. | Typ. | Max. | Unit |
|---|------|------|------|------|
| Ambient Operating Temperature | -40 | | +85 | °C |
| Power Supply Voltage (measured in respect to GND) | +3.0 | | +3.6 | V |

DC Characteristics ($V_{DD} = 3.3V \pm 10\%$, $T_A = -40^\circ C$ to $+85^\circ C$)

| Symbol | Parameter | Conditions | Min. | Typ. | Max. | Unit |
|------------|-----------------------------------|--------------------------------|--------------------------------------|------|----------------|------------|
| V_{DD} | Supply Voltage | | 3.0 | 3.3 | 3.6 | V |
| V_{IH} | Input High Voltage ⁽¹⁾ | OE, S0, S1, SS0, SS1 | 2.0 | | $V_{DD} + 0.3$ | V |
| V_{IL} | Input Low Voltage ⁽¹⁾ | OE, S0, S1, SS0, SS1 | GND - 0.3 | | 0.8 | V |
| I_{IL} | Input Leakage Current | $0 < V_{in} < V_{DD}$ | With input pull-up and pull-downs | -20 | 20 | μA |
| | | | Without input pull-up and pull-downs | -5 | 5 | |
| I_{DD} | Operating Supply Current | $R_L = 50\Omega$, $C_L = 2pF$ | | | 95 | mA |
| I_{DDOE} | | OE = LOW | | | 50 | mA |
| C_{IN} | Input Capacitance | @ 55MHz | | | 7 | pF |
| C_{OUT} | Output Capacitance | @ 55MHz | | | 6 | pF |
| L_{PIN} | Pin Inductance | | | | 5 | nH |
| R_{OUT} | Output Resistance | CLK Outputs | 3.0 | | | k Ω |

Notes:

1. Single edge is monotonic when transitioning through region.

HCSL Output AC Characteristics ($V_{DD} = 3.3V \pm 10\%$, $T_A = -40^{\circ}C$ to $+85^{\circ}C$)

| Symbol | Parameter | Conditions | Min. | Typ. | Max. | Unit |
|------------------|---|---------------------------------------|------|------|------|---------|
| F_{IN} | Input Frequency | | | 25 | | MHz |
| V_{OUT} | Output Frequency | | 25 | | 200 | MHz |
| V_{OH} | Output High Voltage ^(1,2) | 100 MHz HCSL output @ $V_{DD} = 3.3V$ | 660 | 800 | 900 | mV |
| V_{OL} | Output Low Voltage ^(1,2) | | -150 | 0 | | mV |
| V_{CPA} | Crossing Point Voltage ^(1,2) | Absolute | 250 | 350 | 550 | mV |
| V_{CN} | Crossing Point Voltage ^(1,2,4) | Variation over all edges | | | 140 | mV |
| J_{CC} | Jitter, Cycle-to-Cycle ^(1,3) | | | 35 | 60 | ps |
| $J_{RMS2.0}$ | PCIe 2.0 RMS Jitter | PCIe 2.0 Test Method @ 100MHz Output | | | 3.1 | ps |
| $J_{RMS3.0}$ | PCIe 3.0 RMS Jitter | PLL L-BW @ 2M & 5M 1st H3 | | 1.75 | 3 | ps |
| | | PLL L-BW @ 2M & 4M 1st H3 | | 2.18 | 3 | ps |
| | | PLL H-BW @ 2M & 5M 1st H3 | | 0.45 | 1 | ps |
| | | PLL H-BW @ 2M & 4M 1st H3 | | 0.45 | 1 | ps |
| MF | Modulation Frequency | Spread Spectrum | 30 | 31.5 | 33 | kHz |
| t_{OR} | Rise Time ^(1,2) | From 0.175V to 0.525V | 175 | | 700 | ps |
| t_{OF} | Fall Time ^(1,2) | From 0.525V to 0.175V | 175 | | 700 | ps |
| T_{SKEW} | Skew between outputs | At Crossing Point Voltage | | | 50 | ps |
| $T_{DUTY-CYCLE}$ | Duty Cycle ^(1,3) | | 45 | | 55 | % |
| T_{OE} | Output Enable Time ⁽⁵⁾ | All outputs | | | 10 | μs |
| T_{OT} | Output Disable Time ⁽⁵⁾ | All outputs | | | 10 | μs |
| t_{STABLE} | From power-up to $V_{DD}=3.3V$ | From Power-up $V_{DD}=3.3V$ | | 3.0 | | ms |
| t_{SPREAD} | Setting period after spread change | Setting period after spread change | | 3.0 | | ms |

Notes:

- $R_L = 50\text{-Ohm}$ with $C_L = 2\text{ pF}$
- Single-ended waveform
- Differential waveform
- Measured at the crossing point
- CLK pins are tri-stated when OE is LOW

Thermal Characteristics

| Symbol | Parameter | Conditions | Min. | Typ. | Max. | Unit |
|---------------|--|------------|------|------|------|------|
| θ_{JA} | Thermal Resistance Junction to Ambient | Still air | | | 90 | °C/W |
| θ_{JC} | Thermal Resistance Junction to Case | | | | 24 | °C/W |

Recommended Crystal Specification

Pericom recommends:

- a) GC2500003 XTAL 49S/SMD(4.0 mm), 25M, CL=18pF, +/-30ppm
http://www.pericom.com/pdf/datasheets/se/GC_GF.pdf
- b) FY2500081, SMD 5x3.2(4P), 25M, CL=18pF, +/-30ppm
http://www.pericom.com/pdf/datasheets/se/FY_F9.pdf
- c) FL2500047, SMD 3.2x2.5(4P), 25M, CL=18pF, +/-20ppm
<http://www.pericom.com/pdf/datasheets/se/FL.pdf>

Packaging Mechanical: 16-Pin TSSOP (L)

| | |
|---|---|
| <p>The drawing shows three views of the 16-pin TSSOP (L) package. The top view shows a square body with 16 pins on the top edge and 16 pins on the bottom edge. Dimensions include a body width of 0.169 to 0.177 inches (4.3 to 4.5 mm), a pin pitch of 0.193 to 0.201 inches (4.9 to 5.1 mm), and a pin height of 0.047 inches maximum (1.20 mm). The side view shows a maximum height of 0.047 inches (1.20 mm) and a seating plane. The detail view shows a pin width of 0.0256 inches (0.65 mm) BSC, a pin thickness of 0.007 inches (0.19 mm), and a pin length of 0.002 to 0.006 inches (0.05 to 0.15 mm). Other dimensions include a body length of 0.45 to 0.75 inches (11.4 to 19.0 mm), a body thickness of 0.018 to 0.030 inches (0.45 to 0.75 mm), a body width of 0.252 inches (6.4 mm) BSC, and a lead thickness of 0.004 to 0.008 inches (0.09 to 0.20 mm).</p> | <p style="text-align: center;">DOCUMENT CONTROL NO. PD - 1310</p> <hr/> <p style="text-align: center;">REVISION: E DATE: 03/09/05</p> |
| <p>Note:</p> <ol style="list-style-type: none"> 1. Package Outline Exclusive of Mold Flash and Metal Burr 2. Controlling dimensions in millimeters 3. Ref: JEDEC MO-153F/AB | <div style="text-align: center;"> <p>PERICOM[®]</p> <p>Pericom Semiconductor Corporation 3545 N. 1st Street, San Jose, CA 95134 1-800-435-2335 • www.pericom.com</p> </div> <hr/> <p>DESCRIPTION: 16-Pin, 173-Mil Wide, TSSOP</p> <hr/> <p>PACKAGE CODE: L</p> |

Note: For latest package info, please check: <http://www.pericom.com/products/packaging/mechanicals.php>

Packaging Mechanical: 16-Pin QSOP (Q)

| | |
|--|--|
| <p style="text-align: center;">X.XX DENOTES DIMENSIONS IN MILLIMETERS X.XX</p> <p>Note: 1) Controlling dimensions in inches. 2) Ref: JEDEC MO-137B/AB. 3) Dimensions do not include mold flash, protrusions or gate burrs</p> | <p>DOCUMENT CONTROL NO. PD - 1201</p> <hr/> <p>REVISION: G</p> <p>DATE: 11/07/07</p> |
| <p>Pericom Semiconductor Corporation 3545 N. 1st Street, San Jose, CA 95134 1-800-435-2335 • www.pericom.com</p> | |
| <p>DESCRIPTION: 16-Pin 150-Mil Wide QSOP</p> <hr/> <p>PACKAGE CODE: Q</p> | |

Note: For latest package info, please check: <http://www.pericom.com/products/packaging/mechanicals.php>

Ordering Information

| Ordering Code | Package Code | Package Type |
|---------------|--------------|-------------------------------|
| PI6C557-03BLE | L | Pb-free & Green, 16-pin TSSOP |
| PI6C557-03BQE | Q | Pb-free & Green, 16-pin QSOP |

Notes:

- Thermal characteristics can be found on the company web site at www.pericom.com/packaging/
- "E" denotes Pb-free and Green
- Adding an "X" at the end of the ordering code denotes tape and reel packaging