1.5 Ω On Resistance, ±15 V/12 V/±5 V, *i*CMOS, Dual SPDT Switch

Data Sheet

ADG1436

FEATURES

- 1.5 Ω on resistance
- 0.3 Ω on-resistance flatness
- 0.1 Ω on-resistance match between channels
- Continuous current per channel
  - LFCSP package: up to 400 mA
  - TSSOP package: up to 260 mA
- Fully specified at +12 V, ±15 V, and ±5 V
- No V_L supply required
- 3 V logic-compatible inputs
- Rail-to-rail operation
- 16-lead TSSOP and 4 mm × 4 mm, 16-lead LFCSP packages

APPLICATIONS

- Automatic test equipment
- Data acquisition systems
- Battery-powered systems
- Sample-and-hold systems
- Audio signal routing
- Communication systems
- Relay replacement

FUNCTIONAL BLOCK DIAGRAMS

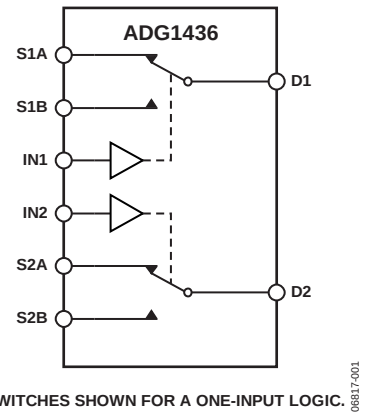

Figure 1. TSSOP Package

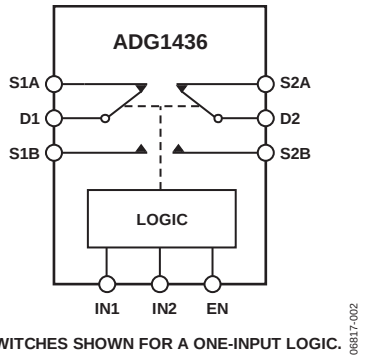

Figure 2. LFCSP Package

GENERAL DESCRIPTION

The ADG1436 is a monolithic CMOS device containing two independently selectable SPDT switches. An EN input on the LFCSP package enables or disable the device. When disabled, all channels are switched off. Each switch conducts equally well in both directions when on and has an input signal range that extends to the supplies. In the off condition, signal levels up to the supplies are blocked. Both switches exhibit break-before-make switching action for use in multiplexer applications.

The ADG1436 is designed on an *i*CMOS® process. *i*CMOS (industrial-CMOS) is a modular manufacturing process combining high voltage CMOS (complementary metal-oxide semiconductor) and bipolar technologies. It enables the development of a wide range of high performance analog ICs capable of 33 V operation in a footprint that no previous generation of high voltage parts has been able to achieve. Unlike analog ICs using conventional CMOS processes, *i*CMOS components can tolerate high supply voltages while providing increased performance, dramatically lower power consumption, and reduced package size.

The on-resistance profile is very flat over the full analog input range, ensuring excellent linearity and low distortion when switching audio signals. *i*CMOS construction ensures ultralow power dissipation, making the part ideally suited for portable and battery-powered instruments.

PRODUCT HIGHLIGHTS

1. 2.6 Ω maximum on resistance over temperature.
2. Minimum distortion.
3. Ultralow power dissipation: <0.03 µW.
4. 16-lead TSSOP and 16-lead 4 mm × 4 mm LFCSP packages.

Rev. B

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REVISION HISTORY

9/2016—Rev. A to Rev. B

Changes to Figure 4 8
Updated Outline Dimensions 16
Changes to Ordering Guide 16

3/2009—Rev. 0 to Rev. A

Change to I_{DD} Parameter, Table 1 3
Change to I_{DD} Parameter, Table 2 4

7/2008—Revision 0: Initial Version

SPECIFICATIONS

15 V DUAL SUPPLY

V_{DD} = 15 V ± 10%, V_{SS} = −15 V ± 10%, GND = 0 V, unless otherwise noted.

Table 1.

Parameter	25°C	−40°C to +85°C	−40°C to +125°C	Unit	Test Conditions/Comments
ANALOG SWITCH					
Analog Signal Range			V_{DD} to V_{SS}	V	
On Resistance (R_{ON})	1.5			Ω typ	V_S = ±10 V, I_S = −10 mA; see Figure 23
	1.8	2.3	2.6	Ω max	V_{DD} = +13.5 V, V_{SS} = −13.5 V
On-Resistance Match Between Channels (ΔR_{ON})	0.1			Ω typ	V_S = ±10 V, I_S = −10 mA
	0.18	0.19	0.21	Ω max	
On-Resistance Flatness ($R_{FLAT(ON)}$)	0.28			Ω typ	V_S = ±10 V, I_S = −10 mA
	0.36	0.4	0.45	Ω max	
LEAKAGE CURRENTS					V_{DD} = +16.5 V, V_{SS} = −16.5 V
Source Off Leakage, I_S (Off)	±0.04			nA typ	V_S = ±10 V, V_S = ±10 V; see Figure 24
	±0.55	±2	±12.5	nA max	
Drain Off Leakage, I_D (Off)	±0.04			nA typ	V_S = ±10 V, V_S = ±10 V; see Figure 24
	±0.55	±2	±12.5	nA max	
Channel On Leakage, I_D, I_S (On)	±0.1			nA typ	V_S = V_D = ±10 V; see Figure 25
	±2	±4	±35	nA max	
DIGITAL INPUTS					
Input High Voltage, V_{INH}			2.0	V min	
Input Low Voltage, V_{INL}			0.8	V max	
Input Current, I_{INL} or I_{INH}	0.005			μA typ	V_{IN} = V_{GND} or V_{DD}
			±0.1	μA max	
Digital Input Capacitance, C_{IN}	3.5			pF typ	
DYNAMIC CHARACTERISTICS[1]					
Transition Time, $t_{TRANSITION}$	125			ns typ	R_L = 300 Ω, C_L = 35 pF
	170	215	245	ns max	V_S = +10 V; see Figure 30
t_{ON} (EN)	95			ns typ	R_L = 300 Ω, C_L = 35 pF
	120	140	155	ns max	V_S = 10 V; see Figure 30
t_{OFF} (EN)	105			ns typ	R_L = 300 Ω, C_L = 35 pF
	130	150	170	ns max	V_S = 10 V; see Figure 30
Break-Before-Make Time Delay, t_{BBM}	20			ns typ	R_L = 300 Ω, C_L = 35 pF
			10	ns min	V_{S1} = V_{S2} = +10 V; see Figure 31
Charge Injection	−20			pC typ	V_S = 0 V, R_S = 0 Ω, C_L = 1 nF; see Figure 33
Off Isolation	−80			dB typ	R_L = 50 Ω, C_L = 5 pF, f = 100 kHz; see Figure 26
Channel-to-Channel Crosstalk	−80			dB typ	R_L = 50 Ω, C_L = 5 pF, f = 100 kHz; see Figure 27
Total Harmonic Distortion + Noise	0.011			% typ	R_L = 110 Ω, 15 V p-p, f = 20 Hz to 20 kHz; see Figure 29
−3 dB Bandwidth	110			MHz typ	R_L = 50 Ω, C_L = 5 pF; see Figure 28
Insertion Loss	−0.18			dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz; see Figure 28
C_S (Off)	23			pF typ	f = 1 MHz, V_S = 0 V
C_D (Off)	50			pF typ	f = 1 MHz, V_S = 0 V
C_D, C_S (On)	120			pF typ	f = 1 MHz, V_S = 0 V
POWER REQUIREMENTS					V_{DD} = +16.5 V, V_{SS} = −16.5 V
I_{DD}	0.001			μA typ	Digital Inputs = 0 V or V_{DD}
			1	μA max	
I_{DD}	170			μA typ	Digital Input = 5 V
			285	μA max	
I_{SS}	0.001			μA typ	Digital Inputs = 0 V, 5 V, or V_{DD}
			1.0	μA max	
V_{DD}/V_{SS}			±4.5/±16.5	V min/max	GND = 0 V

[1] Guaranteed by design, not subject to production test.

12 V SINGLE SUPPLY

V_{DD} = 12 V ± 10%, V_{SS} = 0 V, GND = 0 V, unless otherwise noted.

Table 2.

Parameter	25°C	−40°C to +85°C	−40°C to +125°C	Unit	Test Conditions/Comments
ANALOG SWITCH					
Analog Signal Range			0 V to V_{DD}	V	
On Resistance (R_{ON})	2.8			Ω typ	V_S = 0 V to 10 V, I_S = −10 mA; see Figure 23
	3.5	4.3	4.8	Ω max	V_{DD} = +10.8 V, V_{SS} = 0 V
On-Resistance Match Between Channels (ΔR_{ON})	0.13			Ω typ	V_S = 0 V to 10 V, I_S = −10 mA
	0.21	0.23	0.25	Ω max	
On-Resistance Flatness ($R_{FLAT(ON)}$)	0.6			Ω typ	V_S = 0 V to 10 V, I_S = −10 mA
	1.1	1.2	1.3	Ω max	
LEAKAGE CURRENTS					V_{DD} = 13.2 V, V_{SS} = 0 V
Source Off Leakage, I_S (Off)	±0.04			nA typ	V_S = 1 V/10 V, V_D = 10 V/1 V; see Figure 24
	±0.55	±2	±12.5	nA max	
Drain Off Leakage, I_D (Off)	±0.04			nA typ	V_S = 1 V/10 V, V_D = 10 V/1 V; see Figure 24
	±0.55	±2	±12.5	nA max	
Channel On Leakage, I_D, I_S (On)	±0.1			nA typ	V_S = V_D = 1 V or 10 V; see Figure 25
	±1	±4	±35	nA max	
DIGITAL INPUTS					
Input High Voltage, V_{INH}			2.0	V min	
Input Low Voltage, V_{INL}			0.8	V max	
Input Current, I_{INL} or I_{INH}	0.001			μA typ	V_{IN} = V_{GND} or V_{DD}
			±0.1	μA max	
Digital Input Capacitance, C_{IN}	3.5			pF typ	
DYNAMIC CHARACTERISTICS[1]					
Transition Time, $t_{TRANSITION}$	200			ns typ	R_L = 300 Ω, C_L = 35 pF
	270	320	350	ns max	V_S = 8 V; see Figure 30
t_{ON} (EN)	175			ns typ	R_L = 300 Ω, C_L = 35 pF
	235	280	310	ns max	V_S = 8 V; see Figure 30
t_{OFF} (EN)	105			ns typ	R_L = 300 Ω, C_L = 35 pF
	145	175	195	ns max	V_S = 8 V; see Figure 30
Break-Before-Make Time Delay, t_{BBM}	70			ns typ	R_L = 300 Ω, C_L = 35 pF
			10	ns min	V_{S1} = V_{S2} = 8 V; see Figure 31
Charge Injection	30			pC typ	V_S = 6 V, R_S = 0 Ω, C_L = 1 nF; see Figure 33
Off Isolation	−80			dB typ	R_L = 50 Ω, C_L = 5 pF, f = 100 kHz; see Figure 26;
Channel-to-Channel Crosstalk	−80			dB typ	R_L = 50 Ω, C_L = 5 pF, f = 100 kHz; see Figure 27
−3 dB Bandwidth	78			MHz typ	R_L = 50 Ω, C_L = 5 pF; see Figure 28
Insertion Loss	−0.3			dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz; see Figure 28
C_S (Off)	40			pF typ	f = 1 MHz, V_S = 6 V
C_D (Off)	80			pF typ	f = 1 MHz, V_S = 6 V
C_D, C_S (On)	140			pF typ	f = 1 MHz, V_S = 6 V
POWER REQUIREMENTS					V_{DD} = 13.2 V
I_{DD}	0.001			μA typ	Digital inputs = 0 V or V_{DD}
			1.0	μA max	
I_{DD}	170			μA typ	Digital inputs = 5 V
			285	μA max	
V_{DD}			5/16.5	V min/max	GND = 0 V, V_{SS} = 0 V

[1] Guaranteed by design, not subject to production test.

5 V DUAL SUPPLY

V_{DD} = 5 V ± 10%, V_{SS} = −5 V ± 10%, GND = 0 V, unless otherwise noted.

Table 3.

Parameter	25°C	−40°C to +85°C	−40°C to +125°C	Unit	Test Conditions/Comments
ANALOG SWITCH					
Analog Signal Range			V_{DD} to V_{SS}	V	
On Resistance (R_{ON})	3.3			Ω typ	V_S = ±4.5 V, I_S = −10 mA; see Figure 23
	4	4.9	5.4	Ω max	V_{DD} = +4.5 V, V_{SS} = −4.5 V
On-Resistance Match Between Channels (ΔR_{ON})	0.13			Ω typ	V_S = ±4.5 V, I_S = −10 mA
	0.22	0.23	0.25	Ω max	
On-Resistance Flatness ($R_{FLAT(ON)}$)	0.9			Ω typ	V_S = ±4.5 V, I_S = −10 mA
	1.1	1.24	1.31	Ω max	
LEAKAGE CURRENTS					V_{DD} = +5.5 V, V_{SS} = −5.5 V
Source Off Leakage, I_S (Off)	±0.03			nA typ	V_S = ±4.5 V, V_D = ∓4.5 V; see Figure 24
	±0.2	±1	±12.5	nA max	
Drain Off Leakage, I_D (Off)	±0.03			nA typ	V_S = ±4.5 V, V_D = ∓4.5 V; see Figure 24
	±0.2	±1	±12.5	nA max	
Channel On Leakage, I_D, I_S (On)	±0.05			nA typ	V_S = V_D = ±4.5V; see Figure 25
	±0.25	±1.5	±35	nA max	
DIGITAL INPUTS					
Input High Voltage, V_{INH}			2.0	V min	
Input Low Voltage, V_{INL}			0.8	V max	
Input Current, I_{INL} or I_{INH}	0.001			μA typ	V_{IN} = V_{GND} or V_{DD}
			±0.1	μA max	
Digital Input Capacitance, C_{IN}	3.5			pF typ	
DYNAMIC CHARACTERISTICS[1]					
Transition Time, $t_{TRANSITION}$	310			ns typ	R_L = 300 Ω, C_L = 35 pF
	445	510	565	ns max	V_S = 3 V; see Figure 30
t_{ON} (EN)	255			ns typ	R_L = 300 Ω, C_L = 35 pF
	355	415	460	ns max	V_S = 3 V; see Figure 30
t_{OFF} (EN)	215			ns typ	R_L = 300 Ω, C_L = 35 pF
	305	355	400	ns max	V_S = 3 V; see Figure 30
Break-Before-Make Time Delay, t_{BBM}	80			ns typ	R_L = 300 Ω, C_L = 35 pF
			10	ns min	V_{S1} = V_{S2} = 3 V; see Figure 31
Charge Injection	30			pC typ	V_S = 0 V, R_S = 0 Ω, C_L = 1 nF; see Figure 33
Off Isolation	−80			dB typ	R_L = 50 Ω, C_L = 5 pF, f = 100 kHz; see Figure 26
Channel-to-Channel Crosstalk	−80			dB typ	R_L = 50 Ω, C_L = 5 pF, f = 100 kHz; see Figure 27
Total Harmonic Distortion + Noise	0.03			% typ	R_L = 110 Ω, 2.5 V pp, f = 20 Hz to 20 kHz; see Figure 29
−3 dB Bandwidth	85			MHz typ	R_L = 50 Ω, C_L = 5 pF; see Figure 28
Insertion Loss	−0.28			dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz; see Figure 28
C_S (Off)	33			pF typ	V_S = 0 V, f = 1 MHz
C_D (Off)	65			pF typ	V_S = 0 V, f = 1 MHz
C_D, C_S (On)	145			pF typ	V_S = 0 V, f = 1 MHz
POWER REQUIREMENTS					V_{DD} = +5.5 V, V_{SS} = −5.5 V
I_{DD}	0.001			μA typ	Digital inputs = 0 V or V_{DD}
			1.0	μA max	
I_{SS}	0.001			μA typ	Digital inputs = 0 V or V_{DD}
			1.0	μA max	
V_{DD}/V_{SS}			±4.5/±16.5	V min/max	GND = 0 V

[1] Guaranteed by design, not subject to production test.

CONTINUOUS CURRENT PER CHANNEL

Table 4.

Parameter	25°C	85°C	125°C	Unit	Test Conditions/Comments
CONTINUOUS CURRENT PER CHANNEL[1]					
15 V Dual Supply					V_{DD} = +13.5 V, V_{SS} = −13.5 V
ADG1436 TSSOP	260	170	100	mA max	
ADG1436 LFCSP	400	250	120	mA max	
12 V Single Supply					V_{DD} = 10.8 V, V_{SS} = 0 V
ADG1436 TSSOP	240	160	100	mA max	
ADG1436 LFCSP	350	240	120	mA max	
5 V Dual Supply					V_{DD} = +4.5 V, V_{SS} = −4.5 V
ADG1436 TSSOP	240	160	100	mA max	
ADG1436 LFCSP	300	240	120	mA max	

[1] Guaranteed by design, not subject to production test.

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted.

Table 5.

Parameter	Ratings
V_{DD} to V_{SS}	35 V
V_{DD} to GND	−0.3 V to +25 V
V_{SS} to GND	+0.3 V to −25 V
Analog Inputs[1]	V_{SS} − 0.3 V to V_{DD} + 0.3 V or 30 mA, whichever occurs first
Digital Inputs[1]	GND − 0.3 V to V_{DD} + 0.3 V or 30 mA, whichever occurs first
Peak Current, S or D	600 mA (pulsed at 1 ms, 10% duty cycle maximum)
Continuous Current per Channel, S or D[2]	Data + 15%
Operating Temperature Range	
Automotive (Y Version)	−40°C to +125°C
Storage Temperature Range	−65°C to +150°C
Junction Temperature	150°C
16-Lead TSSOP, θ_{JA} Thermal Impedance (4-Layer Board)	112°C/W
16-Lead LFCSP, θ_{JA} Thermal Impedance	30.4°C/W
Reflow Soldering Peak Temperature, Pb Free	260(+0/−5)°C

[1] Over voltages at IN, S, and D are clamped by internal diodes. Current must be limited to the maximum ratings given.
[2] See data given in Table 4.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

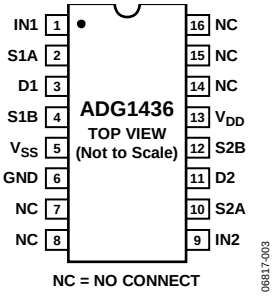


Figure 3.TSSOP Pin Configuration

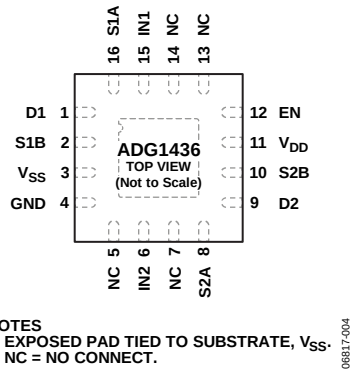


Figure 4. LFCSP Pin Configuration

Table 6. Pin Function Descriptions

Pin No.			
TSSOP	**LFCSP**	**Mnemonic**	**Function**
1	15	IN1	Logic Control Input.
2	16	S1A	Source Terminal. Can be an input or output.
3	1	D1	Drain Terminal. Can be an input or output.
4	2	S1B	Source Terminal. Can be an input or output.
5	3	V_{SS}	Most Negative Power Supply Potential.
6	4	GND	Ground (0 V) Reference.
7, 8, 14 to 16	5, 7, 13, 14	NC	No Connect.
9	6	IN2	Logic Control Input.
10	8	S2A	Source Terminal. Can be an input or output.
11	9	D2	Drain Terminal. Can be an input or output.
12	10	S2B	Source Terminal. Can be an input or output.
13	11	V_{DD}	Most Positive Power Supply Potential.
N/A	12	EN	Active High Digital Input. When this pin is low, the device is disabled and all switches are off. When this pin is high, INx logic inputs determine the on switches.

TRUTH TABLE FOR SWITCHES

Table 7. ADG1436 TSSOP Truth Table

INx	SxA	SxB
0	Off	On
1	On	Off

Table 8. ADG1436 LFCSP Truth Table

EN	INx	SxA	SxB
0	X	Off	Off
1	0	Off	On
1	1	On	Off

TYPICAL PERFORMANCE CHARACTERISTICS

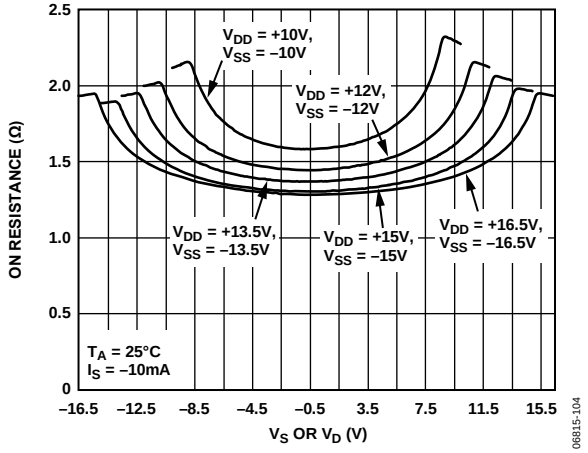


Figure 5. On Resistance vs. V_D or V_S, Dual Supply

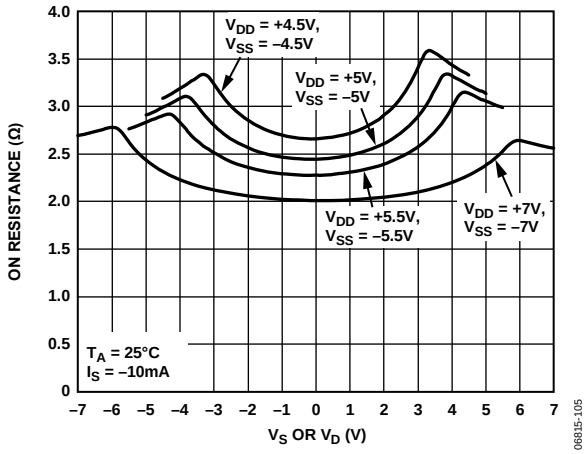


Figure 6. On Resistance vs. V_D or V_S, Dual Supply

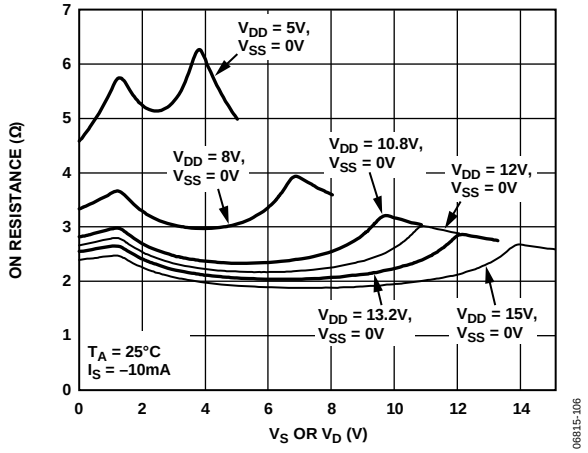


Figure 7. On Resistance vs. V_D or V_S, Single Supply

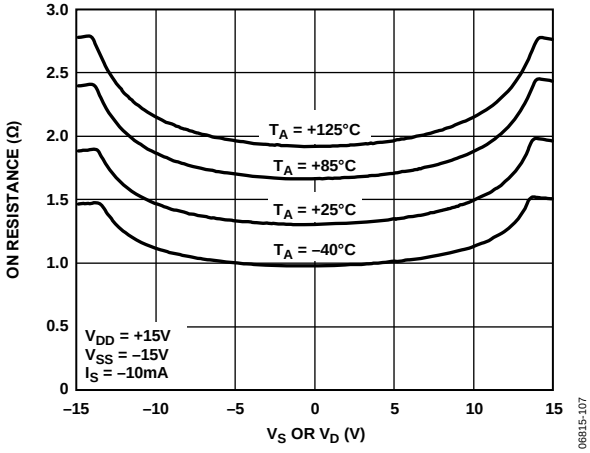


Figure 8. On Resistance vs. V_D or V_S for Different Temperatures, 15 V Dual Supply

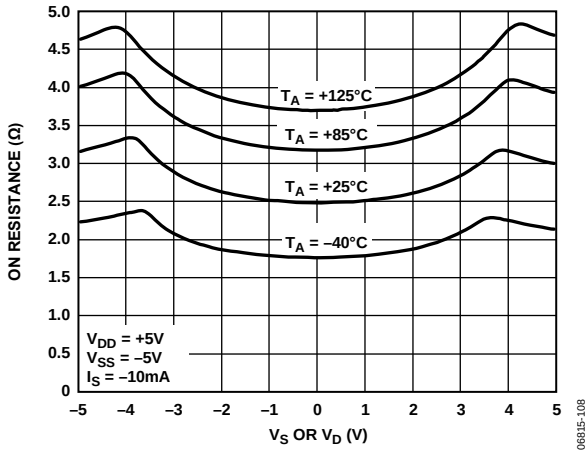


Figure 9. On Resistance vs. V_D or V_S for Different Temperatures, 5 V Dual Supply

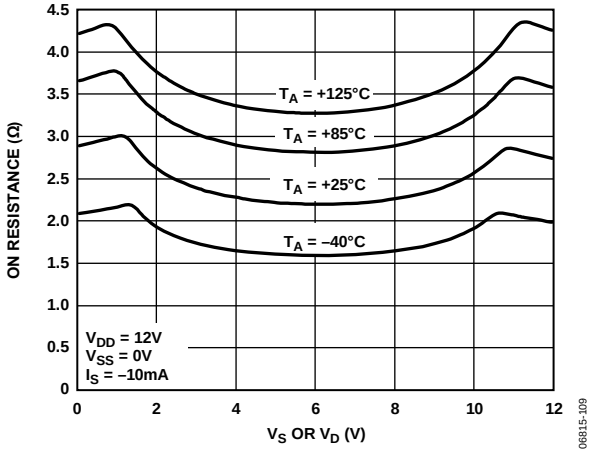


Figure 10. On Resistance vs. V_D or V_S for Different Temperatures, Single Supply

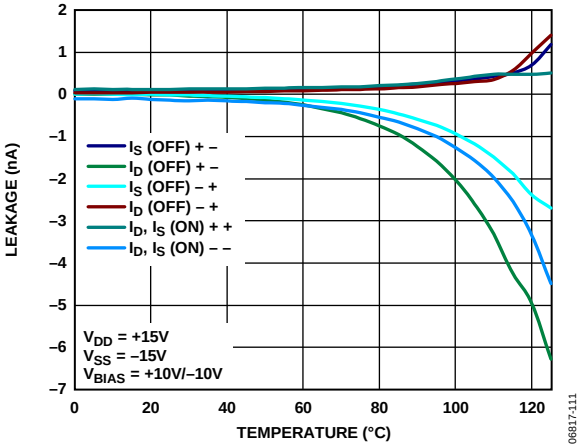


Figure 11. Leakage Currents vs. Temperature, 15 V Dual Supply

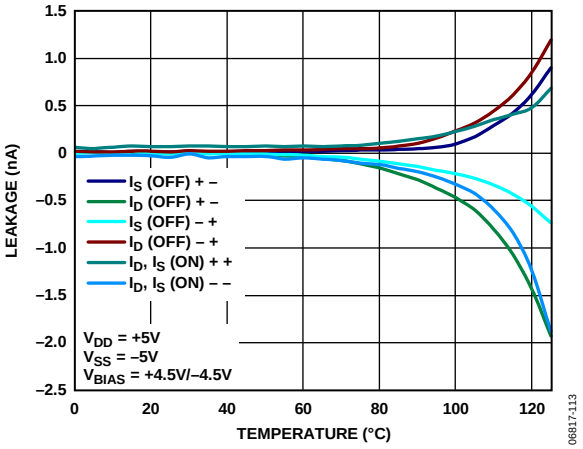


Figure 12. Leakage Currents vs. Temperature, 5 V Dual Supply

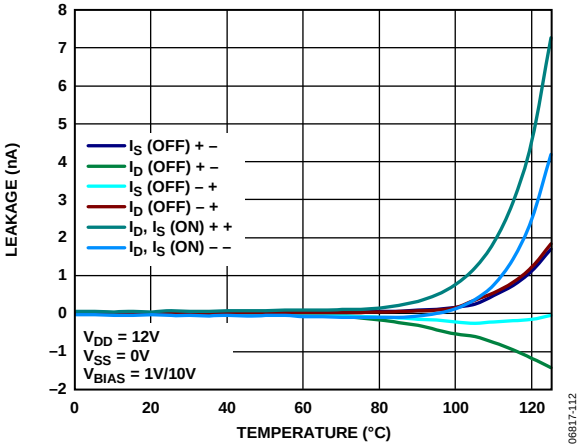


Figure 13. Leakage Currents vs. Temperature, 12 V Single Supply

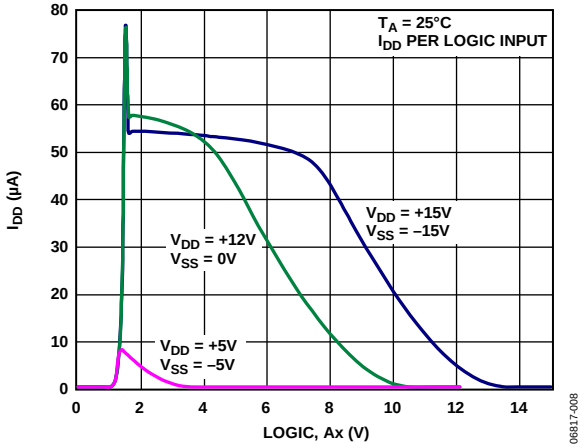


Figure 14. I_{DD} vs. Logic Level

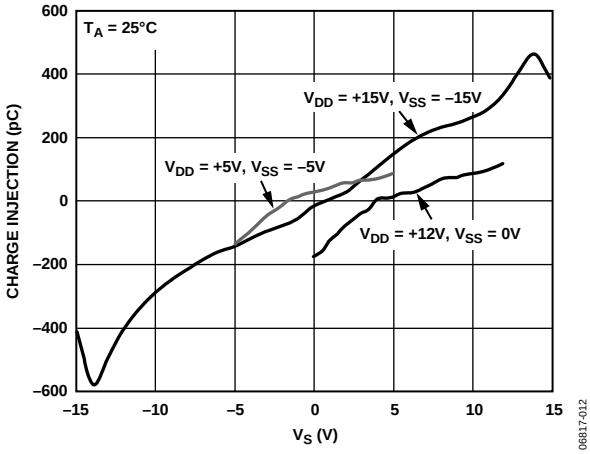


Figure 15. Charge Injection vs. Source Voltage

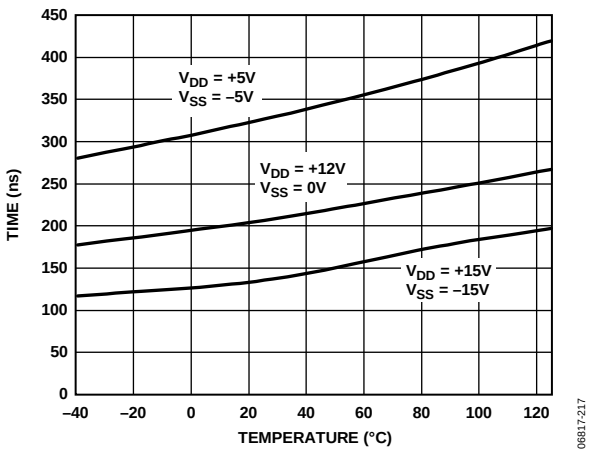


Figure 16. $t_{TRANSITION}$ Time vs. Temperature

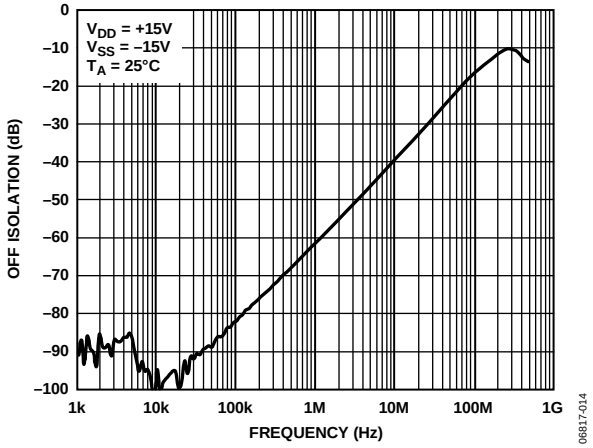


Figure 17. Off Isolation vs. Frequency

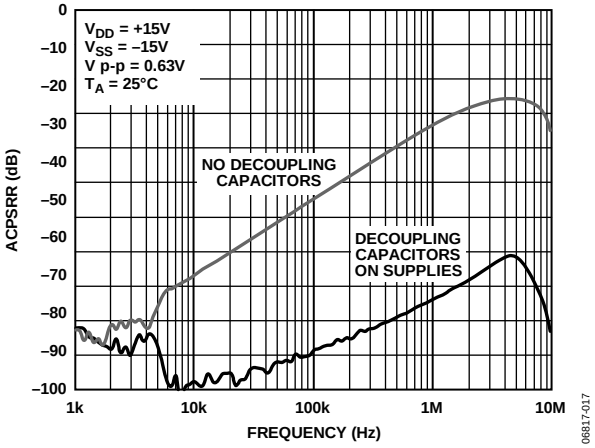


Figure 20. ACPSRR vs. Frequency

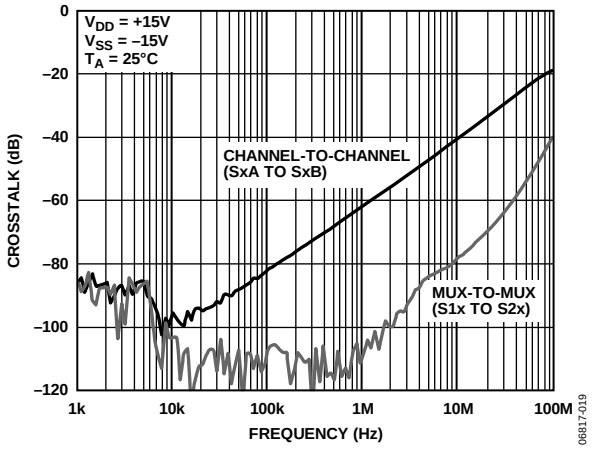


Figure 18. Crosstalk vs. Frequency

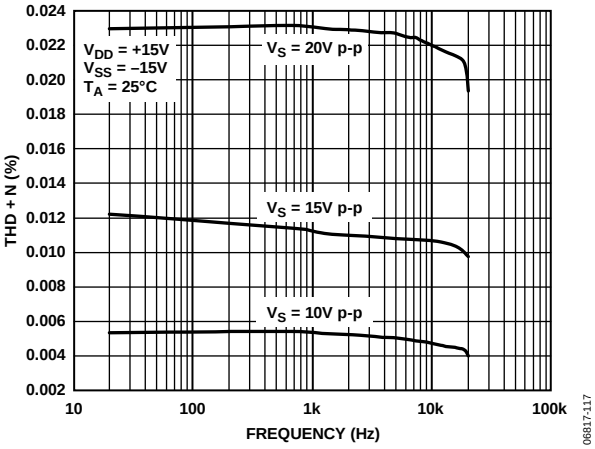


Figure 21. THD + N vs. Frequency, 15 V Dual Supply

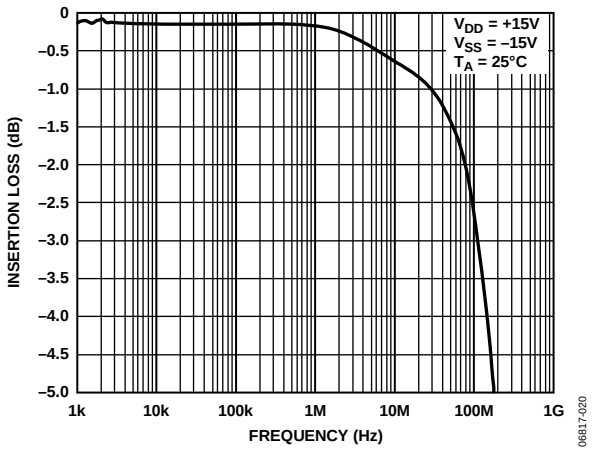


Figure 19. On Response vs. Frequency

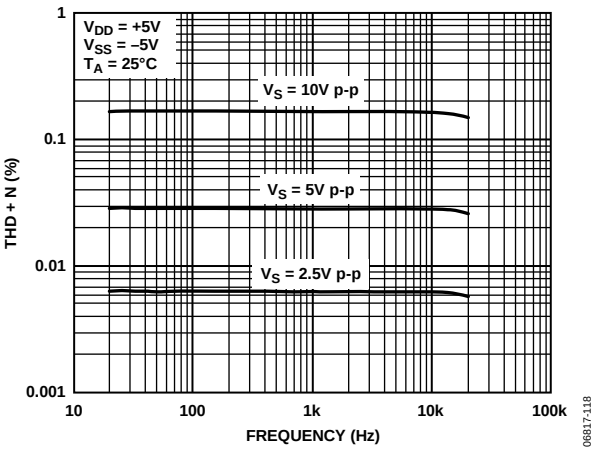


Figure 22. THD + N vs. Frequency, 5 V Dual Supply

TERMINOLOGY

I_{DD}
The positive supply current.

I_{SS}
The negative supply current.

V_D, V_S
The analog voltage on Terminal D and Terminal S.

R_{ON}
The ohmic resistance between Terminal D and Terminal S.

$R_{FLAT(ON)}$
Flatness that is defined as the difference between the maximum and minimum value of on resistance measured over the specified analog signal range.

I_S (Off)
The source leakage current with the switch off.

I_D (Off)
The drain leakage current with the switch off.

I_D, I_S (On)
The channel leakage current with the switch on.

V_{INL}
The maximum input voltage for Logic 0.

V_{INH}
The minimum input voltage for Logic 1.

I_{INL}, I_{INH}
The input current of the digital input.

C_S (Off)
The off-switch source capacitance, which is measured with reference to ground.

C_D (Off)
The off-switch drain capacitance, which is measured with reference to ground.

C_D, C_S (On)
The on-switch capacitance, which is measured with reference to ground.

C_{IN}
The digital input capacitance.

$t_{TRANSITION}$
The delay time between the 50% and 90% points of the digital input and switch on condition when switching from one address state to another.

Charge Injection
A measure of the glitch impulse transferred from the digital input to the analog output during switching.

Off Isolation
A measure of unwanted signal coupling through an off switch.

Crosstalk
A measure of unwanted signal that is coupled through from one channel to another as a result of parasitic capacitance.

Bandwidth
The frequency at which the output is attenuated by 3 dB.

On Response
The frequency response of the on switch.

Insertion Loss
The loss due to the on resistance of the switch.

THD + N
The ratio of the harmonic amplitude plus noise of the signal to the fundamental.

TEST CIRCUITS

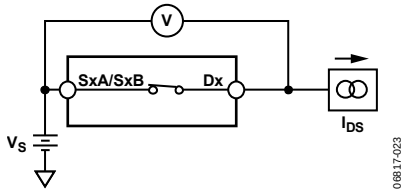


Figure 23. On Resistance

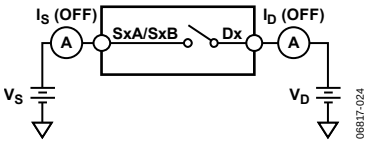


Figure 24. Off Leakage

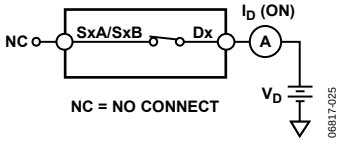


Figure 25. On Leakage

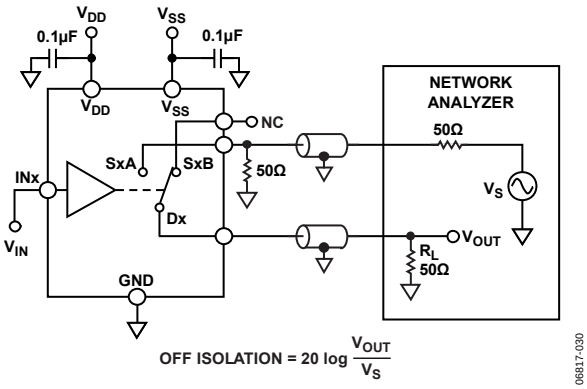


Figure 26. Off Isolation

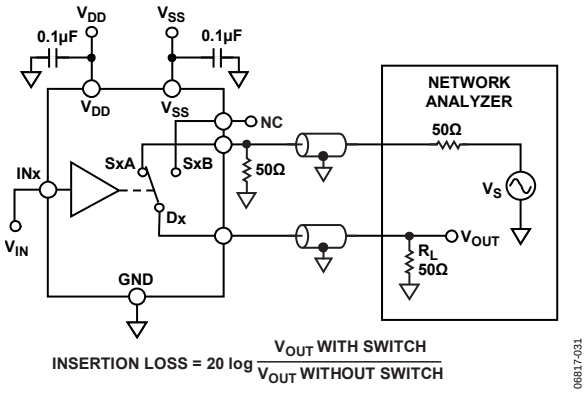


Figure 27. Channel-to-Channel Crosstalk

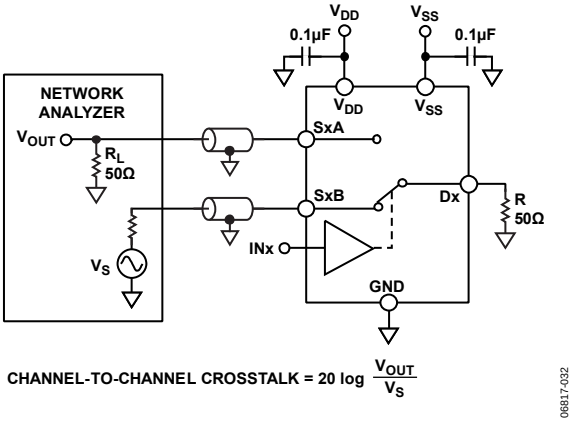


Figure 28. Bandwidth

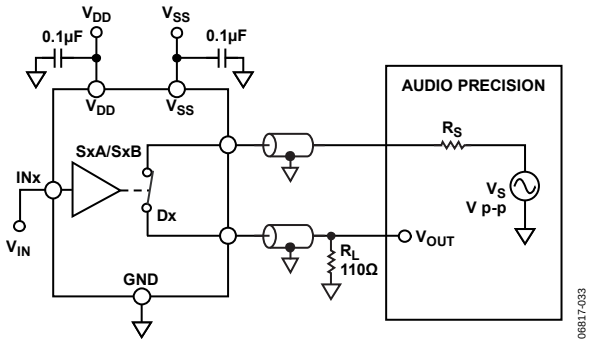


Figure 29. THD + Noise

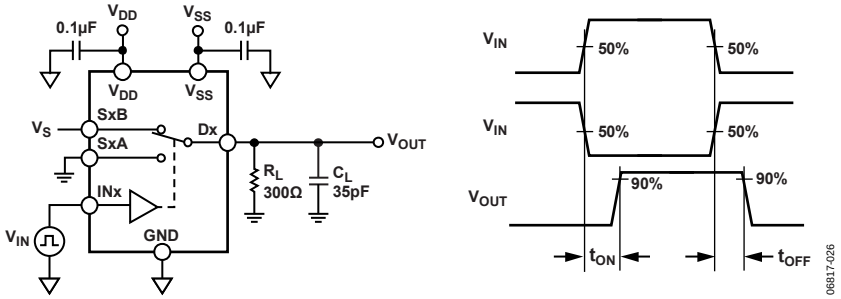


Figure 30. Switching Times

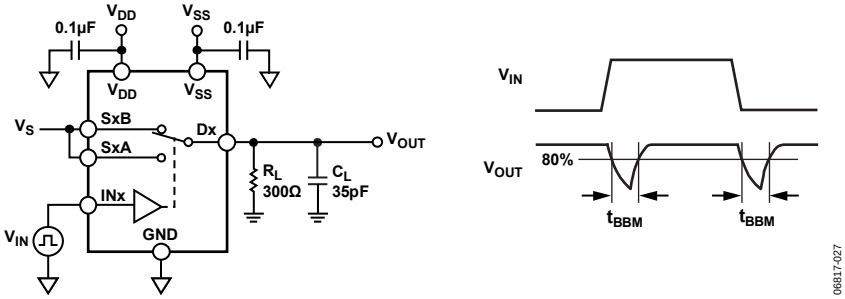


Figure 31. Break-Before-Make Time Delay

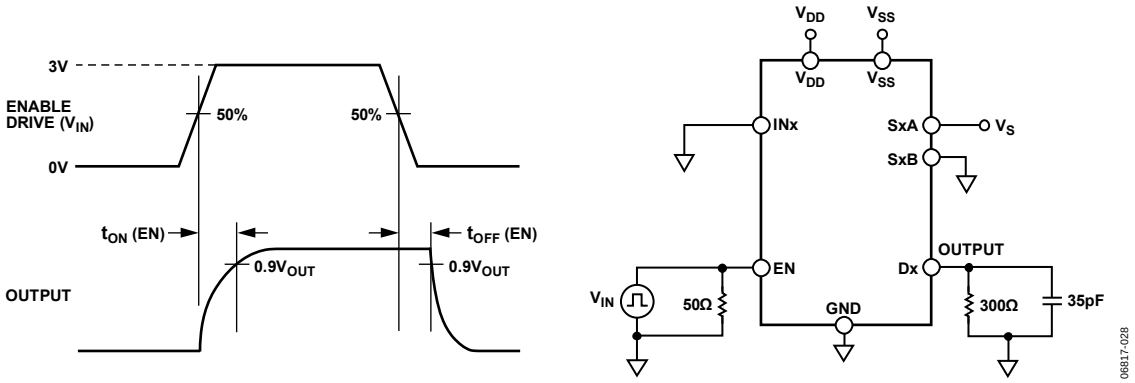


Figure 32. Enable Delay, t_{ON} (EN), t_{OFF} (EN)

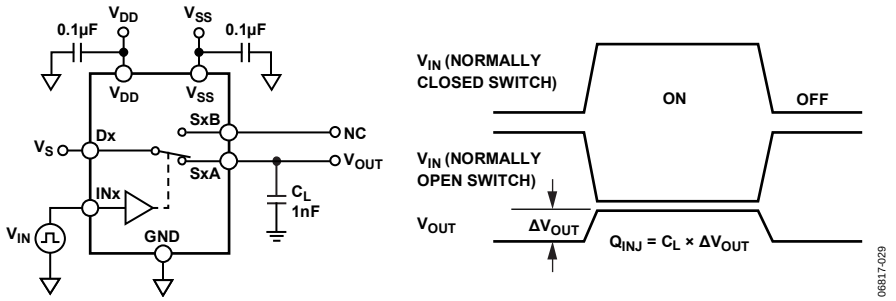
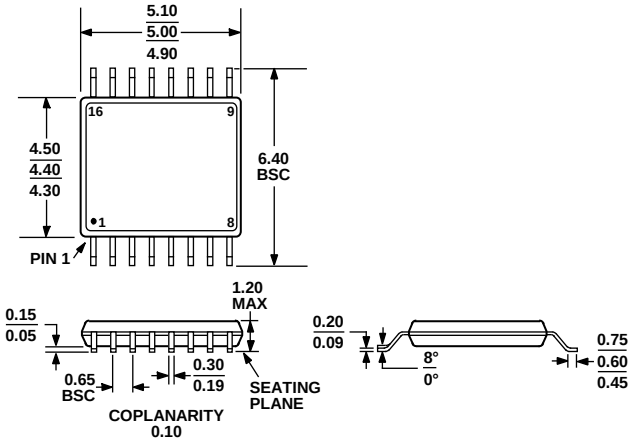


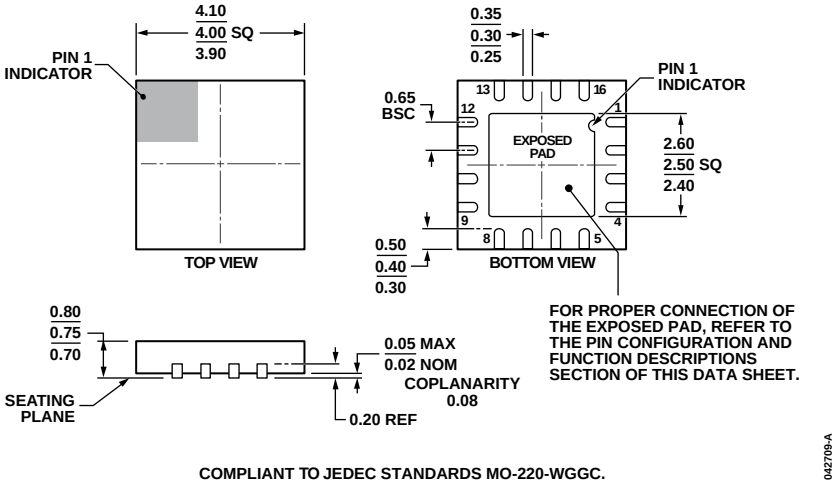
Figure 33. Charge Injection

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-153-AB

Figure 34. 16-Lead Thin Shrink Small Outline Package [TSSOP]
(RU-16)
Dimensions shown in millimeters



COMPLIANT TO JEDEC STANDARDS MO-220-WGGC.

Figure 35. 16-Lead Lead Frame Chip Scale Package [LFCSP]
4 mm × 4 mm Body and 0.75 mm Package Height
(CP-16-26)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option
ADG1436YRUZ	−40°C to +125°C	16-Lead Thin Shrink Small Outline Package [TSSOP]	RU-16
ADG1436YRUZ-REEL7	−40°C to +125°C	16-Lead Thin Shrink Small Outline Package [TSSOP]	RU-16
ADG1436YCPZ-REEL	−40°C to +125°C	16-Lead Lead Frame Chip Scale Package [LFCSP]	CP-16-26
ADG1436YCPZ-REEL7	−40°C to +125°C	16-Lead Lead Frame Chip Scale Package [LFCSP]	CP-16-26

[1] Z = RoHS Compliant Part.