



FEATURES

- 9.5 Ω on resistance at 25°C
- Up to 300 mA of continuous current
- Fully specified at ±15 V/+12 V/±5 V
- 3 V logic-compatible inputs
- Rail-to-rail operation
- Break-before-make switching action
- 28-lead TSSOP and 32-lead, 5 mm × 5 mm LFCSP

APPLICATIONS

- Medical equipment
- Audio and video routing
- Automatic test equipment
- Data acquisition systems
- Battery-powered systems
- Sample-and-hold systems
- Communication systems

GENERAL DESCRIPTION

The **ADG1406** and **ADG1407** are monolithic iCMOS® analog multiplexers comprising 16 single channels and eight differential channels, respectively. The **ADG1406** switches one of 16 inputs to a common output, as determined by the 4-bit binary address lines (A0, A1, A2, and A3). The **ADG1407** switches one of eight differential inputs to a common differential output, as determined by the 3-bit binary address lines (A0, A1, and A2). An EN input on both devices enables or disables the device. When disabled, all channels switch off. When on, each channel conducts equally well in both directions and has an input signal range that extends to the supplies.

The industrial CMOS (iCMOS) modular manufacturing process combines high voltage complementary metal-oxide semiconductor (CMOS) and bipolar technologies. It enables the development of a wide range of high performance analog ICs capable of 33 V operation in a footprint that no other generation

Rev. C

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FUNCTIONAL BLOCK DIAGRAMS

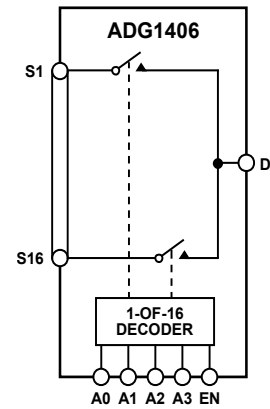


Figure 1.

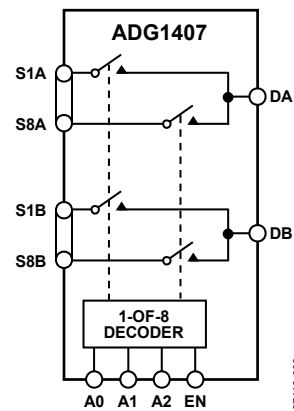


Figure 2.

of high voltage devices has been able to achieve. Unlike analog ICs using conventional CMOS processes, iCMOS components can tolerate high supply voltages while providing increased performance, dramatically lower power consumption, and reduced package size.

The ultralow on resistance and on-resistance flatness of these switches make them ideal solutions for data acquisition and gain switching applications where low distortion is critical. iCMOS construction ensures ultralow power dissipation, making the devices ideally suited for portable and battery-powered instruments.

Table 1. Related Devices

Device No.	Description
ADG1206/ADG1207	Low capacitance, low charge injection, and low leakage 8-/16-channel ±15 V multiplexers

TABLE OF CONTENTS

Features	1	Absolute Maximum Ratings	8
Applications.....	1	Thermal Resistance.....	8
General Description.....	1	ESD Caution.....	8
Functional Block Diagrams.....	1	Pin Configurations and Function Descriptions.....	9
Revision History	2	Typical Performance Characteristics	13
Specifications.....	3	Terminology	17
±15 V Dual Supply	3	Test Circuits.....	18
12 V Single Supply.....	4	Outline Dimensions	20
±5 V Dual Supply	6	Ordering Guide	20
Continuous Current per Channel.....	7		

REVISION HISTORY

6/2016—Rev. B to Rev. C

Changes to Analog Inputs Parameter, Table 7	8
Added Digital Inputs Parameter, Table 7	8

4/2016—Rev. A to Rev. B

Changed CP-32-2 to CP-32-7	Throughout
Changed LFCSP_VQ to LFCSP	Throughout
Changes to Figure 4 and Table 9.....	9
Changes to Figure 6 and Table 10.....	11
Updated Outline Dimensions	20
Changes to Ordering Guide	20

3/2009—Rev. 0 to Rev. A

Change to I _{DD} Parameter, Table 2	4
Change to I _{DD} Parameter, Table 3	5
Changes to Figure 16.....	14

8/2008—Revision 0: Initial Version

SPECIFICATIONS

±15 V DUAL SUPPLY

$V_{DD} = +15\text{ V} \pm 10\%$, $V_{SS} = -15\text{ V} \pm 10\%$, $GND = 0\text{ V}$, unless otherwise noted.¹

Table 2.

Parameter	+25°C	-40°C to +85°C	-40°C to +125°C ¹	Unit	Test Conditions/Comments
ANALOG SWITCH					
Analog Signal Range			V_{SS} to V_{DD}	V	
On Resistance (R_{ON})	9.5 11.5	14	16	Ω typ Ω max	$V_{DD} = +13.5\text{ V}$, $V_{SS} = -13.5\text{ V}$, $V_S = \pm 10\text{ V}$, $I_S = -10\text{ mA}$; see Figure 27
On-Resistance Match Between Channels (ΔR_{ON})	0.55			Ω typ	$V_{DD} = +13.5\text{ V}$, $V_{SS} = -13.5\text{ V}$, $V_S = \pm 10\text{ V}$, $I_S = -10\text{ mA}$
On-Resistance Flatness ($R_{FLAT(ON)}$)	1 1.6	1.5	1.7	Ω max Ω typ	$V_{DD} = +13.5\text{ V}$, $V_{SS} = -13.5\text{ V}$, $V_S = \pm 10\text{ V}$, $I_S = -10\text{ mA}$
	1.9	2.15	2.3	Ω max	
LEAKAGE CURRENTS					
Source Off Leakage, I_S (Off)	± 0.01			nA typ	$V_{DD} = +16.5\text{ V}$, $V_{SS} = -16.5\text{ V}$ $V_S = \pm 10\text{ V}$, $V_D = \mp 10\text{ V}$; see Figure 28
Drain Off Leakage, I_D (Off)	± 0.25 ± 0.01	± 1	± 4	nA max nA typ	$V_S = \pm 10\text{ V}$, $V_D = \mp 10\text{ V}$; see Figure 28
Channel On Leakage, I_D , I_S (On)	± 0.5 ± 0.05 ± 0.5	± 3	± 20	nA max nA typ nA max	$V_S = V_D = \pm 10\text{ V}$; see Figure 29
DIGITAL INPUTS					
Input High Voltage, V_{INH}			2.0	V min	
Input Low Voltage, V_{INL}			0.8	V max	
Input Current	± 0.002			μA typ μA max	$V_{IN} = V_{GND}$ or V_{DD}
Digital Input Capacitance, C_{IN}	3		± 0.1	μF typ	
DYNAMIC CHARACTERISTICS ²					
Transition Time, $t_{TRANSITION}$	105 160	200	225	ns typ ns max	$R_L = 100\ \Omega$, $C_L = 35\text{ pF}$ $V_S = 10\text{ V}$, see Figure 30
Break-Before-Make Time Delay, t_{BBM}	40		10	ns typ ns min	$R_L = 100\ \Omega$, $C_L = 35\text{ pF}$ $V_{S1} = V_{S2} = 10\text{ V}$; see Figure 31
t_{ON} (EN)	83 110	140	155	ns typ ns max	$R_L = 100\ \Omega$, $C_L = 35\text{ pF}$ $V_S = 10\text{ V}$; see Figure 32
t_{OFF} (EN)	98 120	145	165	ns typ ns max	$R_L = 100\ \Omega$, $C_L = 35\text{ pF}$ $V_S = 10\text{ V}$; see Figure 32
Charge Injection	10			pC typ	$V_S = 0\text{ V}$, $R_S = 0\ \Omega$, $C_L = 1\text{ nF}$; see Figure 33
Off Isolation	-73			dB typ	$R_L = 50\ \Omega$, $C_L = 5\text{ pF}$, $f = 1\text{ MHz}$; see Figure 34
Channel-to-Channel Crosstalk	-70			dB typ	$R_L = 50\ \Omega$, $C_L = 5\text{ pF}$, $f = 1\text{ MHz}$; see Figure 35
Total Harmonic Distortion Plus Noise (THD + N)	0.07			% typ	$R_L = 110\ \Omega$, 15 V p-p , $f = 20\text{ Hz to } 20\text{ kHz}$; see Figure 37
-3 dB Bandwidth					$R_L = 50\ \Omega$, $C_L = 5\text{ pF}$; see Figure 36
ADG1406	60			MHz typ	
ADG1407	110			MHz typ	
Insertion Loss	0.6			dB typ	$R_L = 50\ \Omega$, $C_L = 5\text{ pF}$, $f = 1\text{ MHz}$; see Figure 36
C_S (Off)	8			pF typ	$f = 1\text{ MHz}$
C_D (Off)					$f = 1\text{ MHz}$
ADG1406	90			pF typ	
ADG1407	45			pF typ	

Parameter	+25°C	−40°C to +85°C	−40°C to +125°C ¹	Unit	Test Conditions/Comments
C _D , C _S (On) ADG1406 ADG1407	115 70			pF typ pF typ	f = 1 MHz
POWER REQUIREMENTS					
I _{DD}	0.002		1	μA typ μA max	V _{DD} = +16.5 V, V _{SS} = −16.5 V Digital inputs = 0 V or V _{DD}
I _{DD}	280		475	μA typ μA max	Digital inputs = 5 V
I _{SS}	0.002		1	μA typ μA max	Digital inputs = 0 V, 5 V or V _{DD}
V _{DD} /V _{SS}			±4.5/±16.5	V min/max	

¹ Temperature range for B version is −40°C to +125°C.

² Guaranteed by design, not subject to production test.

12 V SINGLE SUPPLY

V_{DD} = 12 V ± 10%, V_{SS} = 0 V, GND = 0 V, unless otherwise noted.

Table 3.

Parameter	+25°C	−40°C to +85°C	−40°C to +125°C ¹	Unit	Test Conditions/Comments
ANALOG SWITCH					
Analog Signal Range			0 to V _{DD}	V	
On Resistance (R _{ON})	18			Ω typ	V _{DD} = 10.8 V, V _{SS} = 0 V; V _S = 0 V to 10 V, I _S = −10 mA; see Figure 27
	21.5	26	28.5	Ω max	
On-Resistance Match Between Channels (ΔR _{ON})	0.55			Ω typ	V _{DD} = 10.8 V, V _{SS} = 0 V; V _S = 0 V to 10 V, I _S = −10 mA
	1.2	1.6	1.8	Ω max	
On-Resistance Flatness (R _{FLAT(ON)})	5			Ω typ	V _{DD} = 10.8 V, V _{SS} = 0 V; V _S = 0 V to 10 V, I _S = −10 mA
	6	6.9	7.3	Ω max	
LEAKAGE CURRENTS					
Source Off Leakage, I _S (Off)	±0.01			nA typ	V _{DD} = 10.8 V V _S = 1 V/10 V, V _D = 10 V/1 V; see Figure 28
	±0.25	±1	±4	nA max	
Drain Off Leakage, I _D (Off)	±0.01			nA typ	V _S = 1 V/10 V, V _D = 10 V/1 V; see Figure 28
	±0.5	±3	±20	nA max	
Channel On Leakage, I _D , I _S (On)	±0.01			nA typ	V _S = V _D = 1 V or 10 V; see Figure 29
	±0.5	±3	±20	nA max	
DIGITAL INPUTS					
Input High Voltage, V _{INH}			2.0	V min	
Input Low Voltage, V _{INL}			0.8	V max	
Input Current	±0.002			μA typ	V _{IN} = V _{GND} or V _{DD}
			±0.1	μA max	
Digital Input Capacitance, C _{IN}	4			pF typ	
DYNAMIC CHARACTERISTICS²					
Transition Time, t _{TRANSITION}	170			ns typ	R _L = 100 Ω, C _L = 35 pF
	250	310	350	ns max	V _S = 8 V; see Figure 29
Break-Before-Make Time Delay, t _{BBM}	75			ns typ	R _L = 100 Ω, C _L = 35 pF
			30	ns min	V _{S1} = V _{S2} = 8 V; see Figure 31

Parameter	+25°C	–40°C to +85°C	–40°C to +125°C ¹	Unit	Test Conditions/Comments
t _{ON} (EN)	145 205	250	285	ns typ ns max	R _L = 100 Ω, C _L = 35 pF V _S = 8 V; see Figure 31
t _{OFF} (EN)	112 150	175	200	ns typ ns max	R _L = 100 Ω, C _L = 35 pF V _S = 8 V; see Figure 31
Charge Injection	10			pC typ	V _S = 6 V, R _S = 0 Ω, C _L = 1 nF; see Figure 33
Off Isolation	–73			dB typ	R _L = 50 Ω, C _L = 5 pF, f = 1 MHz; see Figure 34
Channel-to-Channel Crosstalk	–70			dB typ	R _L = 50 Ω, C _L = 5 pF, f = 1 MHz; see Figure 35
–3 dB Bandwidth					R _L = 50 Ω, C _L = 5 pF; see Figure 36
ADG1406	35			MHz typ	
ADG1407	70			MHz typ	
Insertion Loss	0.6			dB typ	R _L = 50 Ω, C _L = 5 pF, f = 1 MHz; see Figure 36
C _S (Off)	12			pF typ	f = 1 MHz
C _D (Off)					f = 1 MHz
ADG1406	145			pF typ	
ADG1407	72			pF typ	
C _D , C _S (On)					f = 1 MHz
ADG1406	166			pF typ	
ADG1407	93			pF typ	
POWER REQUIREMENTS					
I _{DD}	0.002		1	μA typ μA max	V _{DD} = 13.2 V Digital inputs = 0 V or V _{DD}
I _{DD}	150		475	μA typ μA max	Digital inputs = 5 V
V _{DD}			5/16.5	V min/max	V _{SS} = 0 V, GND = 0 V

¹ Temperature range for B version: –40°C to +125°C.

² Guaranteed by design, not subject to production test.

±5 V DUAL SUPPLY

$V_{DD} = +5\text{ V} \pm 10\%$, $V_{SS} = -5\text{ V} \pm 10\%$, $GND = 0\text{ V}$, unless otherwise noted.

Table 4.

Parameter	+25°C	-40°C to +85°C	-40°C to +125°C ¹	Unit	Test Conditions/Comments
ANALOG SWITCH					
Analog Signal Range			V_{SS} to V_{DD}	V	
On Resistance (R_{ON})	21			Ω typ	$V_{DD} = +4.5\text{ V}$, $V_{SS} = -4.5\text{ V}$, $V_S = \pm 4.5\text{ V}$, $I_S = -10\text{ mA}$; see Figure 27
On-Resistance Match Between Channels (ΔR_{ON})	0.6	29	32	Ω max	
	1.3	1.7	1.9	Ω typ	$V_{DD} = +4.5\text{ V}$, $V_{SS} = -4.5\text{ V}$, $V_S = \pm 4.5\text{ V}$, $I_S = -10\text{ mA}$
On-Resistance Flatness ($R_{FLAT(ON)}$)	5.2			Ω max	$V_{DD} = +4.5\text{ V}$, $V_{SS} = -4.5\text{ V}$, $V_S = \pm 4.5\text{ V}$, $I_S = -10\text{ mA}$
	6.4	7.3	7.6	Ω typ	
LEAKAGE CURRENTS					
Source Off Leakage, I_S (Off)	± 0.01			nA typ	$V_{DD} = +5.5\text{ V}$, $V_{SS} = -5.5\text{ V}$
	± 0.25	± 1	± 4	nA max	$V_S = \pm 4.5\text{ V}$, $V_D = \mp 4.5\text{ V}$; see Figure 28
Drain Off Leakage, I_D (Off)	± 0.01			nA typ	
	± 0.5	± 3	± 20	nA max	$V_S = \pm 4.5\text{ V}$, $V_D = \mp 4.5\text{ V}$; see Figure 28
Channel On Leakage, I_D , I_S (On)	± 0.01	± 3	± 20	nA typ	$V_S = V_D = \pm 4.5\text{ V}$; see Figure 29
	± 0.5	± 3	± 20	nA max	
DIGITAL INPUTS					
Input High Voltage, V_{INH}			2.0	V min	
Input Low Voltage, V_{INL}			0.8	V max	
Input Current	± 0.002			μA typ	$V_{IN} = V_{GND}$ or V_{DD}
			± 0.1	μA max	
Digital Input Capacitance, C_{IN}	3.5			pF typ	
DYNAMIC CHARACTERISTICS²					
Transition Time, $t_{TRANSITION}$	260			ns typ	$R_L = 100\ \Omega$, $C_L = 35\text{ pF}$
	435	510	565	ns max	$V_S = 5\text{ V}$; see Figure 30
Break-Before-Make Time Delay, t_{BBM}	90			ns typ	$R_L = 100\ \Omega$, $C_L = 35\text{ pF}$
			30	ns min	$V_{S1} = V_{S2} = 5\text{ V}$; see Figure 31
t_{ON} (EN)	230			ns typ	$R_L = 100\ \Omega$, $C_L = 35\text{ pF}$
	335	400	445	ns max	$V_S = 5\text{ V}$; see Figure 32
t_{OFF} (EN)	205			ns typ	$R_L = 100\ \Omega$, $C_L = 35\text{ pF}$
	290	340	370	ns max	$V_S = 5\text{ V}$; see Figure 32
Charge Injection	10			pC typ	$V_S = 0\text{ V}$, $R_S = 0\ \Omega$, $C_L = 1\text{ nF}$; see Figure 33
Off Isolation	-73			dB typ	$R_L = 50\ \Omega$, $C_L = 5\text{ pF}$, $f = 1\text{ MHz}$; see Figure 34
Channel-to-Channel Crosstalk	-70			dB typ	$R_L = 50\ \Omega$, $C_L = 5\text{ pF}$, $f = 1\text{ MHz}$; see Figure 35
Total Harmonic Distortion, THD + N	0.18			% typ	$R_L = 110\ \Omega$, 5 V p-p , $f = 20\text{ Hz to } 20\text{ kHz}$; see Figure 37
-3 dB Bandwidth					$R_L = 50\ \Omega$, $C_L = 5\text{ pF}$; see Figure 36
ADG1406	40			MHz typ	
ADG1407	80			MHz typ	
Insertion Loss	1.15			dB typ	$R_L = 50\ \Omega$, $C_L = 5\text{ pF}$, $f = 1\text{ MHz}$; see Figure 36
C_S (Off)	10			pF typ	$f = 1\text{ MHz}$
C_D (Off)					$f = 1\text{ MHz}$
ADG1406	123			pF typ	
ADG1407	62			pF typ	
C_D , C_S (On)					$f = 1\text{ MHz}$
ADG1406	148			pF typ	
ADG1407	88			pF typ	

Parameter	+25°C	-40°C to +85°C	-40°C to +125°C ¹	Unit	Test Conditions/Comments
POWER REQUIREMENTS					
I_{DD}	0.002		1	$\mu\text{A typ}$ $\mu\text{A max}$	$V_{DD} = +5.5\text{ V}, V_{SS} = -5.5\text{ V}$ Digital inputs = 0 V or V_{DD}
I_{SS}	0.002		1	$\mu\text{A typ}$ $\mu\text{A max}$	Digital inputs = 0 V, 5 V, or V_{DD}
V_{DD}/V_{SS}			$\pm 4.5/\pm 16.5$	V min/max	

¹ Temperature range for B version: -40°C to +125°C.

² Guaranteed by design, not subject to production test.

CONTINUOUS CURRENT PER CHANNEL

Table 5. Continuous Current per Channel (ADG1406)

Parameter	25°C	85°C	125°C	Unit	Test Conditions/Comments
CONTINUOUS CURRENT PER CHANNEL¹					
15 V Dual Supply					$V_{DD} = +13.5\text{ V}, V_{SS} = -13.5\text{ V}$
28-Lead TSSOP	180	100	50	mA max	
32-Lead LFCSP	300	150	60	mA max	
12 V Single Supply					$V_{DD} = 10.8\text{ V}, V_{SS} = 0\text{ V}$
28-Lead TSSOP	150	90	50	mA max	
32-Lead LFCSP	260	130	55	mA max	
5 V Dual Supply					$V_{DD} = +4.5\text{ V}, V_{SS} = -4.5\text{ V}$
28-Lead TSSOP	140	85	45	mA max	
32-Lead LFCSP	245	130	55	mA max	

¹ Guaranteed by design, not subject to production test.

Table 6. Continuous Current per Channel (ADG1407)

Parameter	25°C	85°C	125°C	Unit	Test Conditions/Comments
CONTINUOUS CURRENT PER CHANNEL¹					
15 V Dual Supply					$V_{DD} = +13.5\text{ V}, V_{SS} = -13.5\text{ V}$
28-Lead TSSOP	135	85	45	mA max	
32-Lead LFCSP	235	125	55	mA max	
12 V Single Supply					$V_{DD} = 10.8\text{ V}, V_{SS} = 0\text{ V}$
28-Lead TSSOP	110	70	40	mA max	
32-Lead LFCSP	190	110	50	mA max	
5 V Dual Supply					$V_{DD} = +4.5\text{ V}, V_{SS} = -4.5\text{ V}$
28-Lead TSSOP	105	65	40	mA max	
32-Lead LFCSP	180	100	50	mA max	

¹ Guaranteed by design, not subject to production test.

ABSOLUTE MAXIMUM RATINGS

$T_A = 25^\circ\text{C}$, unless otherwise noted.

Table 7.

Parameter	Rating
V_{DD} to V_{SS}	35 V
V_{DD} to GND	-0.3 V to +25 V
V_{SS} to GND	+0.3 V to -25 V
Analog Inputs ¹	$V_{SS} - 0.3\text{ V}$ to $V_{DD} + 0.3\text{ V}$ or 30 mA, whichever occurs first
Digital Inputs ¹	GND - 0.3 V to $V_{DD} + 0.3\text{ V}$ or 30 mA, whichever occurs first
Continuous Current, Sx or Dx Pins	Table 5 and Table 6 specifications + 15%
Peak Current, Sx or Dx Pins (Pulsed at 1 ms, 10% Duty Cycle Maximum)	
28-Lead TSSOP	300 mA
32-Lead LFCSP	550 mA
Operating Temperature Range	
Industrial (B Version)	-40°C to +125°C
Storage Temperature Range	-65°C to +150°C
Junction Temperature	150°C
Reflow Soldering, Pb-Free	
Peak Temperature	260 (+0/-5)°C
Time at Peak Temperature	10 sec to 40 sec

¹ Overvoltages at the Ax, EN, Sx, or Dx pins are clamped by internal diodes. Limit current to the maximum ratings given.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

Only one absolute maximum rating may be applied at any one time.

THERMAL RESISTANCE

θ_{JA} is specified for the worst-case conditions, that is, a device soldered in a circuit board for surface-mount packages.

Table 8. Thermal Resistance

Package Type	θ_{JA}	θ_{JC}	Unit
28-Lead TSSOP	97.9	14	°C/W
32-Lead LFCSP	27.27		°C/W

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

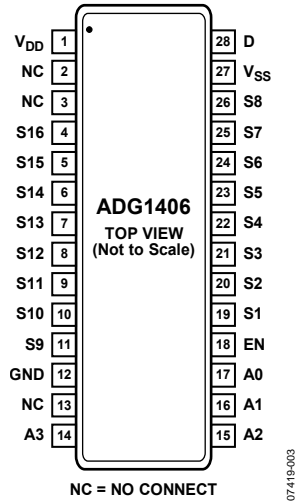


Figure 3. ADG1406 TSSOP Pin Configuration

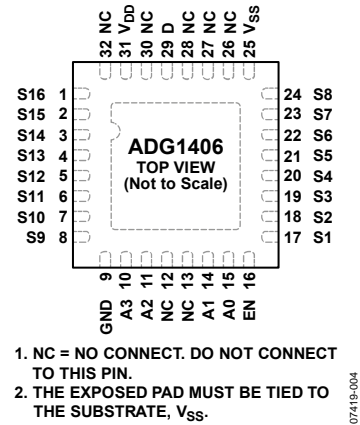


Figure 4. ADG1406 LFCSP Pin Configuration

Table 9. ADG1406 Pin Function Descriptions

Pin No.		Mnemonic	Description
TSSOP	LFCSP		
1	31	V _{DD}	Most Positive Power Supply Potential.
2, 3, 13	12, 13, 26, 27, 28, 30, 32	NC	No Connect.
4	1	S16	Source Terminal 16. This pin can be an input or an output.
5	2	S15	Source Terminal 15. This pin can be an input or an output.
6	3	S14	Source Terminal 14. This pin can be an input or an output.
7	4	S13	Source Terminal 13. This pin can be an input or an output.
8	5	S12	Source Terminal 12. This pin can be an input or an output.
9	6	S11	Source Terminal 11. This pin can be an input or an output.
10	7	S10	Source Terminal 10. This pin can be an input or an output.
11	8	S9	Source Terminal 9. This pin can be an input or an output.
12	9	GND	Ground (0 V) Reference.
14	10	A3	Logic Control Input.
15	11	A2	Logic Control Input.
16	14	A1	Logic Control Input.
17	15	A0	Logic Control Input.
18	16	EN	Active High Digital Input. When this pin is low, the device is disabled and all switches are turned off. When this pin is high, the Ax logic inputs determine which switch is turned on.
19	17	S1	Source Terminal 1. This pin can be an input or an output.
20	18	S2	Source Terminal 2. This pin can be an input or an output.
21	19	S3	Source Terminal 3. This pin can be an input or an output.
22	20	S4	Source Terminal 4. This pin can be an input or an output.
23	21	S5	Source Terminal 5. This pin can be an input or an output.
24	22	S6	Source Terminal 6. This pin can be an input or an output.
25	23	S7	Source Terminal 7. This pin can be an input or an output.
26	24	S8	Source Terminal 8. This pin can be an input or an output.
27	25	V _{SS}	Most Negative Power Supply Potential. In single-supply applications, this pin can be connected to ground.
28	29	D	Drain Terminal. This pin can be an input or an output.
Not applicable	0	EPAD	Exposed Pad. The exposed pad must be tied to the substrate, V _{SS} .

Table 10. **ADG1406** Truth Table

A3	A2	A1	A0	EN	On Switch
X	X	X	X	0	None
0	0	0	0	1	1
0	0	0	1	1	2
0	0	1	0	1	3
0	0	1	1	1	4
0	1	0	0	1	5
0	1	0	1	1	6
0	1	1	0	1	7
0	1	1	1	1	8
1	0	0	0	1	9
1	0	0	1	1	10
1	0	1	0	1	11
1	0	1	1	1	12
1	1	0	0	1	13
1	1	0	1	1	14
1	1	1	0	1	15
1	1	1	1	1	16

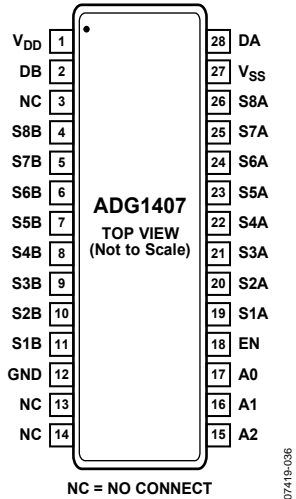


Figure 5. ADG1407 TSSOP Pin Configuration

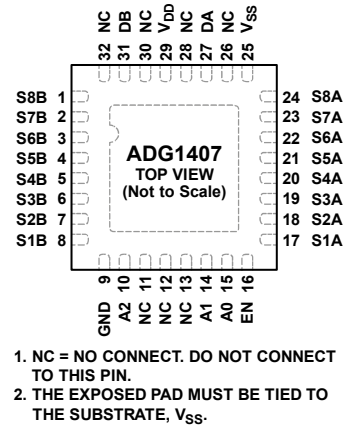


Figure 6. ADG1407 LFCSP Pin Configuration

Table 11. ADG1407 Pin Function Descriptions

Pin No.		Mnemonic	Description
TSSOP	LFCSP		
1	29	V _{DD}	Most Positive Power Supply Potential.
2	31	DB	Drain Terminal B. This pin can be an input or an output.
3, 13, 14	11, 12, 13, 26, 28, 30, 32	NC	No Connect.
4	1	S8B	Source Terminal 8B. This pin can be an input or an output.
5	2	S7B	Source Terminal 7B. This pin can be an input or an output.
6	3	S6B	Source Terminal 6B. This pin can be an input or an output.
7	4	S5B	Source Terminal 5B. This pin can be an input or an output.
8	5	S4B	Source Terminal 4B. This pin can be an input or an output.
9	6	S3B	Source Terminal 3B. This pin can be an input or an output.
10	7	S2B	Source Terminal 2B. This pin can be an input or an output.
11	8	S1B	Source Terminal 1B. This pin can be an input or an output.
12	9	GND	Ground (0 V) Reference.
15	10	A2	Logic Control Input.
16	14	A1	Logic Control Input.
17	15	A0	Logic Control Input.
18	16	EN	Active High Digital Input. When this pin is low, the device is disabled and all switches are turned off. When this pin is high, the Ax logic inputs determine which switch is turned on.
19	17	S1A	Source Terminal 1A. This pin can be an input or an output.
20	18	S2A	Source Terminal 2A. This pin can be an input or an output.
21	19	S3A	Source Terminal 3A. This pin can be an input or an output.
22	20	S4A	Source Terminal 4A. This pin can be an input or an output.
23	21	S5A	Source Terminal 5A. This pin can be an input or an output.
24	22	S6A	Source Terminal 6A. This pin can be an input or an output.
25	23	S7A	Source Terminal 7A. This pin can be an input or an output.
26	24	S8A	Source Terminal 8A. This pin can be an input or an output.
27	25	V _{SS}	Most Negative Power Supply Potential. In single-supply applications, this pin can be connected to ground.
28	27	DA	Drain Terminal A. This pin can be an input or an output.
Not applicable	0	EPAD	Exposed Pad. The exposed pad must be tied to the substrate, V _{SS} .

Table 12. **ADG1407** Truth Table

A2	A1	A0	EN	On Switch Pair
X	X	X	0	None
0	0	0	1	1
0	0	1	1	2
0	1	0	1	3
0	1	1	1	4
1	0	0	1	5
1	0	1	1	6
1	1	0	1	7
1	1	1	1	8

TYPICAL PERFORMANCE CHARACTERISTICS

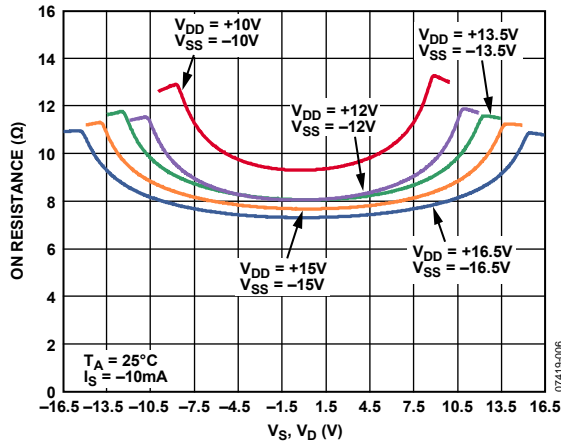


Figure 7. On Resistance as a Function of $V_D (V_S)$, Dual Supply

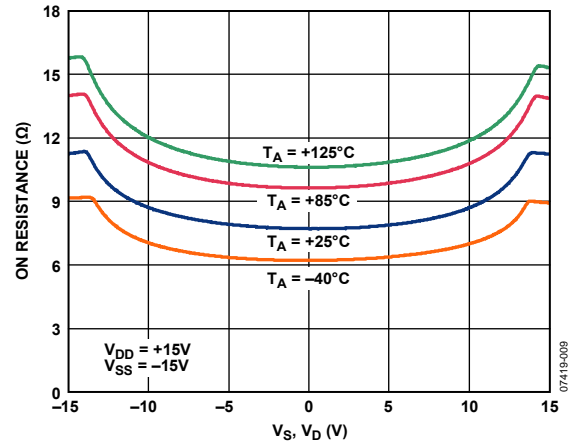


Figure 10. On Resistance as a Function of $V_D (V_S)$ for Different Temperatures, 15 V Dual Supply

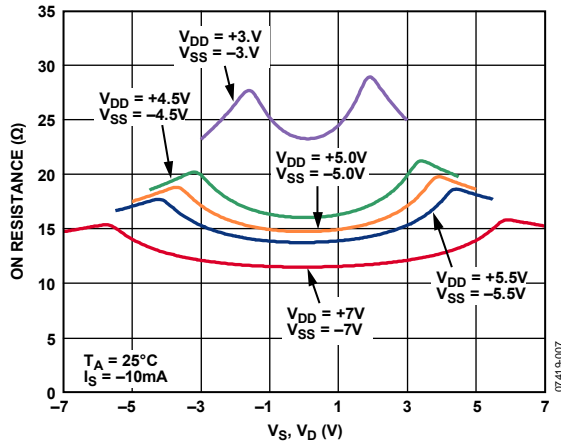


Figure 8. On Resistance as a Function of $V_D (V_S)$, Dual Supply

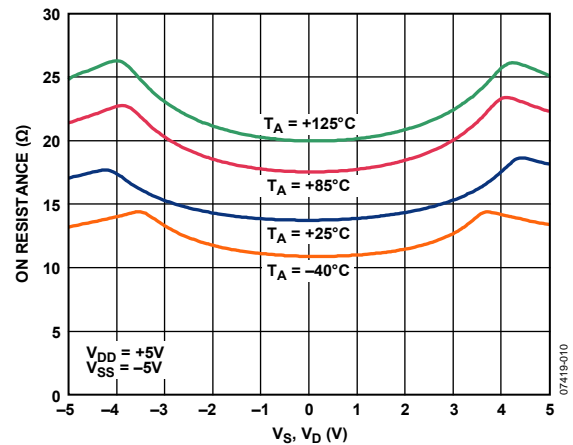


Figure 11. On Resistance as a Function of $V_D (V_S)$ for Different Temperatures, 5 V Dual Supply

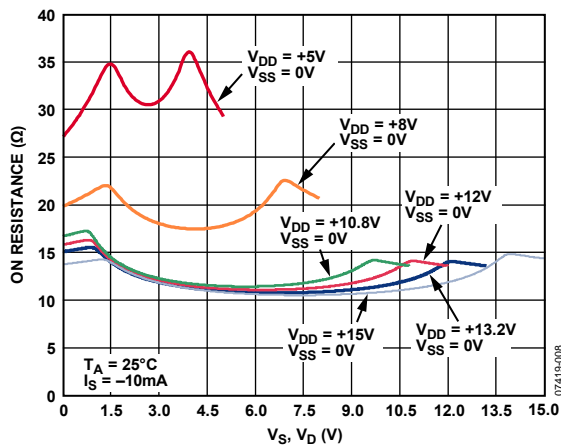


Figure 9. On Resistance as a Function of $V_D (V_S)$, Single Supply

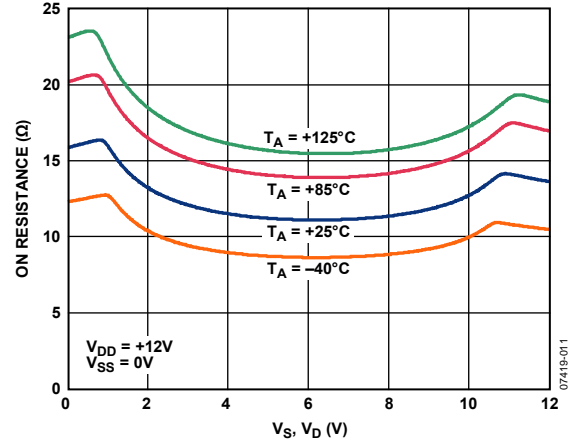


Figure 12. On Resistance as a Function of $V_D (V_S)$ for Different Temperatures, 12 V Single Supply

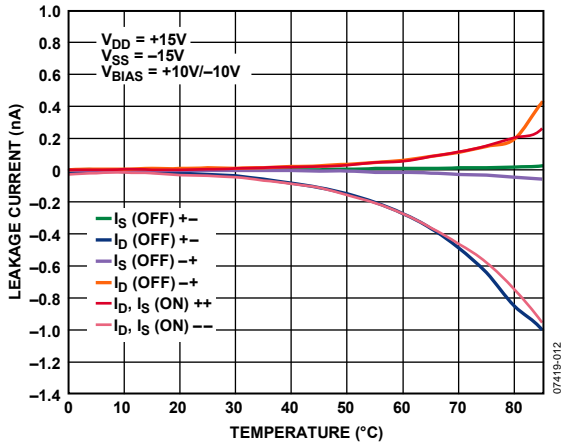


Figure 13. Leakage Current as a Function of Temperature (up to 85°C), 15 V Dual Supply

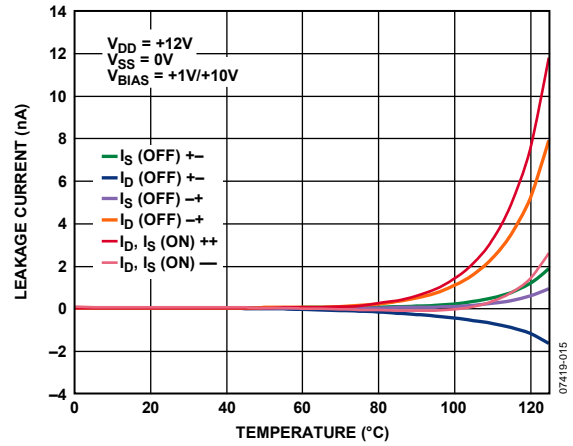


Figure 16. Leakage Current as a Function of Temperature, 12 V Single Supply

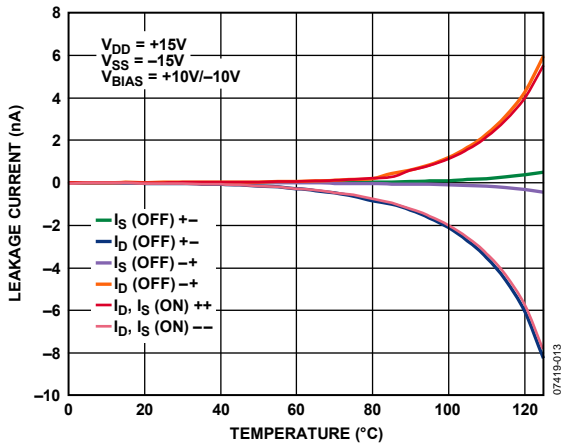


Figure 14. Leakage Current as a Function of Temperature, 15 V Dual Supply

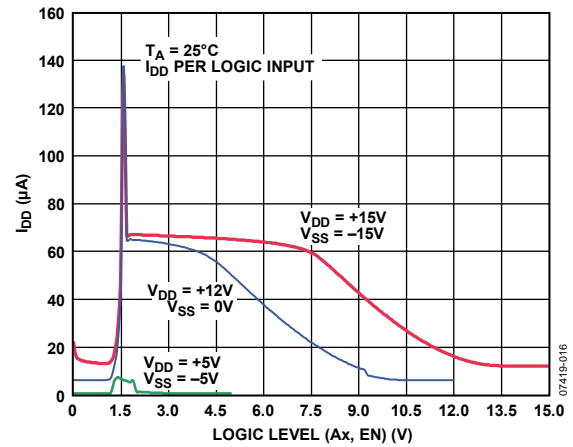


Figure 17. I_{DD} vs. Logic Level

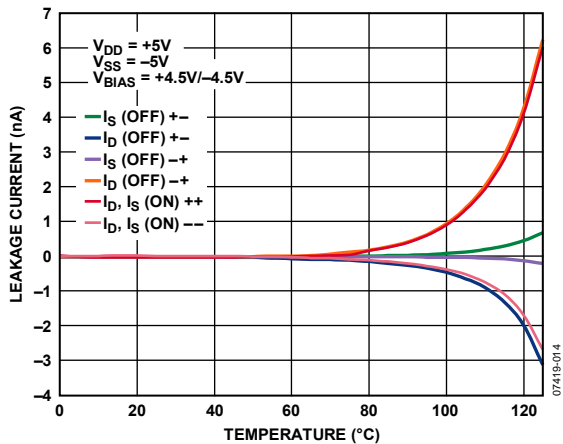


Figure 15. Leakage Current as a Function of Temperature, 5 V Dual Supply

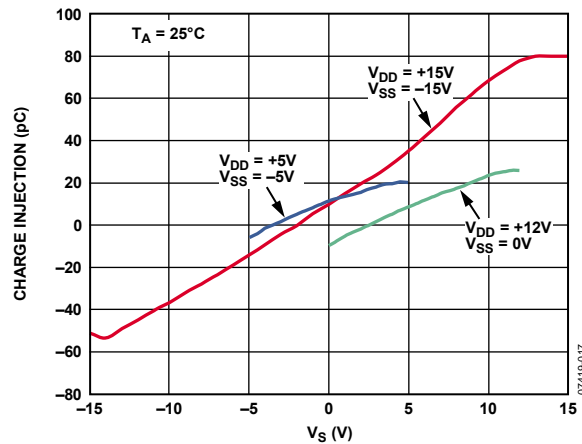


Figure 18. Charge Injection vs. Source Voltage

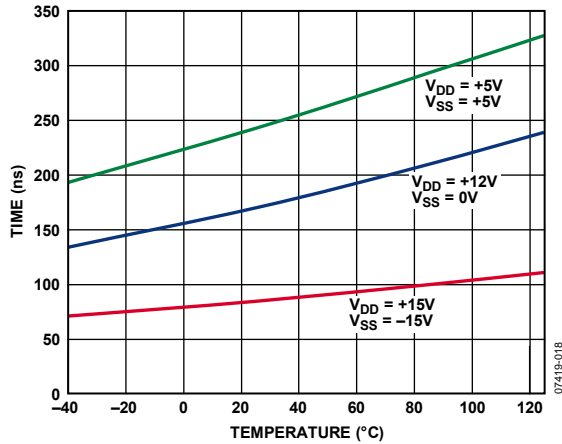


Figure 19. Transition Time vs. Temperature

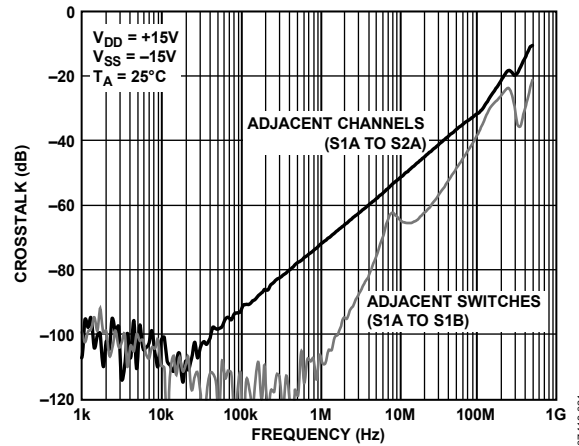


Figure 22. ADG1407 Crosstalk vs. Frequency

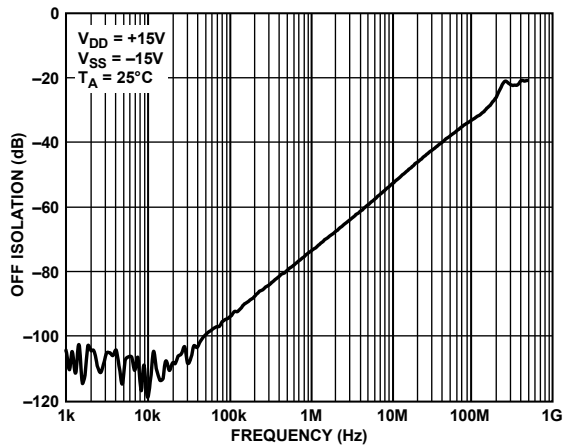


Figure 20. Off Isolation vs. Frequency

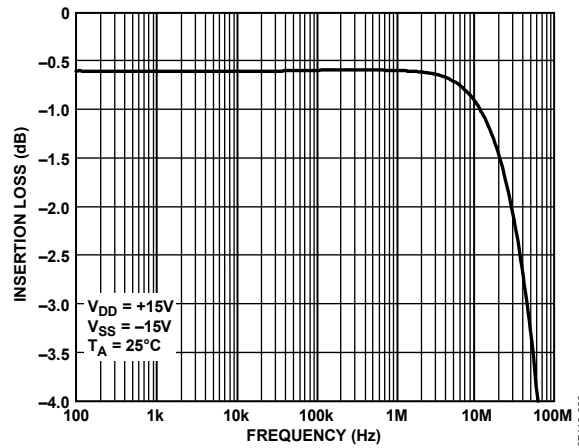


Figure 23. ADG1406 On Response vs. Frequency

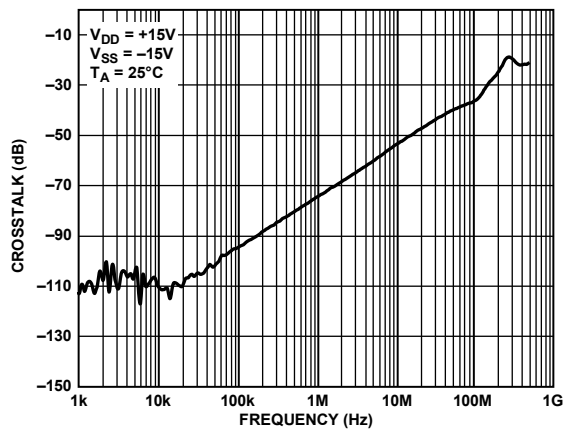


Figure 21. ADG1406 Crosstalk vs. Frequency

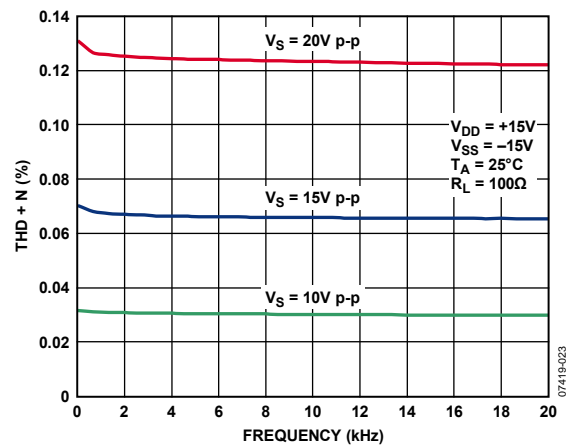


Figure 24. THD + N vs. Frequency, 15 V Dual Supply

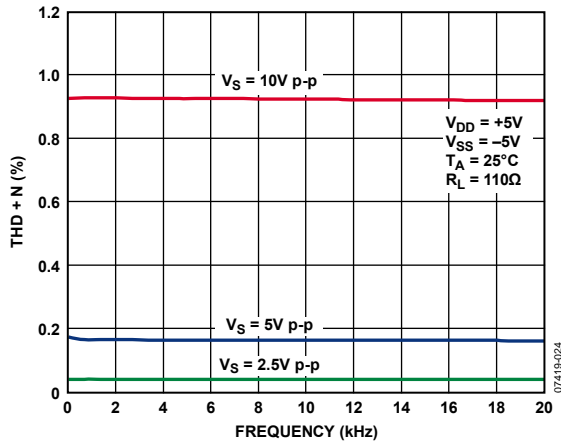


Figure 25. THD + N vs. Frequency, 5 V Dual Supply

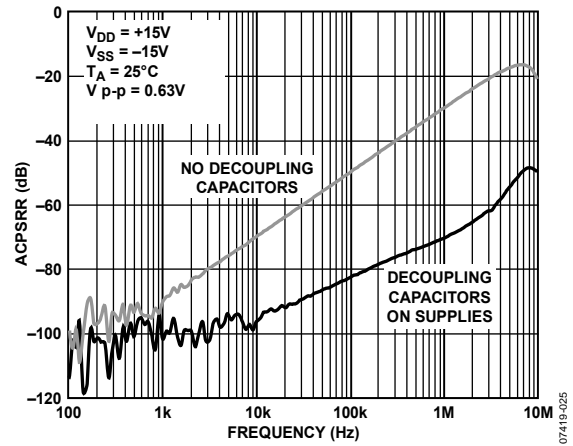


Figure 26. ACPSRR vs. Frequency

TERMINOLOGY

R_{ON}

Ohmic resistance between the D and S terminals.

ΔR_{ON}

Difference between the R_{ON} of any two channels.

$R_{FLAT(ON)}$

Flatness is defined as the difference between the maximum and minimum value of on resistance as measured.

I_S (Off)

Source leakage current when the switch is off.

I_D (Off)

Drain leakage current when the switch is off.

I_D, I_S (On)

Channel leakage current when the switch is on.

V_D, V_S

Analog voltage on Terminal D and Terminal S.

C_S (Off)

Channel input capacitance for the off condition.

C_D (Off)

Channel output capacitance for the off condition.

C_D, C_S (On)

On switch capacitance.

C_{IN}

Digital input capacitance.

t_{ON} (EN)

Delay time between the 50% and 90% points of the digital input and the switch on condition.

t_{OFF} (EN)

Delay time between the 50% and 90% points of the digital input and the switch off condition.

$t_{TRANSITION}$

Delay time between the 50% and 90% points of the digital inputs and the switch on condition when switching from one address state to another.

t_{BMM}

Off time measured between the 80% points of the switches when switching from one address state to another.

V_{INL}

Maximum input voltage for Logic 0.

V_{INH}

Minimum input voltage for Logic 1.

I_{INL}, I_{INH}

Input current of the digital input.

I_{DD}

Positive supply current.

I_{SS}

Negative supply current.

Off Isolation

A measure of unwanted signal coupling through an off channel.

Charge Injection

A measure of the glitch impulse transferred from the digital input to the analog output during switching.

Bandwidth

The frequency at which the output is attenuated by 3 dB.

On Response

The frequency response of the on switch.

Total Harmonic Distortion Plus Noise (THD + N)

The ratio of the harmonic amplitude plus noise of the signal to the fundamental.

AC Power Supply Rejection Ratio (ACPSRR)

Measures the ability of a device to avoid coupling noise and spurious signals that appear on the supply voltage pin to the output of the switch. The dc voltage on the device is modulated by a sine wave of 0.62 V p-p. The ratio of the amplitude of signal on the output to the amplitude of the modulation is the ACPSRR.

TEST CIRCUITS

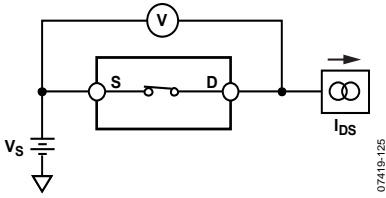


Figure 27. On Resistance

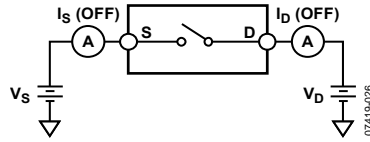


Figure 28. Off Leakage

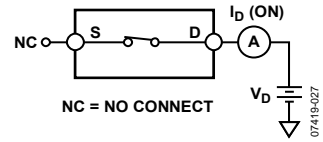


Figure 29. On Leakage

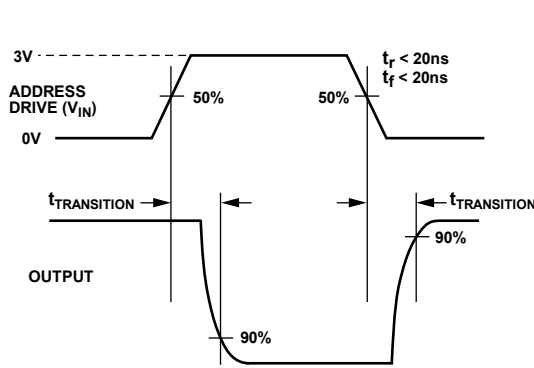
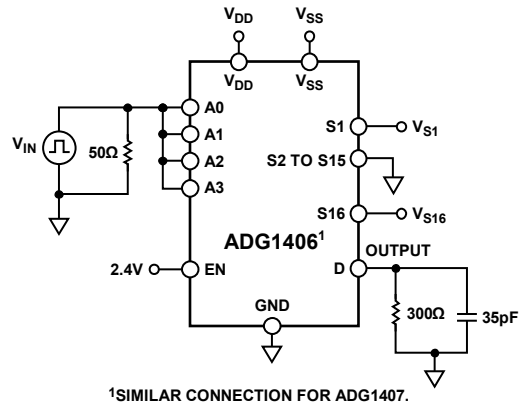


Figure 30. Address to Output Switching Times, $t_{\text{TRANSITION}}$



¹SIMILAR CONNECTION FOR ADG1407.

07419-028

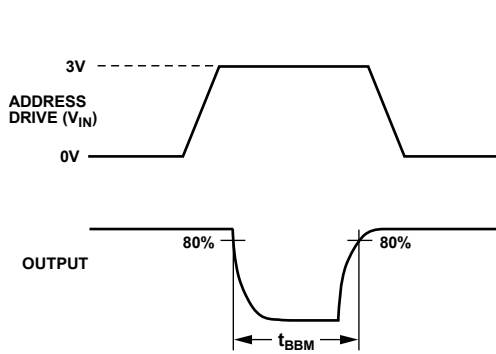
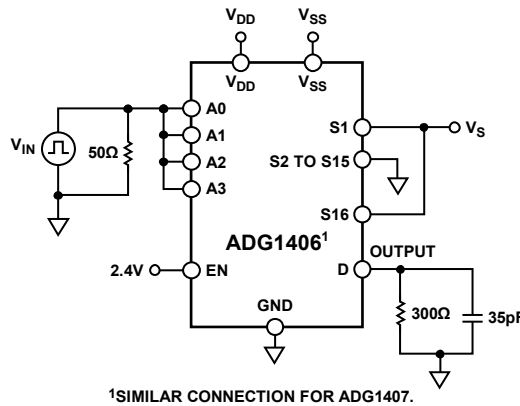


Figure 31. Break-Before-Make Delay, t_{BBM}



¹SIMILAR CONNECTION FOR ADG1407.

07419-029

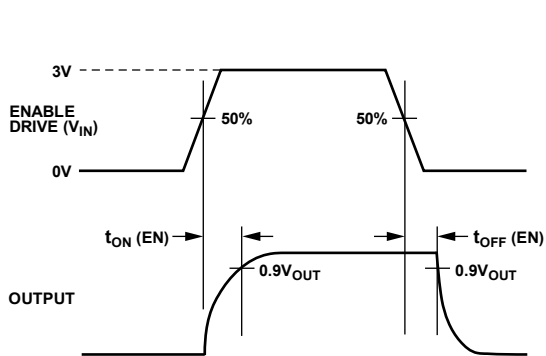
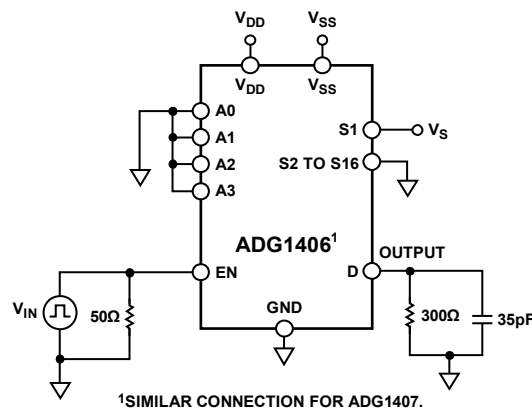
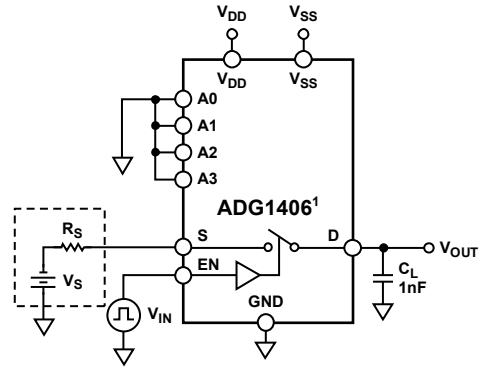
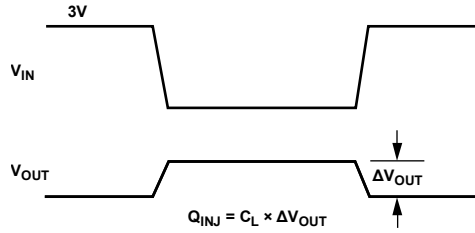


Figure 32. Enable Delay, $t_{\text{ON}}(\text{EN})$, $t_{\text{OFF}}(\text{EN})$



¹SIMILAR CONNECTION FOR ADG1407.

07419-030



¹SIMILAR CONNECTION FOR ADG1407.

07419-031

Figure 33. Charge Injection

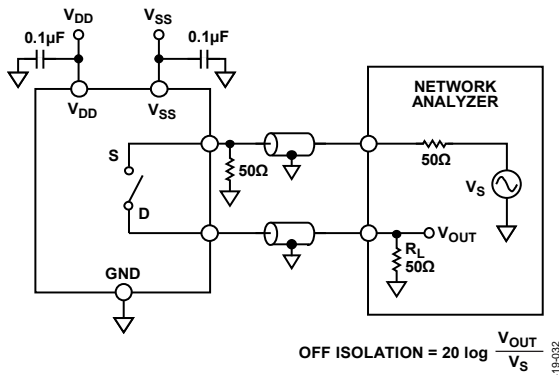


Figure 34. Off Isolation

07419-032

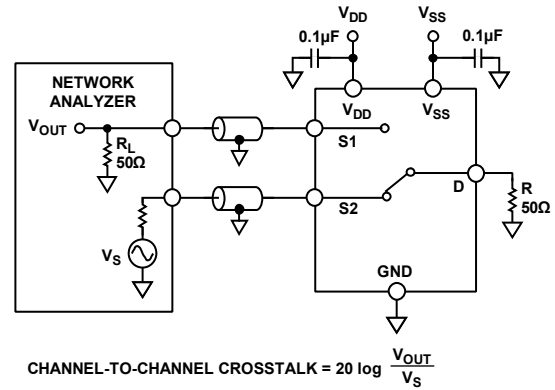


Figure 36. Channel-to-Channel Crosstalk

07419-034

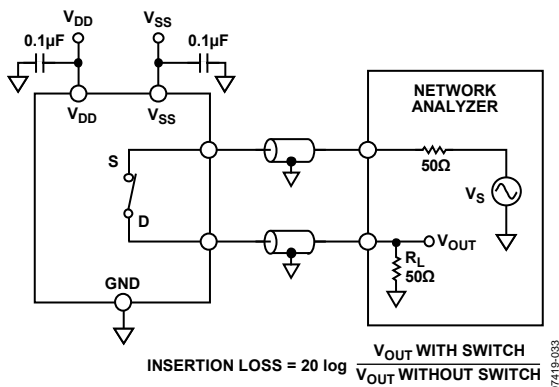


Figure 35. Bandwidth

07419-033

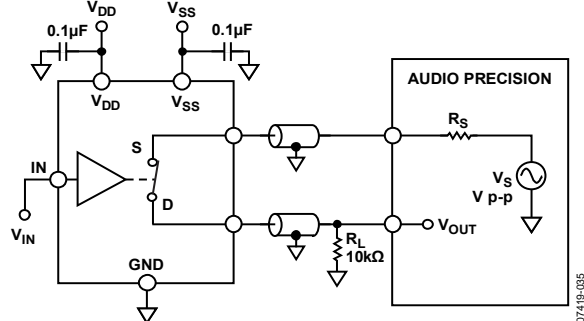
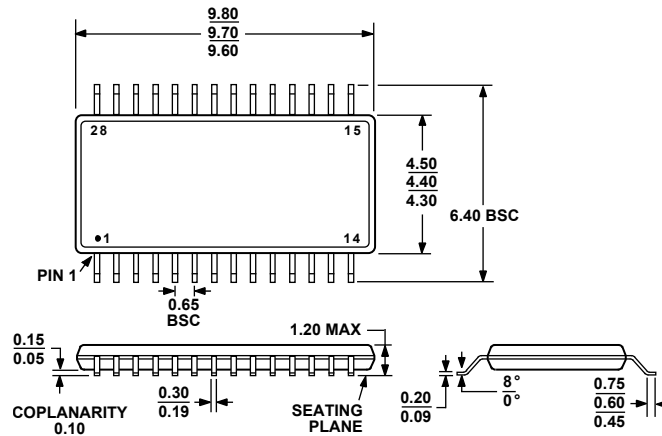


Figure 37. THD + N

07419-035

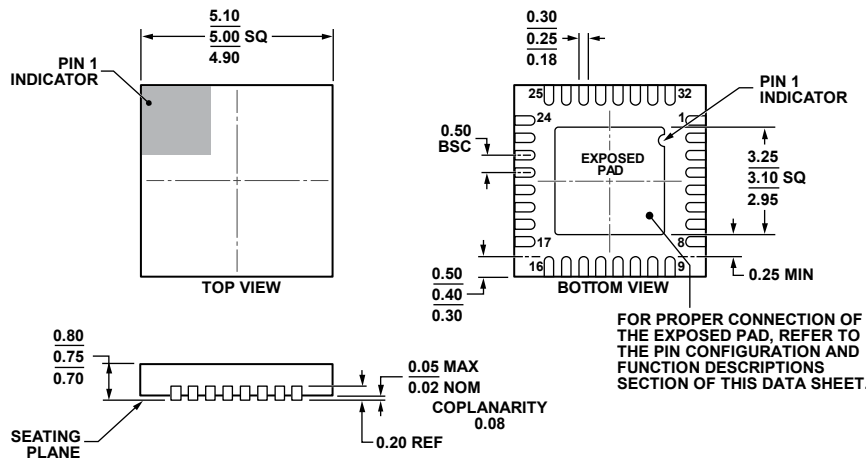
OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-153-AE

Figure 38. 28-Lead Thin Shrink Small Outline Package [TSSOP] (RU-28)

Dimensions shown in millimeters



COMPLIANT TO JEDEC STANDARDS MO-220-WHHD.

Figure 39. 32-Lead Lead Frame Chip Scale Package [LFCSP] 5 mm x 5 mm Body and 0.75 mm Package Height (CP-32-7)

Dimensions shown in millimeters

ORDERING GUIDE

Model ¹	Temperature Range	Description	Package Option
ADG1406BRUZ	-40°C to +125°C	28-Lead Thin Shrink Small Outline Package [TSSOP]	RU-28
ADG1406BRUZ-REEL7	-40°C to +125°C	28-Lead Thin Shrink Small Outline Package [TSSOP]	RU-28
ADG1406BCPZ-REEL7	-40°C to +125°C	32-Lead Lead Frame Chip Scale Package [LFCSP]	CP-32-7
ADG1407BRUZ	-40°C to +125°C	28-Lead Thin Shrink Small Outline Package [TSSOP]	RU-28
ADG1407BRUZ-REEL7	-40°C to +125°C	28-Lead Thin Shrink Small Outline Package [TSSOP]	RU-28
ADG1407BCPZ-REEL7	-40°C to +125°C	32-Lead Lead Frame Chip Scale Package [LFCSP]	CP-32-7

¹ Z = RoHS Compliant Part.