

## FEATURES

- **Tiny: 4 DACs in the Board Space of an SO-8**
- **Micropower: 59 $\mu$ A per DAC Plus 1 $\mu$ A Sleep Mode for Extended Battery Life**
- **Wide 2.7V to 5.5V Supply Range**
- **Rail-to-Rail Voltage Outputs Drive 1000pF**
- Reference Range Includes Supply for Ratiometric 0V-to- $V_{CC}$  Output
- **Reference Input Impedance is Code-Independent —Eliminates External Reference Buffer**
- Individually Addressable DACs
- Differential Nonlinearity:  $\leq \pm 0.75$ LSB Max
- Pin-Compatible Octal Version Available (LTC1660)

## APPLICATIONS

- Mobile Communications
- Remote Industrial Devices
- Automatic Calibration for Manufacturing
- Portable Battery-Powered Instruments
- Trim/Adjust Applications

## DESCRIPTION

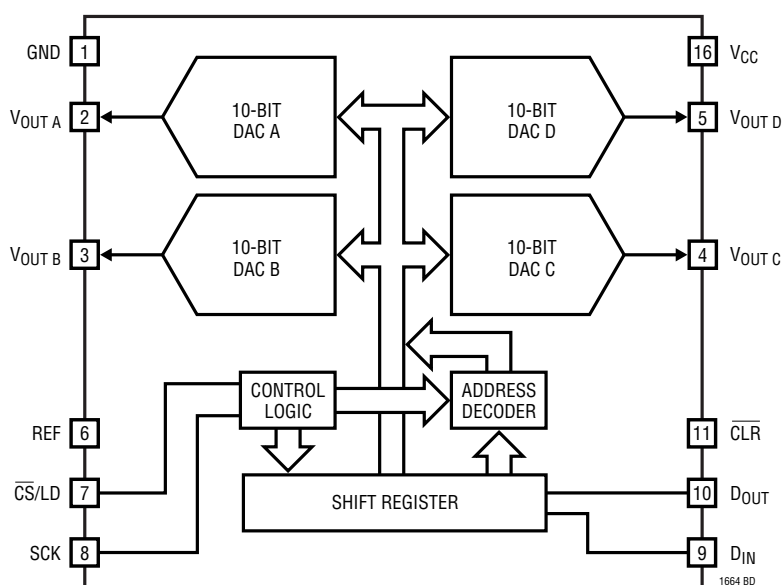
The LTC<sup>®</sup>1664 integrates four accurate, serially addressable 10-bit digital-to-analog converters (DACs) in a tiny 16-pin Narrow SSOP package. Each buffered DAC draws just 59 $\mu$ A total supply current, yet is capable of supplying DC output currents in excess of 5mA and reliably driving capacitive loads of up to 1000pF. Sleep mode further reduces total supply current to 1 $\mu$ A.

Linear Technology's proprietary, inherently monotonic voltage interpolation architecture provides excellent linearity while allowing for an exceptionally small external form factor.

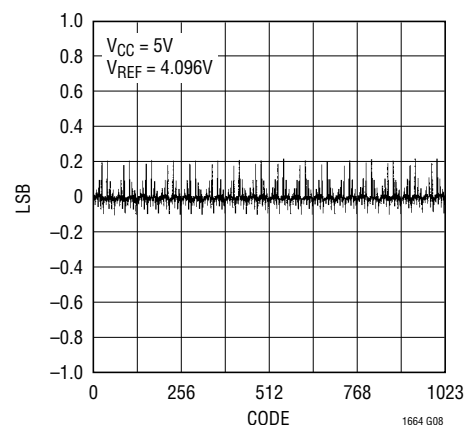
Ultralow supply current, power-saving Sleep mode and extremely compact size make the LTC1664 ideal for battery-powered applications, while its ease of use, high performance and wide supply range make it an excellent choice as a general-purpose converter.

 LTC and LT are registered trademarks of Linear Technology Corporation.

## BLOCK DIAGRAM



Differential Nonlinearity (DNL)



## ABSOLUTE MAXIMUM RATINGS

(Note 1)

$V_{CC}$ to GND	-0.3V to 7.5V
Logic Inputs to GND	-0.3V to 7.5V
$V_{OUT A}$ , $V_{OUT B}$ ... $V_{OUT D}$ , REF to GND	-0.3V to ( $V_{CC} + 0.3V$ )
Maximum Junction Temperature	125°C
Operating Temperature Range	
LTC1664C	0°C to 70°C
LTC1664I	-40°C to 85°C
Storage Temperature Range	-65°C to 150°C
Lead Temperature (Soldering, 10 sec)	300°C

## PACKAGE/ORDER INFORMATION

<p style="text-align: center;">TOP VIEW</p> <p>GN PACKAGE 16-LEAD PLASTIC SSOP</p> <p>N PACKAGE 16-LEAD PDIP</p> <p><math>T_{JMAX} = 125^{\circ}C</math>, <math>\theta_{JA} = 150^{\circ}C/W</math> (GN)  <math>T_{JMAX} = 125^{\circ}C</math>, <math>\theta_{JA} = 100^{\circ}C/W</math> (N)</p>	ORDER PART NUMBER
	<p>LTC1664CGN LTC1664CN LTC1664IGN LTC1664IN</p>
	GN PART MARKING
	<p>1664 1664I</p>

Consult factory for Military grade parts.

## ELECTRICAL CHARACTERISTICS

The ● denotes specifications which apply over the full operating temperature range, otherwise specifications are at  $T_A = 25^{\circ}C$ .  $V_{CC} = 2.7V$  to  $5.5V$ ,  $V_{REF} \leq V_{CC}$ ,  $V_{OUT}$  unloaded, unless otherwise noted.

SYMBOL	PARAMETER	CONDITONS	MIN	TYP	MAX	UNITS	
<b>Accuracy</b>							
	Resolution		●	10		Bits	
	Monotonicity	(Notes 2, 4)	●	10		Bits	
DNL	Differential Nonlinearity	(Notes 2, 4)	●		±0.2	±0.75	LSB
INL	Integral Nonlinearity	(Notes 2, 4)	●		±0.6	±2.5	LSB
$V_{OS}$	Offset Error	(Note 7)	●		±10	±30	mV
	$V_{OS}$ Temperature Coefficient		●		±15		$\mu V/^{\circ}C$
FSE	Full-Scale Error	$V_{CC} = 5V$ , $V_{REF} = 4.096V$ (Note 4)	●		±3	±15	LSB
	Full-Scale Error Temperature Coefficient		●		±30		$\mu V/^{\circ}C$
PSR	Power Supply Rejection	$V_{REF} = 2.5V$			0.18		LSB/V
<b>Reference Input</b>							
	Input Voltage Range		●	0		$V_{CC}$	V
	Resistance	Not in Sleep Mode	●	70	130		k $\Omega$
	Capacitance				12		pF
$I_{REF}$	Reference Current	Sleep Mode	●		0.001	1	$\mu A$
<b>Power Supply</b>							
$V_{CC}$	Positive Supply Voltage		●	2.7		5.5	V
$I_{CC}$	Supply Current	$V_{CC} = 5V$ (Note 3)	●		236	380	$\mu A$
		$V_{CC} = 3V$ (Note 3)	●		186	290	$\mu A$
		Sleep Mode (Note 3)	●		1	3	$\mu A$

## ELECTRICAL CHARACTERISTICS

The ● denotes specifications which apply over the full operating temperature range, otherwise specifications are at  $T_A = 25^\circ\text{C}$ .  $V_{CC} = 2.7\text{V}$  to  $5.5\text{V}$ ,  $V_{REF} \leq V_{CC}$ ,  $V_{OUT}$  unloaded, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS	
<b>DC Performance</b>							
	Short-Circuit Current Low	$V_{OUT} = 0\text{V}$ , $V_{CC} = 5.5\text{V}$ , $V_{REF} = 5.1\text{V}$ , Code = 1023 (Note 9)	●	10	30	100	mA
	Short-Circuit Current High	$V_{OUT} = V_{CC} = 5.5\text{V}$ , $V_{REF} = 5.1\text{V}$ , Code = 0 (Note 9)	●	10	27	120	mA
<b>AC Performance</b>							
	Voltage Output Slew Rate	Rising (Notes 4, 5) Falling (Notes 4, 5)			0.60 0.25		$\text{V}/\mu\text{s}$ $\text{V}/\mu\text{s}$
	Voltage Output Settling Time	Rising $0.1V_{FS}$ to $0.9V_{FS} \pm 0.5\text{LSB}$ (Notes 4, 5) Falling $0.9V_{FS}$ to $0.1V_{FS} \pm 0.5\text{LSB}$ (Notes 4, 5)			6 19		$\mu\text{s}$ $\mu\text{s}$
	Capacitive Load Driving				1000		pF
<b>Digital I/O</b>							
$V_{IH}$	Digital Input High Voltage	$V_{CC} = 2.7\text{V}$ to $5.5\text{V}$ $V_{CC} = 2.7\text{V}$ to $3.6\text{V}$	● ●	2.4 2.0			V V
$V_{IL}$	Digital Input Low Voltage	$V_{CC} = 4.5\text{V}$ to $5.5\text{V}$ $V_{CC} = 2.7\text{V}$ to $5.5\text{V}$	● ●			0.8 0.6	V V
$V_{OH}$	Digital Output High Voltage	$I_{OUT} = -1\text{mA}$ , $D_{OUT}$ Only	●	$V_{CC} - 1$			V
$V_{OL}$	Digital Output Low Voltage	$I_{OUT} = 1\text{mA}$ , $D_{OUT}$ Only	●			0.4	V
$I_{LK}$	Digital Input Leakage	$V_{IN} = \text{GND}$ to $V_{CC}$	●		0.05	$\pm 10$	$\mu\text{A}$
$C_{IN}$	Digital Input Capacitance				2		pF

## TIMING CHARACTERISTICS

The ● denotes specifications which apply over the full operating temperature range, otherwise specifications are at  $T_A = 25^\circ\text{C}$ . (See Figure 1)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS	
<b><math>V_{CC} = 4.5\text{V}</math> to <math>5.5\text{V}</math></b>							
$t_1$	$D_{IN}$ Valid to SCK Setup		●	40	15	ns	
$t_2$	$D_{IN}$ Valid to SCK Hold		●	0	-11	ns	
$t_3$	SCK High Time	(Note 6)	●	30	5	ns	
$t_4$	SCK Low Time	(Note 6)	●	30	7	ns	
$t_5$	$\overline{\text{CS}}/\text{LD}$ Pulse Width	(Note 6)	●	80	30	ns	
$t_6$	LSB SCK High to $\overline{\text{CS}}/\text{LD}$ High	(Note 6)	●	30	4	ns	
$t_7$	$\overline{\text{CS}}/\text{LD}$ Low to SCK High	(Note 6)	●	80	26	ns	
$t_8$	$D_{OUT}$ Propagation Delay	$C_{LOAD} = 15\text{pF}$ (Note 6)	●	5	26	80	ns
$t_9$	SCK Low to $\overline{\text{CS}}/\text{LD}$ Low	(Note 6)	●	20	0	ns	
$t_{10}$	$\overline{\text{CLR}}$ Pulse Width	(Note 6)	●	100	37	ns	
$t_{11}$	$\overline{\text{CS}}/\text{LD}$ High to SCK Positive Edge	(Note 6)	●	30	0	ns	
	SCK Frequency	(Notes 6 and 8)	●			16.7	MHz
<b><math>V_{CC} = 2.7\text{V}</math> to <math>5.5\text{V}</math></b>							
$t_1$	$D_{IN}$ Valid to SCK Setup	(Note 6)	●	60	20	ns	
$t_2$	$D_{IN}$ Valid to SCK Hold	(Note 6)	●	0	-14	ns	
$t_3$	SCK High Time	(Note 6)	●	50	8	ns	
$t_4$	SCK Low Time	(Note 6)	●	50	12	ns	

## TIMING CHARACTERISTICS

The ● denotes specifications which apply over the full operating temperature range, otherwise specifications are at  $T_A = 25^\circ\text{C}$ . (See Figure 1)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
$t_5$	$\overline{\text{CS}}/\text{LD}$ Pulse Width	(Note 6)	●	100	30		ns
$t_6$	LSB SCK High to $\overline{\text{CS}}/\text{LD}$ High	(Note 6)	●	50	5		ns
$t_7$	$\overline{\text{CS}}/\text{LD}$ Low to SCK High	(Note 6)	●	100	27		ns
$t_8$	$D_{\text{OUT}}$ Propagation Delay	$C_{\text{LOAD}} = 15\text{pF}$ (Note 6)	●	5	47	150	ns
$t_9$	SCK Low to $\overline{\text{CS}}/\text{LD}$ Low	(Note 6)	●	30	0		ns
$t_{10}$	CLR Pulse Width	(Note 6)	●	120	41		ns
$t_{11}$	$\overline{\text{CS}}/\text{LD}$ High to SCK Positive Edge	(Note 6)	●	30	0		ns
	SCK Frequency	(Notes 6 and 8)	●			10	MHz

**Note 1:** Absolute maximum ratings are those values beyond which the life of a device may be impaired.

**Note 2:** Nonlinearity and monotonicity are defined and tested at  $V_{\text{CC}} = 5\text{V}$ ,  $V_{\text{REF}} = 4.096\text{V}$ , from code 20 to code 1023. See Rail-to-Rail output considerations.

**Note 3:** Digital inputs at 0V or  $V_{\text{CC}}$ .

**Note 4:** Load is  $10\text{k}\Omega$  in parallel with  $100\text{pF}$ .

**Note 5:**  $V_{\text{CC}} = V_{\text{REF}} = 5\text{V}$ .

**Note 6:** Guaranteed by design and not subject to test.

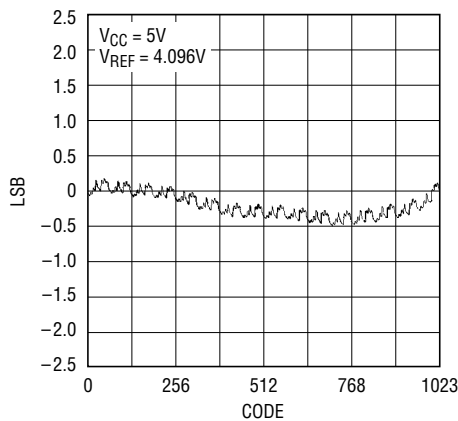
**Note 7:** Measured at code 20.

**Note 8:** If a continuous clock is used,  $\overline{\text{CS}}/\text{LD}$  timing ( $t_7$  and  $t_9$ ) will limit the maximum clock frequency to 5MHz at 4.5V to 5.5V (3.85MHz at 2.7V to 5.5V).

**Note 9:** Any output shorted.

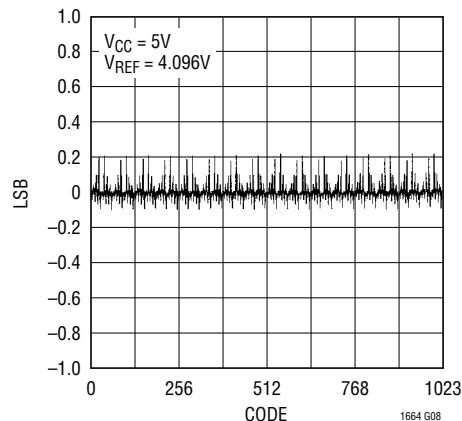
## TYPICAL PERFORMANCE CHARACTERISTICS

Integral Nonlinearity (INL)



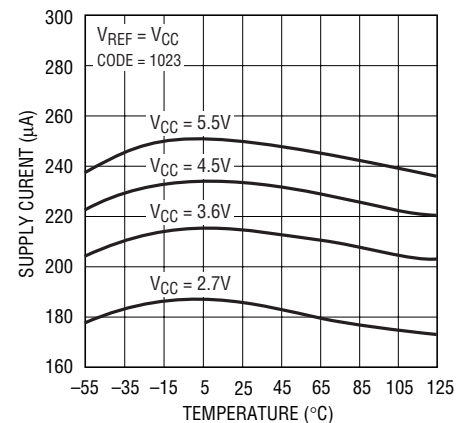
1664 G07

Differential Nonlinearity (DNL)



1664 G08

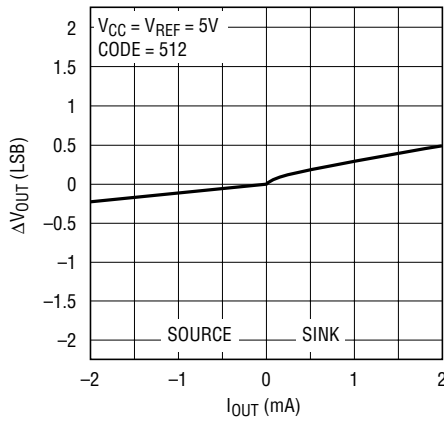
Supply Current vs Temperature



1664 G11

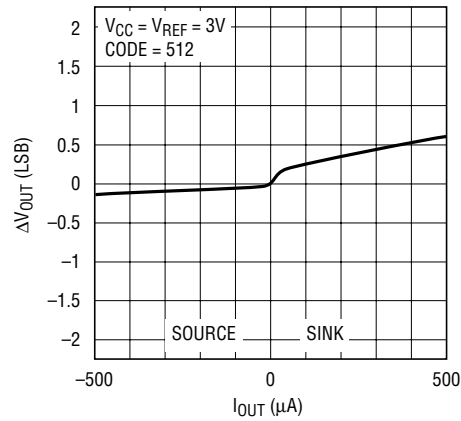
# TYPICAL PERFORMANCE CHARACTERISTICS

**Load Regulation vs Output Current**



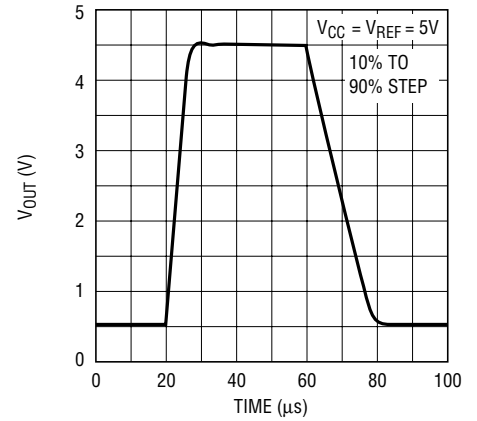
1664 G09

**Load Regulation vs Output Current**



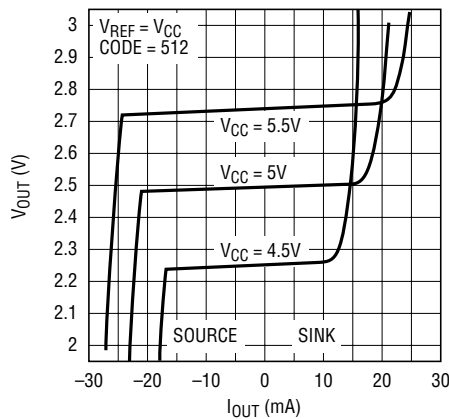
1664 G10

**Large-Signal Step Response**



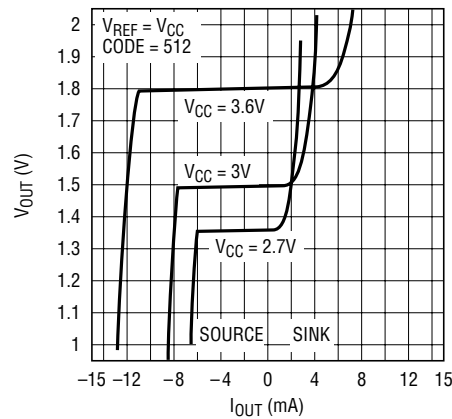
1664 G05

**Midscale Output Voltage vs Load Current**



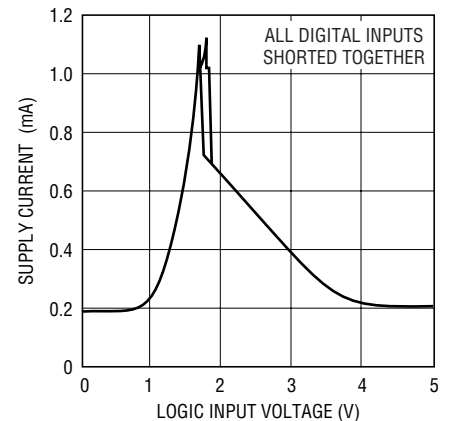
1664 G01

**Midscale Output Voltage vs Load Current**



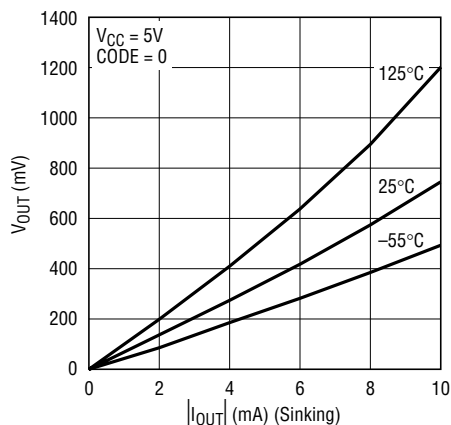
1664 G02

**Supply Current vs Logic Input Voltage**



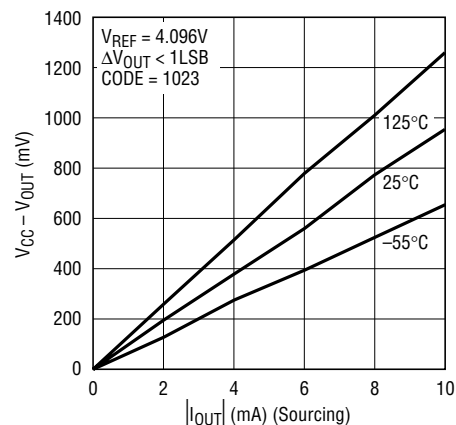
1664 G12

**Minimum V<sub>OUT</sub> vs Load Current (Output Sinking)**



1664 G04

**Minimum Supply Headroom vs Load Current (Output Sourcing)**



1664 G03

## PIN FUNCTIONS

**GND (Pin 1):** System Ground.

**V<sub>OUTA</sub> to V<sub>OUTD</sub> (Pins 2–5):** DAC Analog Voltage Outputs. The output range is

$$0 \text{ to } \left( \frac{1023}{1024} \right) V_{REF}$$

**REF (Pin 6):** Reference Voltage Input.  $0V \leq V_{REF} \leq V_{CC}$ .

**$\overline{CS/LD}$  (Pin 7):** Serial Interface Chip Select/Load Input. When  $\overline{CS/LD}$  is low, SCK is enabled for shifting data on D<sub>IN</sub> into the register. When  $\overline{CS/LD}$  is pulled high, SCK is disabled and data is loaded from the shift register into the specified DAC register(s), updating the analog output(s). CMOS and TTL compatible.

**SCK (Pin 8):** Serial Interface Clock Input. CMOS and TTL compatible.

**D<sub>IN</sub> (Pin 9):** Serial Interface Data Input. Data on the D<sub>IN</sub> pin is shifted into the 16-bit register on the rising edge of SCK. CMOS and TTL compatible.

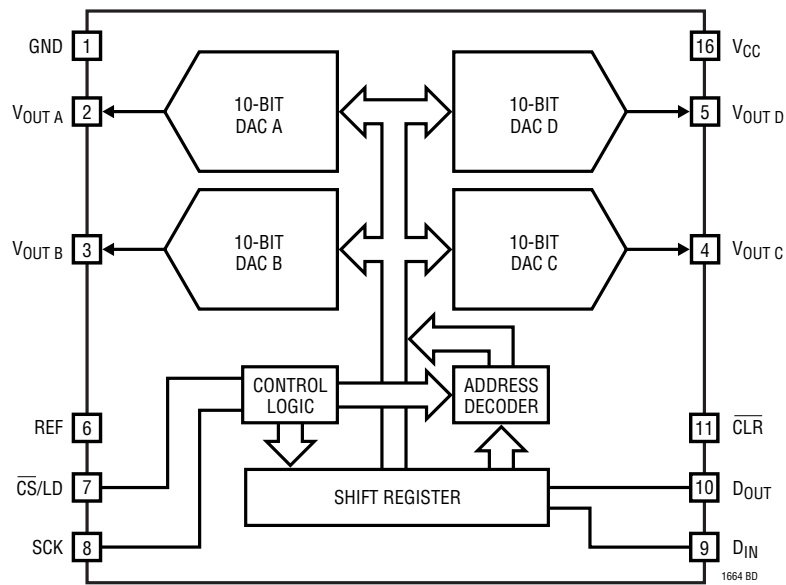
**D<sub>OUT</sub> (Pin 10):** Serial Interface Data Output. Data appears on D<sub>OUT</sub> 16 positive SCK edges after being applied to D<sub>IN</sub>. May be tied to D<sub>IN</sub> of another serial device for daisy-chain operation. CMOS and TTL compatible.

**$\overline{CLR}$  (Pin 11):** Asynchronous Clear Input. All internal shift and DAC registers are cleared to zero at the falling edge of the  $\overline{CLR}$  signal, forcing the analog outputs to zero scale. CMOS and TTL compatible.

**NC (Pins 12–15):** Make no electrical connection to these pins.

**V<sub>CC</sub> (Pin 16):** Supply Voltage Input.  $2.7V \leq V_{CC} \leq 5.5V$ .

## BLOCK DIAGRAM



## TIMING DIAGRAM

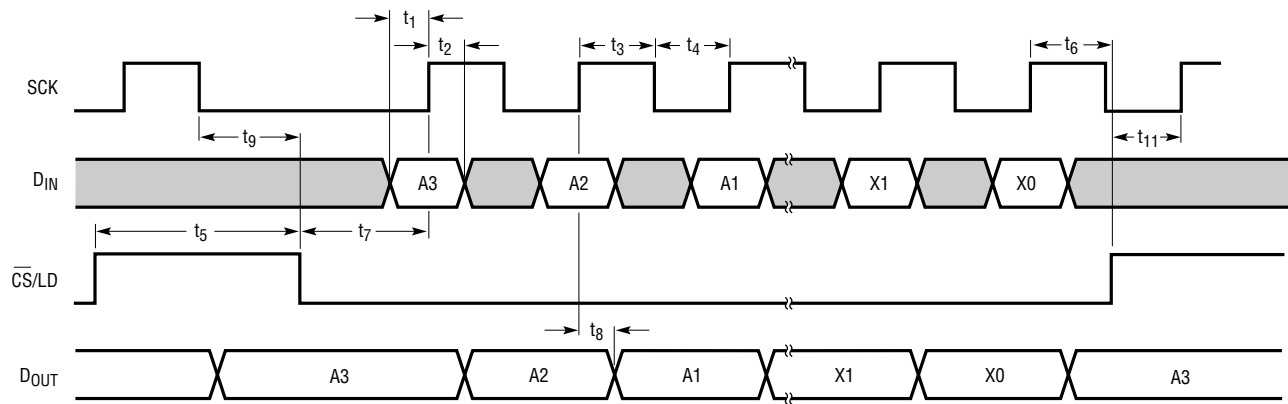


Figure 1

1664 F01

## OPERATION

### Transfer Function

The transfer function is

$$V_{\text{OUT(IDEAL)}} = \left( \frac{k}{1024} \right) V_{\text{REF}}$$

where  $k$  is the decimal equivalent of the binary DAC input code and  $V_{\text{REF}}$  is the voltage at REF (Pin 6).

### Power-On Reset

The LTC1664 clears the outputs to zero scale when power is first applied, making system initialization consistent and repeatable.

### Power Supply Sequencing

The voltage at REF (Pin 6) should be kept within the range  $-0.3V \leq V_{\text{REF}} \leq V_{\text{CC}} + 0.3V$  (see Absolute Maximum Ratings). Particular care should be taken to observe these limits during power supply turn-on and turn-off sequences, when the voltage at  $V_{\text{CC}}$  (Pin 16) is in transition. If it is not possible to sequence the supplies, connect a Schottky diode from REF (anode) to  $V_{\text{CC}}$  (cathode).

### Serial Interface

Referring to Figure 2: With  $\overline{\text{CS/LD}}$  held low, data on the  $D_{\text{IN}}$  input is shifted into the 16-bit shift register on the positive edge of SCK. The 4-bit DAC address, A3-A0, is loaded first (see Table 2), then the 10-bit input code, D9-D0, ordered MSB-to-LSB in each case. Two don't-care bits, X1-X0, are loaded last. When the full 16-bit input word has been shifted in,  $\overline{\text{CS/LD}}$  is pulled high, loading the DAC register with the word and causing the addressed DAC output(s) to update. The clock is disabled internally when  $\overline{\text{CS/LD}}$  is high. Note: SCK must be low before  $\overline{\text{CS/LD}}$  is pulled low.

The buffered serial output of the shift register is available on the  $D_{\text{OUT}}$  pin, which swings from GND to  $V_{\text{CC}}$ . Data appears on  $D_{\text{OUT}}$  16 positive SCK edges after being applied to  $D_{\text{IN}}$ .

Multiple LTC1664's can be controlled from a single 3-wire serial port (i.e., SCK,  $D_{\text{IN}}$  and  $\overline{\text{CS/LD}}$ ) by using the included "daisy-chain" facility. A series of  $m$  chips is configured by connecting each  $D_{\text{OUT}}$  (except the last) to  $D_{\text{IN}}$  of the next chip, forming a single  $16m$ -bit shift register. The SCK and  $\overline{\text{CS/LD}}$  signals are common to all chips in the chain. In use,  $\overline{\text{CS/LD}}$  is held low while  $m$  16-bit words are clocked to  $D_{\text{IN}}$  of the first chip;  $\overline{\text{CS/LD}}$  is then pulled high, updating all of them simultaneously.

### Sleep Mode

DAC address  $1110_{\text{b}}$  is reserved for the special Sleep instruction (see Table 2). In this mode, the digital interface stays active while the analog circuits are disabled; static power consumption is thus virtually eliminated. The reference input and analog outputs are set in a high impedance state and all DAC settings are retained in memory so that when Sleep mode is exited, the outputs of DACs not updated by the Wake command are restored to their last active state.

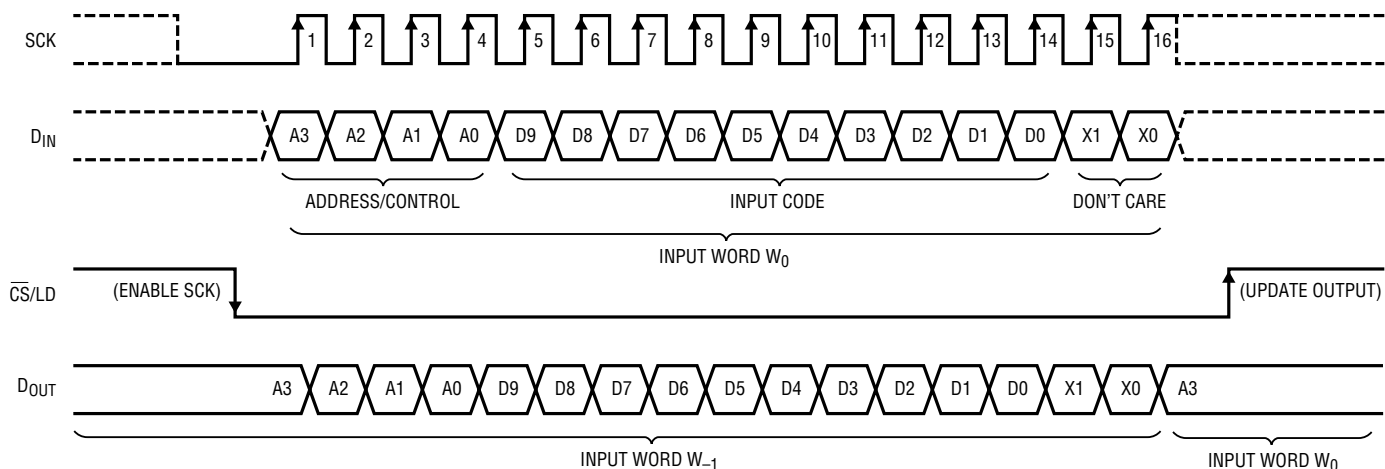
Sleep mode is initiated by performing a load sequence to address  $1110_{\text{b}}$  (the DAC input word D9-D0 is ignored). Once in Sleep mode, a load sequence to any other address (including "No Change" address  $0000_{\text{b}}$ ) causes the LTC1664 to Wake. It is possible to keep one or more chips of a daisy chain in continuous Sleep mode by giving the Sleep instruction to these chips each time the active chips in the chain are updated.

Table 1. LTC1664 Input Word

A3	A2	A1	A0	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	X1	X0
Address/Control				Input Code										Don't Care	



## OPERATION



1664 F02

Figure 2. LTC1664 Register Loading Sequence

Table 2. DAC Address/Control Functions

ADDRESS/CONTROL				DAC STATUS	SLEEP STATUS
A3	A2	A1	A0		
0	0	0	0	No Change	Wake
0	0	0	1	Load DAC A	Wake
0	0	1	0	Load DAC B	Wake
0	0	1	1	Load DAC C	Wake
0	1	0	0	Load DAC D	Wake
0	1	0	1	Reserved	
0	1	1	0	Reserved	
0	1	1	1	Reserved	
1	0	0	0	Reserved	
1	0	0	1	Reserved	
1	0	1	0	Reserved	
1	0	1	1	Reserved	
1	1	0	0	Reserved	
1	1	0	1	Reserved	
1	1	1	0	No Change	Sleep
1	1	1	1	Load ALL DACs with Same 10-Bit Code	Wake

## OPERATION

### Voltage Outputs

Each of the four rail-to-rail output amplifiers contained in the LTC1664 can source or sink up to 5mA. The outputs swing to within a few millivolts of either supply rail when unloaded and have an equivalent output resistance of  $85\Omega$  when driving a load to the rails. The output amplifiers are stable driving capacitive loads of up to 1000pF.

A small resistor placed in series with the output can be used to achieve stability for any load capacitance. A  $1\mu\text{F}$  load can be successfully driven by inserting a  $20\Omega$  resistor; a  $2.2\mu\text{F}$  load needs only a  $10\Omega$  resistor. In either case, larger values of resistance, capacitance or both may be safely substituted for the values given.

### Rail-to-Rail Output Considerations

In any rail-to-rail voltage output DAC, the output is limited to voltages within the supply range.

If the DAC offset is negative, the output for the lowest codes limits at 0V as shown in Figure 3b.

Similarly, limiting can occur near full scale when the REF pin is tied to  $V_{CC}$ . If  $V_{REF} = V_{CC}$  and the DAC full-scale error (FSE) is positive, the output for the highest codes limits at  $V_{CC}$  as shown in Figure 3c. No full-scale limiting can occur if  $V_{REF}$  is less than  $V_{CC} - \text{FSE}$ .

Offset and linearity are defined and tested over the region of the DAC transfer function where no output limiting can occur.

## OPERATION

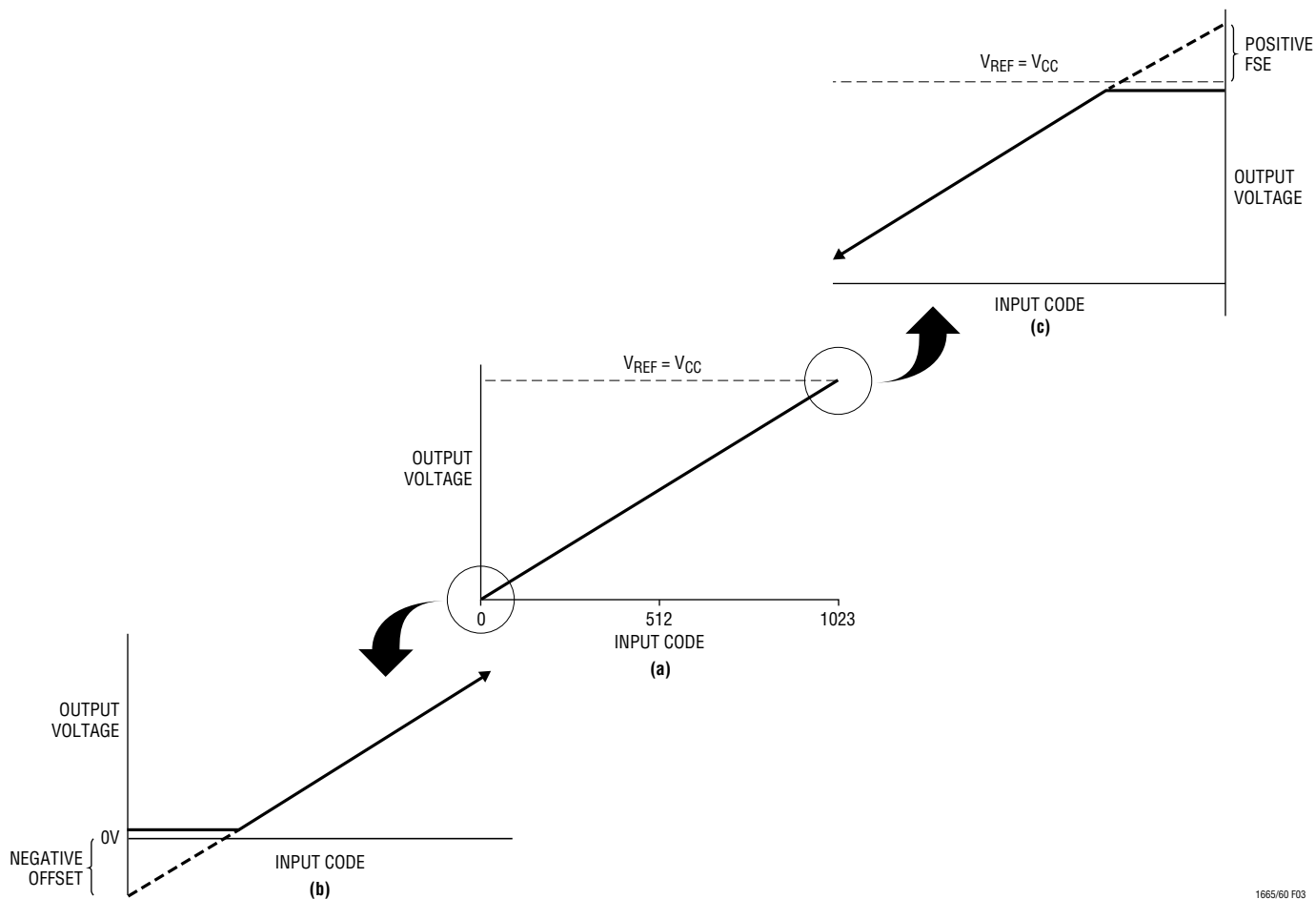
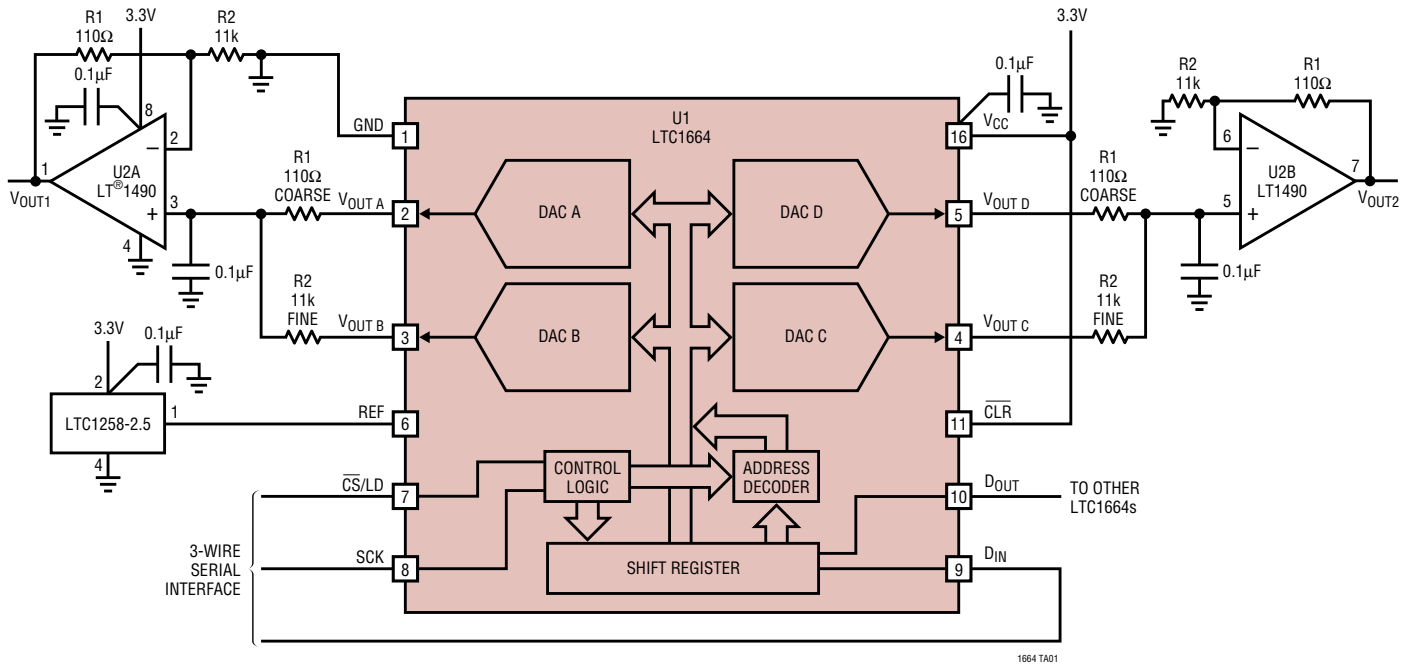


Figure 3. Effects of Rail-to-Rail Operation On a DAC Transfer Curve. (a) Overall Transfer Function (b) Effect of Negative Offset for Codes Near Zero Scale (c) Effect of Positive Full-Scale Error for Input Codes Near Full Scale When  $V_{REF} = V_{CC}$

1665/60 F03

TYPICAL APPLICATIONS

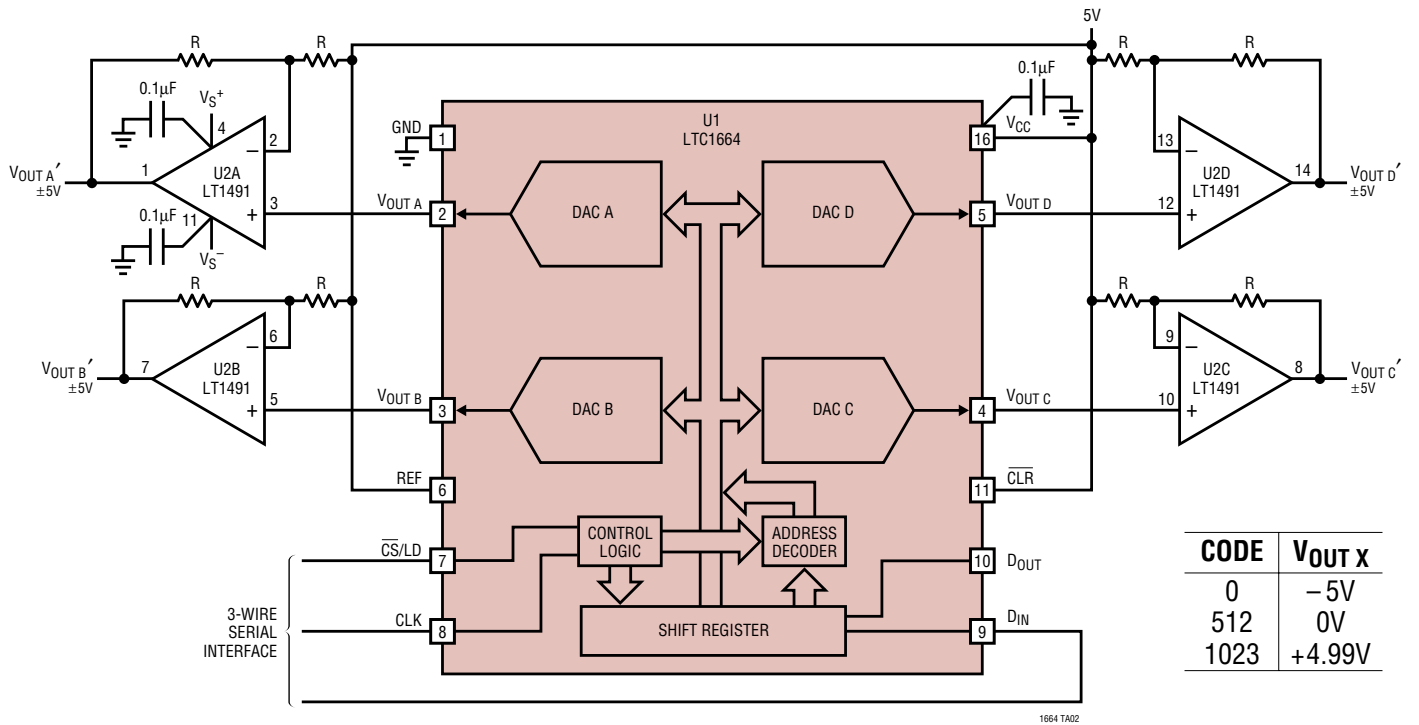
A Low Power Dual Trim Circuit with Coarse/Fine Adjustment



$$\begin{aligned}
 V_{OUT1} &= V_{REF} \left( \frac{CODE A}{1024} + \frac{R1}{R2} \frac{CODE B}{1024} \right) \\
 &= 2.5V \left( \frac{CODE A}{1024} + \frac{1}{100} \frac{CODE B}{1024} \right) \\
 V_{OUT2} &= V_{REF} \left( \frac{CODE D}{1024} + \frac{R1}{R2} \frac{CODE C}{1024} \right) \\
 &= 2.5V \left( \frac{CODE D}{1024} + \frac{1}{100} \frac{CODE C}{1024} \right)
 \end{aligned}$$

# TYPICAL APPLICATIONS

A 4-Channel Bipolar Output Voltage Circuit Configuration

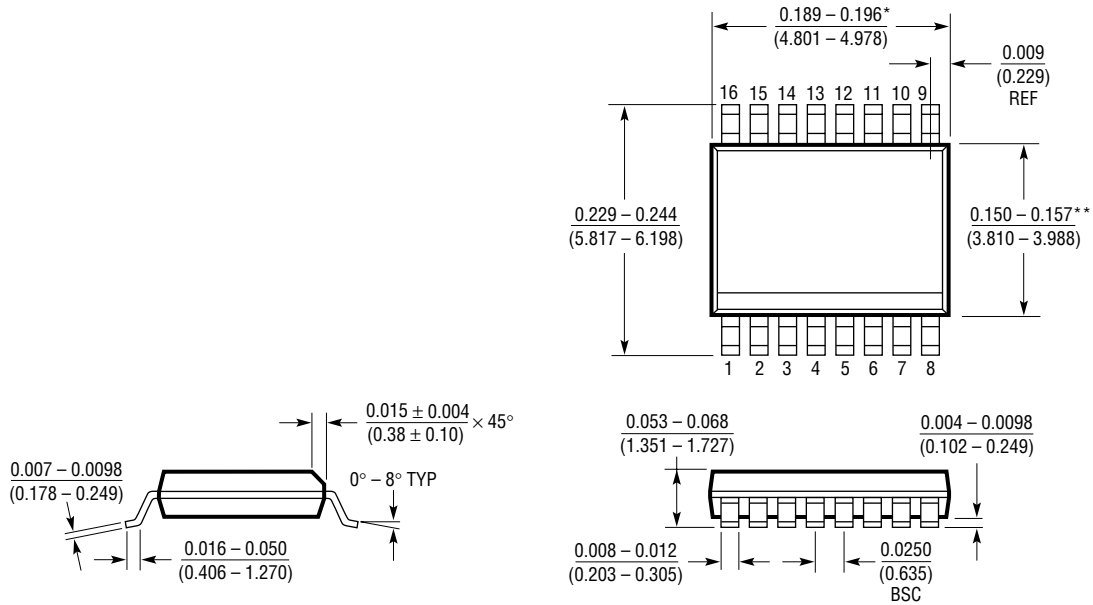


1664 TA02

**PACKAGE DESCRIPTION**

Dimensions in inches (millimeters) unless otherwise noted.

**GN Package**  
**16-Lead Plastic SSOP (Narrow 0.150)**  
 (LTC DWG # 05-08-1641)

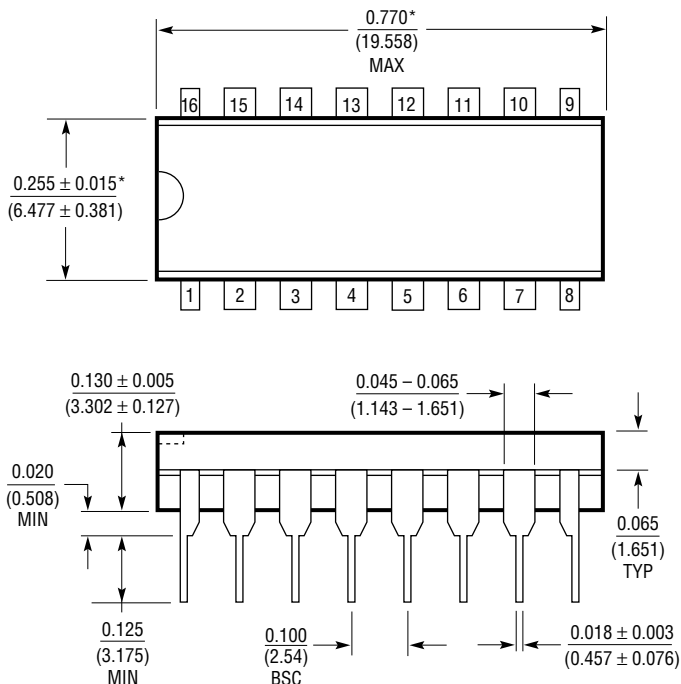


\* DIMENSION DOES NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.006" (0.152mm) PER SIDE  
 \*\* DIMENSION DOES NOT INCLUDE INTERLEAD FLASH. INTERLEAD FLASH SHALL NOT EXCEED 0.010" (0.254mm) PER SIDE

GN16 (SSOP) 1098

**PACKAGE DESCRIPTION** Dimensions in inches (millimeters) unless otherwise noted.

**N Package**  
**16-Lead PDIP (Narrow 0.300)**  
 (LTC DWG # 05-08-1510)

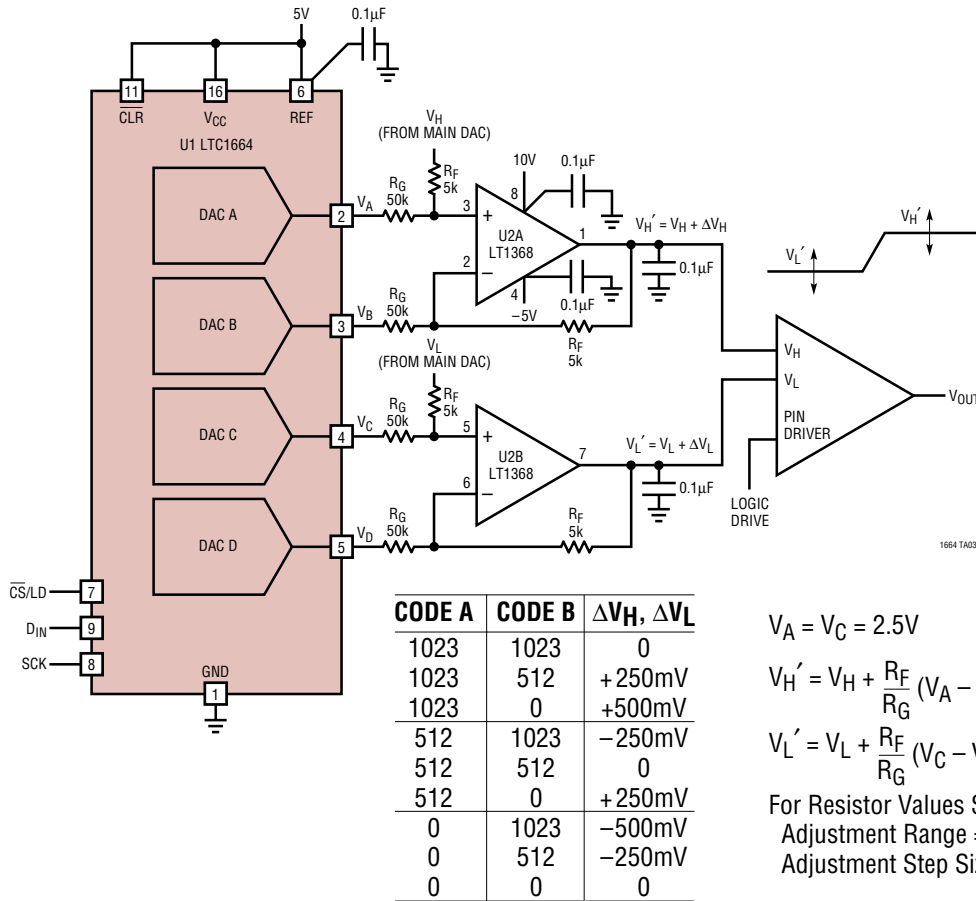


\*THESE DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.  
 MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.010 INCH (0.254mm)

N16 1098

## TYPICAL APPLICATION

An 11-Bit Pin Driver  $V_H$  and  $V_L$  Adjustment Circuit for ATE Applications



## RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTC1665/LTC1660	Octal 8/10-Bit $V_{OUT}$ DAC in 16-Pin Narrow SSOP	$V_{CC} = 2.7V$ to $5.5V$ , $60\mu A$ per DAC, Rail-to-Rail Output
LTC1661	Dual 10-Bit $V_{OUT}$ DAC in 8-Pin MSOP Package	$V_{CC} = 2.7V$ to $5.5V$ , $60\mu A$ per DAC, Rail-to-Rail Output
LTC1662	Ultra Low Power Dual 10-Bit $V_{OUT}$ DAC in 8-Pin MSOP Package	$V_{CC} = 2.7V$ to $5.5V$ , $1.5\mu A$ per DAC, Rail-to-Rail Output
LTC1663	Single 10-Bit $V_{OUT}$ DAC with 2-Wire Interface in SOT-23 Package	$V_{CC} = 2.7V$ to $5.5V$ , Internal Reference, $60\mu A$
LTC1446/LTC1446L	Dual 12-Bit $V_{OUT}$ DACs in SO-8 Package with Internal Reference	LTC1446: $V_{CC} = 4.5V$ to $5.5V$ , $V_{OUT} = 0V$ to $4.095V$ LTC1446L: $V_{CC} = 2.7V$ to $5.5V$ , $V_{OUT} = 0V$ to $2.5V$
LTC1448	Dual 12-Bit $V_{OUT}$ DAC in SO-8 Package	$V_{CC} = 2.7V$ to $5.5V$ , External Reference Can Be Tied to $V_{CC}$
LTC1454/LTC1454L	Dual 12-Bit $V_{OUT}$ DACs in SO-16 Package with Added Functionality	LTC1454: $V_{CC} = 4.5V$ to $5.5V$ , $V_{OUT} = 0V$ to $4.095V$ LTC1454L: $V_{CC} = 2.7V$ to $5.5V$ , $V_{OUT} = 0V$ to $2.5V$
LTC1458/LTC1458L	Quad 12-Bit Rail-to-Rail Output DACs with Added Functionality	LTC1458: $V_{CC} = 4.5V$ to $5.5V$ , $V_{OUT} = 0V$ to $4.095V$ LTC1458L: $V_{CC} = 2.7V$ to $5.5V$ , $V_{OUT} = 0V$ to $2.5V$
LT1460	Micropower Precision Series Reference, 2.5V, 5V, 10V Versions	0.075% Max, 10ppm/°C Max, Only $130\mu A$ Supply Current
LTC1590	Dual 12-Bit $I_{OUT}$ DAC in SO-16 Package	$V_{CC} = 4.5V$ to $5.5V$ , 4-Quadrant Multiplication
LTC1654	Dual 14-Bit DAC in SO-8 Footprint	1LBS DNL, Selectable Speed/Power
LTC1659	Single Rail-to-Rail 12-Bit $V_{OUT}$ DAC in 8-Lead MSOP Package	Low Power Multiplying $V_{OUT}$ DAC. Output Swings from GND to REF. REF Input Can Be Tied to $V_{CC}$