EN55022B Compliant 36V_{IN}, 15V_{OUT}, 8A, DC/DC µModule Regulator

FEATURES

- **Complete Low EMI Switch Mode Power Supply**
- **EN55022 Class B Compliant**
- **Wide Input Voltage Range: 5V to 36V**
- **8A Output Current**
- **3.3V to 15V Output Voltage Range**
- **Low Input and Output Referred Noise**
- **Output Voltage Tracking and Margining**
- **PLL Frequency Synchronization**
- **2% Maximum Total DC Error**
- **Power Good Tracks with Margining**
- **Current Foldback Protection**
- **Parallel/Current Sharing**
- Ultrafast Transient Response
- Current Mode Control
- Programmable Soft-Start
- Output Overvoltage Protection
- –55°C to 125°C Operating Temperature Range (LTM4613MPV)
- Small Surface Mount Footprint, Low Profile (15mm × 15mm × 4.32mm) LGA Package

APPLICATIONS

- Telecom and Networking Equipment
- Industrial and Avionic Equipment
- RF Systems

DESCRIPTION

The LTM®4613 is a complete, ultralow noise, 8A switch mode DC/DC power supply. Included in the package are the switching controller, power FETs, inductor and all support components. Operating over an input voltage range of 5V to 36V, the LTM4613 supports an output voltage range of 3.3V to 15V, set by a single external resistor. Only bulk input and output capacitors are needed to finish the design.

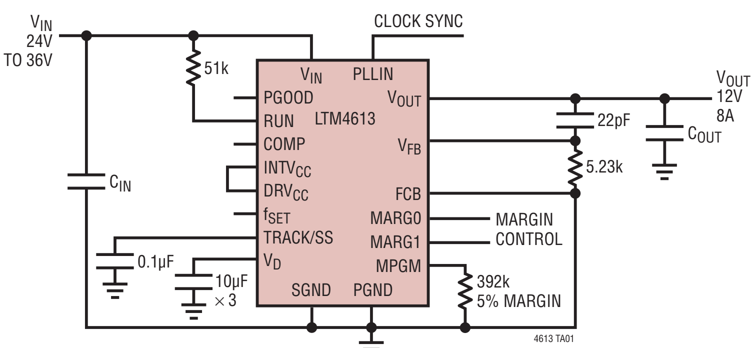
High switching frequency and an adaptive on-time current mode architecture enables a very fast transient response to line and load changes without sacrificing stability.

The onboard input filter and noise cancellation circuits achieve low noise coupling, thus effectively reducing the electromagnetic interference (EMI)—see Figure 7. Furthermore, the DC/DC µModule® regulator can be synchronized with an external clock to reduce undesirable frequency harmonics and allow PolyPhase® operation for high load currents.

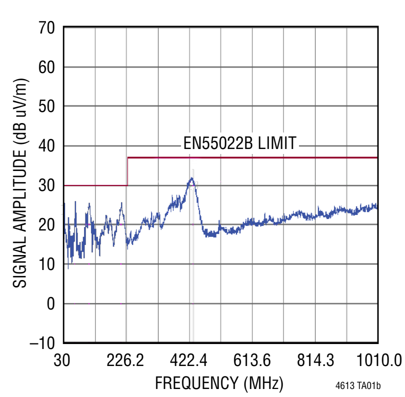
The LTM4613 is offered in a space saving and thermally enhanced 15mm × 15mm × 4.32mm LGA package, which enables utilization of unused space on the bottom of PC boards for high density point-of-load regulation. The LTM4613 is Pb-free and RoHS compliant.

TYPICAL APPLICATION

12V/8A Ultralow Noise µModule with 24V to 36V Input



Radiated Emission Scan with 24V_{IN} to 12V_{OUT} at 8A



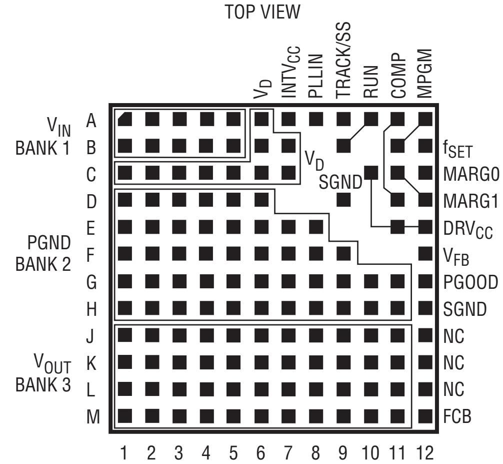
ABSOLUTE MAXIMUM RATINGS

(Note 1)

$INTV_{CC}$, DRV_{CC} .... –0.3V to 6V
V_{OUT} .... –0.3V to 16V
PLLIN, FCB, TRACK/SS, MPGM, MARG0,
MARG1, PGOOD ....–0.3V to $INTV_{CC}$ + 0.3V
RUN .... –0.3V to 5V
V_{FB}, COMP .... –0.3V to 2.7V
V_{IN}, V_D .... –0.3V to 36V
Internal Operating Temperature Range (Note 2)
E- and I-Grades.................................–40°C to 125°C
MP-Grade ....–55°C to 125°C
Storage Temperature Range ....–55°C to 125°C
Peak Package Body Temperature .... 245°C

PIN CONFIGURATION

TOP VIEW



LGA PACKAGE
133-LEAD (15mm × 15mm × 4.32mm)
T_{JMAX} = 125°C, θ_{JCtop} = 17°C/w, $\theta_{JCbottom}$ = 2.3°C/W, θ_{JA} = 11°C/W to 14°C/W,
θ_{JA} DERIVED FROM 95mm × 76mm PCB WITH 4 LAYERS
WEIGHT = 1.7g

ORDER INFORMATION

LEAD FREE FINISH	TRAY	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LTM4613EV#PBF	LTM4613EV#PBF	LTM4613V	133-Lead (15mm × 15mm × 4.32mm) LGA	–40°C to 125°C
LTM4613IV#PBF	LTM4613IV#PBF	LTM4613V	133-Lead (15mm × 15mm × 4.32mm) LGA	–40°C to 125°C
LTM4613MPV#PBF	LTM4613MPV#PBF	LTM4613V	133-Lead (15mm × 15mm × 4.32mm) LGA	–55°C to 125°C

Consult LTC Marketing for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
This product is only offered in trays. For more information go to: http://www.linear.com/packaging/

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full internal operating temperature range, otherwise specifications are at T_A = 25°C (Note 2), V_{IN} = 24V, unless otherwise noted. Per Typical Application (front page) configuration.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
$V_{IN(DC)}$	Input DC Voltage		●	5		36	V
$V_{OUT(DC)}$	Output Voltage, Total Variation with Line and Load	C_{IN} = 10µF × 3, C_{OUT} = 47µF ×4; FCB = 0, V_{IN} = 24V to 36V, V_{OUT} = 12V	●	11.83	12.07	12.31	V
Input Specifications							
$V_{IN(UVLO)}$	Undervoltage Lockout Threshold	I_{OUT} = 0A			3.2	4.8	V
$I_{INRUSH(VIN)}$	Input Inrush Current at Start-Up	I_{OUT} = 0A; C_{IN} = 10µF × 3, C_{OUT} = 47µF ×4; C_{SS} = 22nF V_{OUT} = 12V V_{IN} = 24V V_{IN} = 36V			 150 120		 mA mA
$I_{Q(VIN)}$	Input Supply Bias Current	V_{IN} = 36V, V_{OUT} = 12V, Switching Continuous, I_{OUT} = 0A V_{IN} = 24V, V_{OUT} = 12V, Switching Continuous, I_{OUT} = 0A Shutdown, RUN = 0, V_{IN} = 36V			78 60 50		mA mA µA
$I_{S(VIN)}$	Input Supply Current	V_{IN} = 36V, V_{OUT} = 12V, I_{OUT} = 8A V_{IN} = 24V, V_{OUT} = 12V, I_{OUT} = 8A			2.90 4.26		A A
V_{INTVCC}	Internal V_{CC} Voltage	V_{IN} = 36V, RUN > 2V, I_{OUT} = 0A		4.7	5	5.3	V
Output Specifications							
$I_{OUT(DC)}$	Output Continuous Current Range	V_{IN} = 24V, V_{OUT} = 12V (Note 4)		0		8	A
$\frac{\Delta V_{OUT(LINE)}}{V_{OUT}}$	Line Regulation Accuracy	V_{OUT} = 12V, FCB = 0V, V_{IN} = 24V to 36V, I_{OUT} = 0A	 ●		 0.05	 0.3	 %
$\frac{\Delta V_{OUT(LOAD)}}{V_{OUT}}$	Load Regulation Accuracy	V_{OUT} = 12V, FCB = 0V, I_{OUT} = 0A to 8A (Note 4) V_{IN} = 36V V_{IN} = 24V	 ● ●		 0.5 0.5	 0.75 0.75	 % %
$V_{IN(AC)}$	Input Ripple Voltage	I_{OUT} = 0A, C_{IN} = 1 × 10µF X5R Ceramic and 1 × 100µF Electrolytic, 3 × 10µF X5R Ceramic on V_D Pins V_{IN} = 24V, V_{OUT} = 12V (Note 5)			 10		 mV_{P-P}
$V_{OUT(AC)}$	Output Ripple Voltage	I_{OUT} = 0A, C_{OUT} = 1 × 10µF, 4 × 47µF X5R Ceramic V_{IN} = 24V, V_{OUT} = 12V			 19		 mV_{P-P}
f_S	Output Ripple Voltage Frequency	V_{IN} = 24V, V_{OUT} = 12V, I_{OUT} = 0A			600		kHz
$\Delta V_{OUT(START)}$	Turn-On Overshoot	C_{OUT} = 47µF ×4, V_{OUT} = 12V, I_{OUT} = 0A, C_{SS} = 22nF V_{IN} = 36V V_{IN} = 24V			 20 20		 mV mV
t_{START}	Turn-On Time	C_{OUT} = 47µF ×4, V_{OUT} = 12V, I_{OUT} = 0A, C_{SS} = Open V_{IN} = 36V V_{IN} = 24V			 0.3 0.3		 ms ms
$\Delta V_{OUT(LS)}$	Peak Deviation for Dynamic Load	Load: 0% to 50% to 0% of Full Load C_{OUT} = 1 × 10µF, 3 × 47µF X5R Ceramic, 1 × 47µF POSCAP V_{IN} = 24V, V_{OUT} = 12V			 250		 mV
t_{SETTLE}	Settling Time for Dynamic Load Step	Load: 0% to 50% to 0% of Full Load C_{OUT} = 1 × 10µF, 3 × 47µF X5R Ceramic, 1 × 47µF POSCAP V_{IN} = 24V, V_{OUT} = 12V			100		µs
$I_{OUT(PK)}$	Output Current Limit	C_{OUT} = 47µF ×4 V_{IN} = 36V, V_{OUT} = 12V V_{IN} = 24V, V_{OUT} = 12V			 12 12		 A A

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full internal operating temperature range, otherwise specifications are at T_A = 25°C (Note 2), V_{IN} = 24V, unless otherwise noted. Per Typical Application (front page) configuration.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Control Section							
V_{FB}	Voltage at V_{FB} Pin	I_{OUT} = 0A, V_{OUT} = 12V	●	0.591	0.6	0.609	V
V_{RUN}	RUN Pin On/Off Threshold			1	1.5	1.9	V
$I_{SS/TRACK}$	Soft-Start Charging Current	$V_{SS/TRACK}$ = 0V		–1	–1.5	–2	μA
V_{FCB}	Forced Continuous Threshold			0.57	0.6	0.63	V
I_{FCB}	Forced Continuous Pin Current	V_{FCB} = 0V			–1	–2	μA
$t_{ON(MIN)}$	Minimum On-Time	(Note 3)			50	100	ns
$t_{OFF(MIN)}$	Minimum Off-Time	(Note 3)			250	400	ns
R_{PLLIN}	PLLIN Input Resistor				50		kΩ
I_{DRVCC}	Current into DRV_{CC} Pin	V_{OUT} = 12V, I_{OUT} = 0A, DRV_{CC} = 5V			22	30	mA
R_{FBHI}	Resistor Between V_{OUT} and V_{FB} Pins			99.5	100	100.5	kΩ
V_{MPGM}	Margin Reference Voltage				1.18		V
V_{MARG0}, V_{MARG1}	MARG0, MARG1 Voltage Thresholds				1.4		V
PGOOD							
ΔV_{FBH}	PGOOD Upper Threshold	V_{FB} Rising		7	10	13	%
ΔV_{FBL}	PGOOD Lower Threshold	V_{FB} Falling		–7	–10	–13	%
$\Delta V_{FB(HYS)}$	PGOOD Hysteresis	V_{FB} Returning			1.5		%
V_{PGL}	PGOOD Low Voltage	I_{PGOOD} = 5mA			0.2	0.4	V

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: The LTM4613 is tested under pulsed load conditions such that $T_J \approx T_A$. The LTM4613E is guaranteed to meet performance specifications over the 0°C to 125°C internal operating temperature range. Specifications over the –40°C to 125°C internal operating temperature range are assured by design, characterization and correlation with statistical process controls. The LTM4613I is guaranteed to meet specifications over the –40°C to 125°C internal operating temperature range. The LTM4613MP is guaranteed and tested over the full –55°C to 125°C internal operating temperature range. Note that the maximum ambient temperature consistent with these specifications is determined by specific operating conditions in conjunction with board layout, the rated package thermal resistance and other environmental factors.

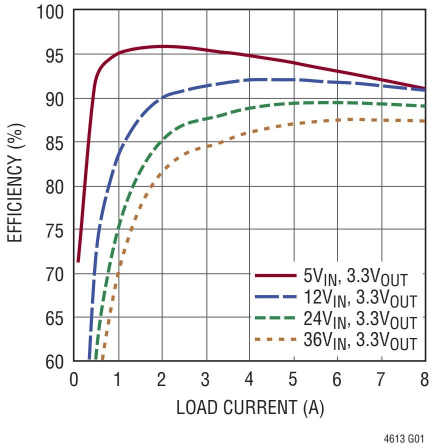
Note 3: 100% tested at die level only.

Note 4: See the Output Current Derating curves for different V_{IN}, V_{OUT} and T_A.

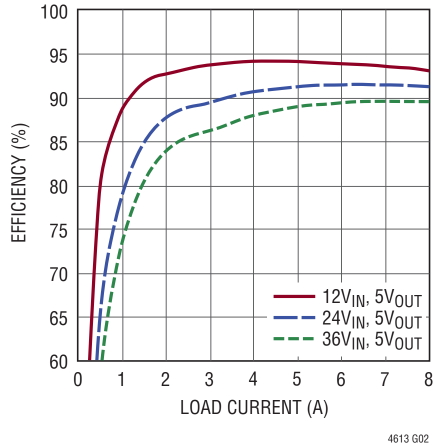
Note 5: Guaranteed by design.

TYPICAL PERFORMANCE CHARACTERISTICS (Refer to Figure 18)

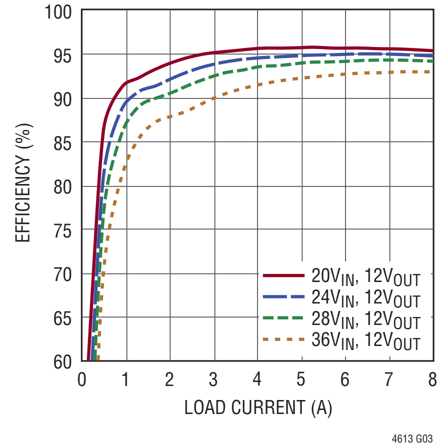
Efficiency vs Load Current with 3.3V_{OUT} (FCB = 0)



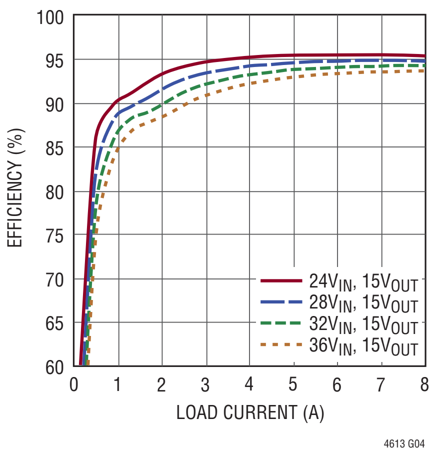
Efficiency vs Load Current with 5V_{OUT} (FCB = 0)



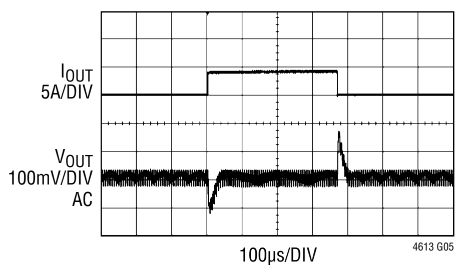
Efficiency vs Load Current with 12V_{OUT} (FCB = 0)



Efficiency vs Load Current with 15V_{OUT} (FCB = 0)

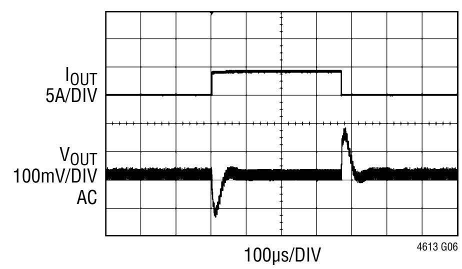


Transient Response from 12V_{IN} to 3.3V_{OUT}



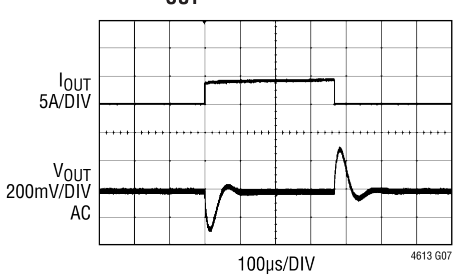
LOAD STEP: 0A TO 4A
C_{OUT} = 1 × 47µF POSCAP
1 × 10µF CERAMIC CAPACITOR AND
3 × 47µF CERAMIC CAPACITORS

Transient Response from 12V_{IN} to 5V_{OUT}



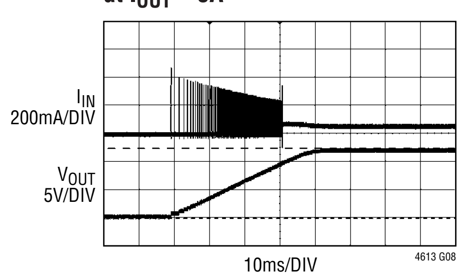
LOAD STEP: 0A TO 4A
C_{OUT} = 1 × 47µF POSCAP
1 × 10µF CERAMIC CAPACITOR AND
3 × 47µF CERAMIC CAPACITORS

Transient Response from 24V_{IN} to 12V_{OUT}



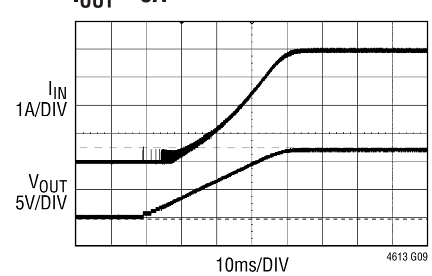
LOAD STEP: 0A TO 4A
C_{OUT} = 1 × 47µF POSCAP
1 × 10µF CERAMIC CAPACITOR AND
3 × 47µF CERAMIC CAPACITORS

Start-Up with 24V_{IN} to 12V_{OUT} at I_{OUT} = 0A



SOFT-START CAPACITOR: 0.1µF
C_{IN} = 2 × 10µF CERAMIC CAPACITORS AND
1 × 100µF OS-CON CAPACITOR

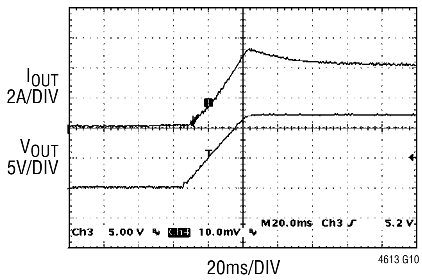
Start-Up with 24V_{IN} to 12V_{OUT} at I_{OUT} = 8A



SOFT-START CAPACITOR: 0.1µF
C_{IN} = 2 × 10µF CERAMIC CAPACITORS AND
1 × 100µF OS-CON CAPACITOR

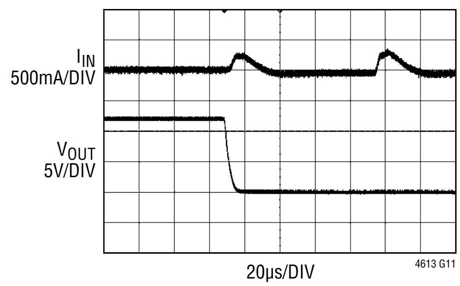
TYPICAL PERFORMANCE CHARACTERISTICS

Start-Up with $24V_{IN}$ to $12V_{OUT}$ at I_{OUT} = 8A, T_A = –55°C



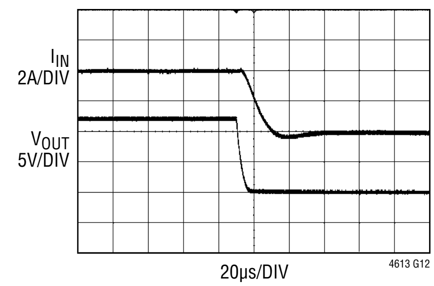
SOFT-START CAPACITOR: 0.1µF
C_{IN} = 2 × 10µF CERAMIC CAPACITORS AND
1 × 100µF OS-CON CAPACITOR

Short-Circuit with $24V_{IN}$ to $12V_{OUT}$ at I_{OUT} = 0A



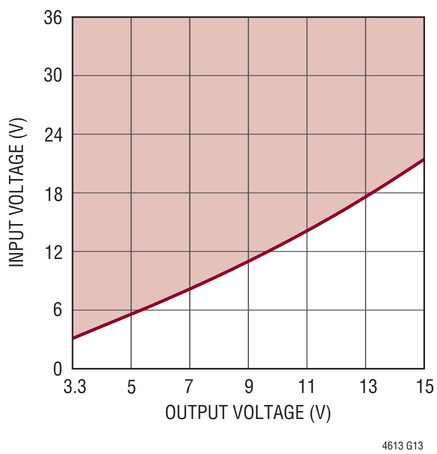
C_{OUT} = 1 × 47µF POSCAP,
1 × 10µF CERAMIC CAPACITORS
AND 3 × 47µF CERAMIC CAPACITORS

Short-Circuit with $24V_{IN}$ to $12V_{OUT}$ at I_{OUT} = 8A

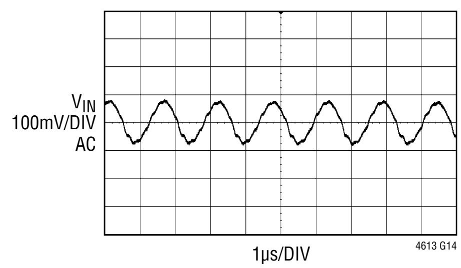


C_{OUT} = 1 × 47µF POSCAP,
1 × 10µF CERAMIC CAPACITORS
AND 3 × 47µF CERAMIC CAPACITORS

V_{IN} to V_{OUT} Step-Down Ratio

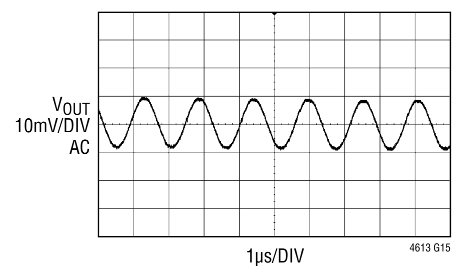


Input Ripple



V_{IN} = 24V
V_{OUT} = 12V AT 8A RESISTIVE LOAD
C_{IN} = 2 × 10µF CERAMIC CAPACITORS AND
1 × 100µF OS-CON CAPACITOR

Output Ripple



V_{IN} = 24V
V_{OUT} = 12V AT 8A RESISTIVE LOAD
C_{OUT} = 1 × 47µF POSCAP
1 × 10µF CERAMIC CAPACITOR AND
3 × 47µF CERAMIC CAPACITORS

PIN FUNCTIONS (See Package Description for Pin Assignments)

V_{IN} (Bank 1): Power Input Pins. Apply input voltage between these pins and PGND pins. Recommend placing input decoupling capacitance directly between V_{IN} pins and PGND pins.

PGND (Bank 2): Power Ground Pins for Both Input and Output Returns.

V_{OUT} (Bank 3): Power Output Pins. Apply output load between these pins and PGND pins. Recommend placing output decoupling capacitance directly between these pins and PGND pins (see the LTM4613 Pin Configuration below).

V_D (Pins C1 to C7, B6 to B7, A6): Top FET Drain Pins. Add more high frequency ceramic decoupling capacitors between V_D and PGND to handle the input RMS current and reduce the input ripple further.

DRV_{CC} (Pins C10, E11, E12): These pins normally connect to $INTV_{CC}$ for powering the internal MOSFET drivers. They can be biased up to 6V from an external supply with about 50mA capability. This improves efficiency at the higher input voltages by reducing power dissipation in the module. See the Applications Information section.

$INTV_{CC}$ (Pin A7): This pin is for additional decoupling of the 5V internal regulator.

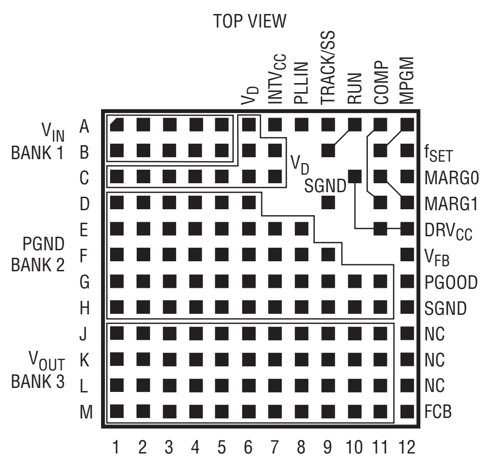
PLLIN (Pin A8): External Clock Synchronization Input to the Phase Detector. This pin is internally terminated to SGND with a 50k resistor. Apply a clock above 2V and below $INTV_{CC}$ subject to minimum on-time and minimum off-time requirements. See the Applications Information section.

FCB (Pin M12): Forced Continuous Input. Connect this pin to SGND to force continuous synchronization operation at light load or to $INTV_{CC}$ to enable discontinuous mode operation at light load.

TRACK/SS (Pin A9): Output Voltage Tracking and Soft-Start Pin. When the module is configured as a master output, then a soft-start capacitor is placed on this pin to ground to control the master ramp rate. A soft-start capacitor can be used for soft-start turn-on as a standalone regulator. Slave operation is performed by putting a resistor divider from the master output to the ground, and connecting the center point of the divider to this pin. See the Applications Information section.

MPGM (Pins A12, B11): Programmable Margining Input. A resistor from these pins to ground sets a current that is equal to 1.18V/R. This current multiplied by 10k will equal a value in millivolts that is a percentage of the 0.6V reference voltage. Leave floating if margining is not used. See the Applications Information section. To parallel LTM4613s, each requires an individual MPGM resistor. Do not tie MPGM pins together.

f_{SET} (Pin B12): Frequency Set Internally to 600kHz at 12V Output. An external resistor can be placed from this pin to ground to increase frequency or from this pin to V_{IN} to reduce frequency. See the Applications Information section for frequency adjustment.



LGA PACKAGE
133-LEAD (15mm × 15mm × 4.32mm)

LTM4613 Pin Configuration

PIN FUNCTIONS

V_{FB} (Pin F12): The Negative Input of the Error Amplifier. Internally, this pin is connected to V_{OUT} with a 100k 0.5% precision resistor. Different output voltages can be programmed with an additional resistor between the V_{FB} and SGND pins. See the Applications Information section.

MARG0 (Pin C12): LSB Logic Input for the Margining Function. Together with the MARG1 pin, the MARG0 pin will determine if a margin high, margin low, or no margin state is applied. The pin has an internal pull-down resistor of 50k. See the Applications Information section.

MARG1 (Pins C11, D12): MSB Logic Input for the Margining Function. Together with the MARG0 pin, the MARG1 pin will determine if a margin high, margin low, or no margin state is applied. The pins have an internal pull-down resistor of 50k. See the Applications Information section.

SGND (Pins D9, H12): Signal Ground Pins. These pins connect to PGND at output capacitor point.

COMP (Pins A11, D11): Current Control Threshold and Error Amplifier Compensation Point. The current comparator threshold increases with this control voltage. The voltage ranges from 0V to 2.4V with 0.7V corresponding to zero sense voltage (zero current).

PGOOD (Pin G12): Output Voltage Power Good Indicator. Open-drain logic output that is pulled to ground when the output voltage is not within ±10% of the regulation point, after a 25µs power bad mask timer expires.

RUN (Pins A10, B9): Run Control Pins. A voltage above 1.9V will turn on the module, and below 1V will turn off the module. A programmable UVLO function can be accomplished with a resistor from V_{IN} to this pin that has a 5.1V Zener to ground. Maximum pin voltage is 5V.

MTP (Pins J12, K12, L12): No Connect Pins. Leave floating. Used for mounting to PCB.

BLOCK DIAGRAM

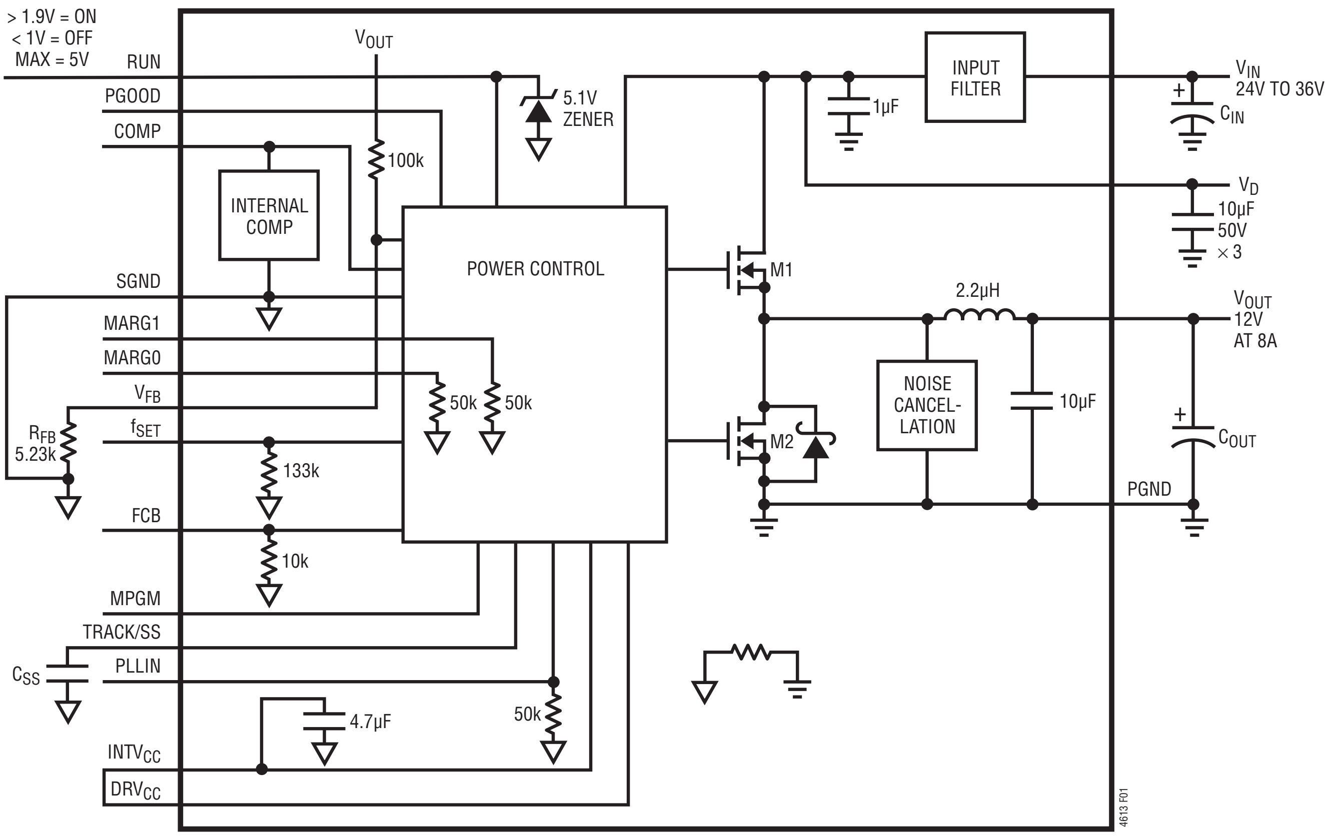


Figure 1. Simplified Block Diagram

DECOUPLING REQUIREMENTS

Specifications are at $T_A = 25°C$. Use Figure 1 configuration.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
C_{IN}	External Input Capacitor Requirement (V_{IN} = 24V to 36V, V_{OUT} = 12V)	I_{OUT} = 8A	30	100		μF
C_{OUT}	External Output Capacitor Requirement (V_{IN} = 24V to 36V, V_{OUT} = 12V)	I_{OUT} = 8A	100	220		μF

OPERATION

Power Module Description

The LTM4613 is a standalone nonisolated switch mode DC/DC power supply. It can deliver 8A of DC output current with minimal external input and output capacitors. This module provides a precisely regulated output voltage programmable via one external resistor from $3.3V_{DC}$ to $15V_{DC}$ over a wide 5V to 36V input voltage. The typical application schematic is shown in Figure 18.

The LTM4613 has an integrated constant on-time current mode regulator, ultralow $R_{DS(ON)}$ FETs with fast switching speed and integrated Schottky diodes. The typical switching frequency is 600kHz at full load at 12V output. With current mode control and internal feedback loop compensation, the LTM4613 module has sufficient stability margins and good transient performance under a wide range of operating conditions and with a wide range of output capacitors, even all ceramic output capacitors.

Current mode control provides cycle-by-cycle fast current limiting. Moreover, foldback current limiting is provided in an overcurrent condition when V_{FB} drops. Internal overvoltage and undervoltage comparators pull the open-drain PGOOD output low if the output feedback voltage exits a ±10% window around the regulation point. Furthermore, in an overvoltage condition, internal top FET M1 is turned off and bottom FET M2 is turned on and held on until the overvoltage condition clears.

Input filter and noise cancellation circuitry reduce the noise coupling to inputs and outputs, and ensure the electromagnetic interference (EMI) meets the limits of EN55022 Class B (see Figure 7).

Pulling the RUN pin below 1V forces the controller into its shutdown state, turning off both M1 and M2. At light load currents, discontinuous mode (DCM) operation can be enabled to achieve higher efficiency compared to continuous mode (CCM) by setting FCB pin higher than 0.6V.

When the DRV_{CC} pin is connected to $INTV_{CC}$, an integrated 5V linear regulator powers the internal gate drivers. If a 5V external bias supply is applied on DRV_{CC} pin, then an efficiency improvement will occur due to the reduced power loss in the internal linear regulator. This is especially true at the higher input voltage range.

The MPGM, MARG0, and MARG1 pins are used to support voltage margining, where the percentage of margin is programmed by the MPGM pin, while the MARG0 and MARG1 select positive or negative margining. The PLLIN pin provides frequency synchronization of the device to an external clock. The TRACK/SS pin is used for power supply tracking and soft-start programming.

APPLICATIONS INFORMATION

The typical LTM4613 application circuit is shown in Figure 18. External component selection is primarily determined by the input voltage, the maximum load current and the output voltage. Refer to Table 2 for specific external capacitor requirements for a particular application.

V_{IN} to V_{OUT} Stepdown Ratios

There are restrictions in the maximum V_{IN} and V_{OUT} step down ratio that can be achieved for a given input voltage. These constraints are shown in the Typical Performance Characteristic curve labeled "V_{IN} to V_{OUT} Step-Down Ratio." Note that additional thermal derating may be applied. See the Thermal Considerations and Output Current Derating section in this data sheet.

Output Voltage Programming and Margining

The PWM controller has an internal 0.6V reference voltage. As shown in the Block Diagram, a 100k 0.5% internal feedback resistor connects the V_{OUT} and V_{FB} pins together. Adding a resistor, R_{FB}, from the V_{FB} pin to the SGND pin programs the output voltage.

$$V_{OUT} = 0.6V \bullet \frac{100k + R_{FB}}{R_{FB}}$$

or equivalently,

$$R_{FB} = \frac{100k}{\frac{V_{OUT}}{0.6V} - 1}$$

APPLICATIONS INFORMATION

Table 1. R_{FB} Standard 1% Resistor Values vs V_{OUT}

V_{OUT} (V)	3.3	5	6	8	10	12	14	15
R_{FB} (kΩ)	22.1	13.7	11	8.06	6.34	5.23	4.42	4.12

The MPGM pin programs a current that when multiplied by an internal 10k resistor sets up the 0.6V reference ± offset for margining. A 1.18V reference divided by the R_{PGM} resistor on the MPGM pin programs the current. Calculate $V_{OUT(MARGIN)}$:

$$V_{OUT(MARGIN)} = \frac{\%V_{OUT}}{100} \bullet V_{OUT}$$

Where $\%V_{OUT}$ is the percentage of V_{OUT} to be margined, and $V_{OUT(MARGIN)}$ is the margin quantity in volts:

$$R_{PGM} = \frac{V_{OUT}}{0.6V} \bullet \frac{1.18V}{V_{OUT(MARGIN)}} \bullet 10k$$

Where R_{PGM} is the resistor value to place on the MPGM pin to ground.

The output margining will be ± margining of the value. This is controlled by the MARG0 and MARG1 pins. See the truth table below:

MARG1	MARG0	MODE
LOW	LOW	NO MARGIN
LOW	HIGH	MARGIN UP
HIGH	LOW	MARGIN DOWN
HIGH	HIGH	NO MARGIN

Parallel Operation

The LTM4613 device is an inherently current mode controlled device. This allows the paralleled modules to have very good current sharing and balanced thermal on the design. Figure 21 shows a schematic of the parallel design. The voltage feedback equation changes with the variable N as modules are paralleled. The equation:

$$R_{FB} = \frac{\frac{100k}{N}}{\frac{V_{OUT}}{0.6V} - 1}$$

where N is the number of paralleled modules.

Operating Frequency

The operating frequency of the LTM4613 is optimized to achieve the compact package size and the minimum output ripple voltage while still keeping high efficiency. As shown in Figure 2, the frequency is linearly increased with larger output voltages to keep the low output current ripple. Figure 3 shows the inductor current ripple ΔI with different output voltages. In most applications, no additional frequency adjusting is required.

If lower output ripple is required, the operating frequency f can be increased by adding a resistor R_{fSET} between f_{SET} pin and SGND, as shown in Figure 19.

$$f = \frac{V_{OUT}}{1.5 \bullet 10^{-10} (R_{fSET} \| 133k)}$$

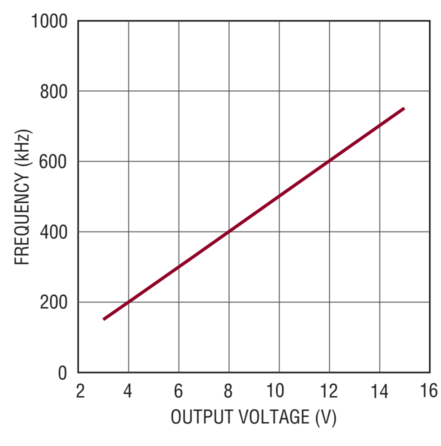


Figure 2. Operating Frequency vs Output Voltage

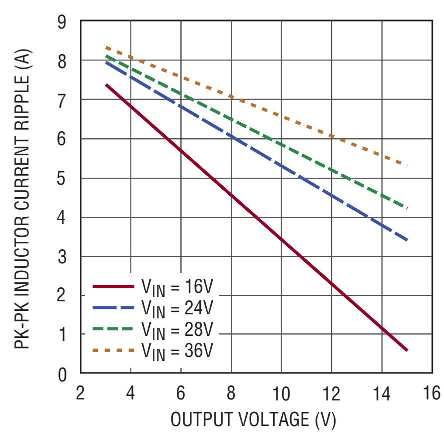


Figure 3. Pk-Pk Inductor Current Ripple vs Output Voltage

APPLICATIONS INFORMATION

For output voltages more than 12V, the frequency can be higher than 600kHz, thus reducing the efficiency significantly. Additionally, the minimum off time 400ns normally limits the operation when the input voltage is close to the output voltage. Therefore, it is recommended to lower the frequency in these conditions by connecting a resistor (R_{fSET}) from the f_{SET} pin to V_{IN}, as shown in Figure 20.

$$f = \frac{V_{OUT}}{5 \bullet 10^{-11} \left(\frac{3 \bullet R_{fSET} \bullet 133k}{R_{fSET} - 2 \bullet 133k} \right)}$$

The load current can affect the frequency due to its constant on-time control. If constant frequency is a necessity, the PLLIN pin can be used to synchronize the frequency of the LTM4613 to an external clock subject to minimum on-time and off-time limits, as shown in Figures 21 to 23.

Input Capacitors

LTM4613 is designed to achieve the low input conducted EMI noise due to the fast switching of turn-on and turn-off. Additionally, a high-frequency inductor is integrated into the input line for noise attenuation. V_D and V_{IN} pins are available for external input capacitors to form a high frequency π filter. As shown in Figure 18, the ceramic capacitors, C1-C3, on the V_D pins is used to handle most of the RMS current into the converter, so careful attention is needed for capacitors C1-C3 selection.

For a buck converter, the switching duty cycle can be estimated as:

$$D = \frac{V_{OUT}}{V_{IN}}$$

Without considering the inductor current ripple, the RMS current of the input capacitor can be estimated as:

$$I_{CIN(RMS)} = \frac{I_{OUT(MAX)}}{\eta} \bullet \sqrt{D \bullet (1 - D)}$$

In this equation, η is the estimated efficiency of the power module. Note the capacitor ripple current ratings are often based on temperature and hours of life. This makes it advisable to properly derate the input capacitor, or choose a capacitor rated at a higher temperature than required. Always contact the capacitor manufacturer for derating requirements.

In a typical 8A output application, three very low ESR, X5R or X7R, 10µF ceramic capacitors are recommended for C1-C3. This decoupling capacitance should be placed directly adjacent to the module V_D pins in the PCB layout to minimize the trace inductance and high frequency AC noise. Each 10µF ceramic is typically good for 2A of RMS ripple current. Refer to your ceramics capacitor catalog for the RMS current ratings.

To attenuate the high frequency noise, extra input capacitors should be connected to the V_{IN} pads and placed before the high frequency inductor to form the π filter. One of these low ESR ceramic input capacitors is recommended to be close to the connection into the system board. A large bulk 100µF capacitor is only needed if the input source impedance is compromised by long inductive leads or traces.

Output Capacitors

The LTM4613 is designed for low output voltage ripple. The bulk output capacitors defined as C_{OUT} are chosen with low enough effective series resistance (ESR) to meet the output voltage ripple and transient requirements. C_{OUT} can be low ESR tantalum capacitor, low ESR polymer capacitor or ceramic capacitor. The typical capacitance is 4 × 47µF if all ceramic output capacitors are used. Additional output filtering may be required by the system designer, if further reduction of output ripple or dynamic transient spike is required. Table 2 shows a matrix of different output voltages and output capacitors to minimize the voltage droop and overshoot during a 4A load transient. The table optimizes total equivalent ESR and total bulk capacitance to maximize transient performance.

Multiphase operation with multiple LTM4613 devices in parallel will also lower the effective output ripple current due to the phase interleaving operation. Refer to Figure 4 for the normalized output ripple current versus the duty cycle. Figure 4 provides a ratio of peak-to-peak output ripple current to the inductor ripple current as functions of duty cycle and the number of paralleled phases. Pick the corresponding duty cycle and the number of phases to get the correct output ripple current value. For example, each phase's inductor ripple current ΔI_L is ~5.0A for a 36V

APPLICATIONS INFORMATION

Table 2. Output Voltage Response Versus Component Matrix (Refer to Figure 19)

TYPICAL MEASURED VALUES

VENDORS	PART NUMBER	VENDORS	PART NUMBER
Murata	GRM32ER61C476KEI5L (47µF, 16V)	Murata	GRM32ER71H106K (10µF, 50V)
Murata	GRM32ER61C226KE20L (22µF, 16V)	TDK	C3225X5RIC226M (22µF, 16V)

V_{OUT} (V)	C_{IN} (CERAMIC)	C_{IN} (BULK)	C_{OUT1} (CERAMIC)	C_{OUT2} (BULK)	V_{IN} (V)	DROOP (mV)	PK-TO-PK (mV)	RECOVERY TIME (µs)	LOAD STEP (A)	LOAD STEP SLEW RATE (A/µS)	R_{FB} (kΩ)
3.3	2 × 10µF 50V	100µF 50V	2 × 22uF 16V	150µF 16V	5	84	175	50	4	10	22.1
3.3	2 × 10µF 50V	100µF 50V	4 × 47uF 16V	None	5	91	181	40	4	10	22.1
3.3	2 × 10µF 50V	100µF 50V	2 × 22uF 16V	150µF 16V	12	100	188	50	4	10	22.1
3.3	2 × 10µF 50V	100µF 50V	4 × 47uF 16V	None	12	100	191	40	4	10	22.1
3.3	2 × 10µF 50V	100µF 50V	2 × 22uF 16V	150µF 16V	24	113	200	50	4	10	22.1
3.3	2 × 10µF 50V	100µF 50V	4 × 47uF 16V	None	24	103	197	40	4	10	22.1
5	2 × 10µF 50V	100µF 50V	2 × 22uF 16V	150µF 16V	12	109	222	60	4	10	13.7
5	2 × 10µF 50V	100µF 50V	4 × 47uF 16V	None	12	122	238	50	4	10	13.7
5	2 × 10µF 50V	100µF 50V	2 × 22uF 16V	150µF 16V	24	119	228	60	4	10	13.7
5	2 × 10µF 50V	100µF 50V	4 × 47uF 16V	None	24	122	238	50	4	10	13.7
5	2 × 10µF 50V	100µF 50V	2 × 22uF 16V	150µF 16V	36	125	231	60	4	10	13.7
5	2 × 10µF 50V	100µF 50V	4 × 47uF 16V	None	36	128	247	50	4	10	13.7
12	2 × 10µF 50V	100µF 50V	2 × 22uF 16V	150µF 16V	24	178	363	150	4	10	5.23
12	2 × 10µF 50V	100µF 50V	4 × 47uF 16V	None	24	238	488	90	4	10	5.23
12	2 × 10µF 50V	100µF 50V	2 × 22uF 16V	150µF 16V	36	181	369	150	4	10	5.23
12	2 × 10µF 50V	100µF 50V	4 × 47uF 16V	None	36	244	500	90	4	10	5.23

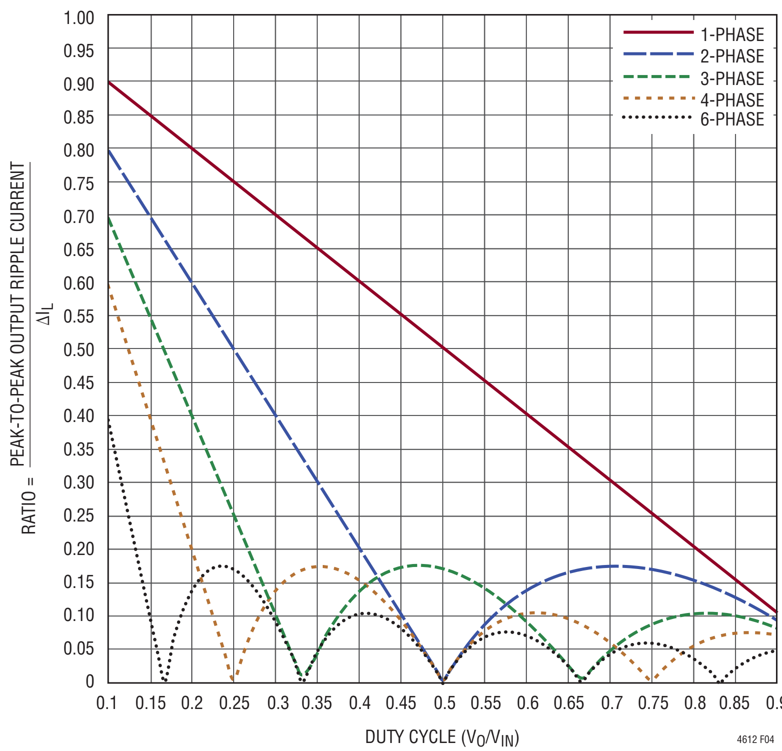


Figure 4. Normalized Output Ripple Current vs Duty Cycle, $\Delta I_L = V_O T / L_I$

APPLICATIONS INFORMATION

to 12V design. The duty cycle is about 0.33. The 2-phase curve shows a ratio of ~0.33 for a duty cycle of 0.33. This 0.33 ratio of output ripple current to the inductor ripple current ΔI_L at 5.0A equals 1.65A of the output ripple current (ΔI_O).

The output voltage ripple has two components that are related to the amount of bulk capacitance and effective series resistance (ESR) of the output bulk capacitance. The equation is:

$$\Delta V_{OUT(P-P)} \approx \left(\frac{\Delta I_O}{8 \cdot f \cdot N \cdot C_{OUT}}\right) + \frac{ESR \cdot \Delta I_O}{N}$$

Where f is the frequency and N is the number of paralleled phases.

Fault Conditions: Current Limit and Overcurrent Foldback

LTM4613 has a current mode controller, which inherently limits the cycle-by-cycle inductor current not only in steady state operation, but also in transient.

To further limit current in the event of an overload condition, the LTM4613 provides foldback current limiting. If the output voltage falls by more than 50%, then the maximum output current is progressively lowered to about one sixth of its full current limit value.

Soft-Start and Tracking

The TRACK/SS pin provides a means to either soft-start the regulator or track it to a different power supply. A capacitor on this pin will program the ramp rate of the output voltage. A 1.5μA current source will charge up the external soft-start capacitor to 80% of the 0.6V internal voltage reference plus or minus any margin delta. This will control the ramp of the internal reference and the output voltage. The total soft-start time can be calculated as:

$$t_{SOFTSTART} \cong 0.8 \cdot (0.6 \pm 0.6 \cdot V_{OUT}\ \text{Margin}\ \%) \cdot \frac{C_{SS}}{1.5\mu A}$$

If the RUN pin falls below 2.5V, then the soft-start pin is reset to allow for the proper soft-start again. Current foldback and force continuous mode are disabled during the soft-start process. The soft-start function can also be used to control the output ramp rising time, so that another regulator can be easily tracked.

Output Voltage Tracking

Output voltage tracking can be programmed externally using the TRACK/SS pin. The output can be tracked up and down with another regulator. Figure 5 shows an example of coincident tracking where the master regulator's output is divided down with an external resistor divider that is the same as the slave regulator's feedback divider. Ratiometric modes of tracking can be achieved by selecting different resistor values to change the output tracking ratio. The master output must be greater than the slave output

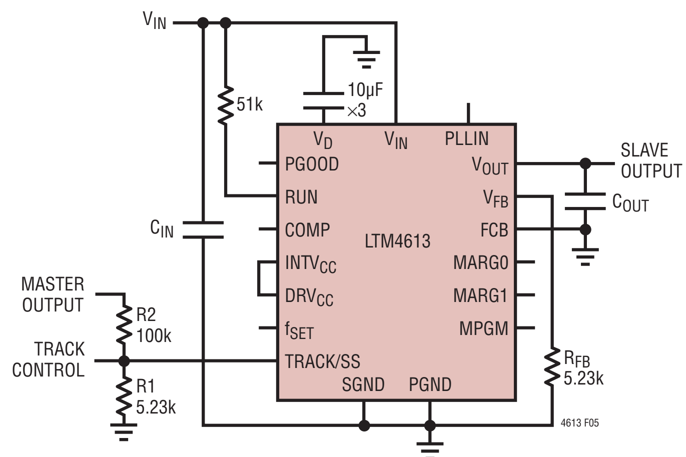


Figure 5. Coincident Tracking

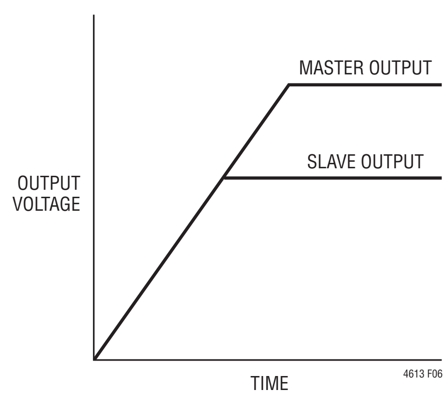


Figure 6. Coincident Output Tracking

APPLICATIONS INFORMATION

for the tracking to work. Figure 6 shows the coincident output tracking.

Ratiometric tracking can be achieved by a few simple calculations and the slew rate value applied to the master's TRACK pin. The TRACK pin has a control range from 0 to 0.6V. The master's TRACK pin slew rate is directly equal to the master's output slew rate in Volts/Time. The equation:

$$\frac{MR}{SR}\bullet 100k = R2$$

where MR is the master's output slew rate and SR is the slave's output slew rate in Volts/Time. When coincident tracking is desired, then MR and SR are equal, thus R2 is equal the 100k. R_{TA} is derived from equation:

$$R1 = \frac{0.6V}{\frac{V_{FB}}{100k} + \frac{V_{FB}}{R_{FB}} - \frac{V_{TRACK}}{R2}}$$

where V_{FB} is the feedback voltage reference of the regulator, and V_{TRACK} is 0.6V. Since R2 is equal to the 100k top feedback resistor of the slave regulator in equal slew rate or coincident tracking, then R1 is equal to R_{FB} with V_{FB} = V_{TRACK}. Therefore R2 = 100k, and R1 = 5.23k in Figure 5.

In ratiometric tracking, a different slew rate maybe desired for the slave regulator. R2 can be solved for when SR is slower than MR. Make sure that the slave supply slew rate is chosen to be fast enough so that the slave output voltage will reach it final value before the master output.

For example, MR = 1.5V/1ms, and SR = 1.2V/1ms. Then R2 = 125k. Solve for R1 to equal to 5.18k.

Each of the TRACK pins will have the 1.5μA current source on when a resistive divider is used to implement tracking on that specific channel. This will impose an offset on the TRACK pin input. Smaller values resistors with the same ratios as the resistor values calculated from the above equation can be used. For example, where the 100k is used then a 10k can be used to reduce the TRACK pin offset to a negligible value.

RUN Enable

The RUN pin is used to enable the power module. The pin has an internal 5.1V Zener to ground. The pin can be driven with 5V logic levels.

The RUN pin can also be used as an undervoltage lockout (UVLO) function by connecting a resistor divider from the input supply to the RUN pin. The equation for UVLO threshold:

$$V_{UVLO} = \frac{R_A + R_B}{R_B}\bullet 1.5V$$

where R_A is the top resistor, and R_B is the bottom resistor.

Power Good

The PGOOD pin is an open-drain pin that can be used to monitor valid output voltage regulation. This pin monitors a ±10% window around the regulation point, and tracks with margining.

COMP Pin

The pin is the external compensation pin. The module has already been internally compensated for most output voltages. Linear Technology provides LTpowerCAD™ for more control loop optimization.

FCB Pin

The FCB pin determines whether the bottom MOSFET remains on when current reverses in the inductor. Tying this pin above its 0.6V threshold enables discontinuous operation where the bottom MOSFET turns off when inductor current reverses. FCB pin below the 0.6V threshold forces continuous synchronous operation, allowing current to reverse at light loads and maintaining high frequency operation.

PLLIN Pin

The power module has a phase-locked loop comprised of an internal voltage controlled oscillator and a phase detector. This allows the internal top MOSFET turn-on to be locked to the rising edge of the external clock. The external clock frequency range must be within ±30% around the set operating frequency. A pulse detection circuit is used to detect a clock on the PLLIN pin to turn on the phase-locked loop. The pulse width of the clock has to be at least 400ns. The clock high level must be above 2V and clock

APPLICATIONS INFORMATION

low level below 0.3V. During the start-up of the regulator, the phase-locked loop function is disabled.

$INTV_{CC}$ and DRV_{CC} Connection

An internal low dropout regulator produces an internal 5V supply that powers the control circuitry and DRV_{CC} for driving the internal power MOSFETs. Therefore, if the system does not have a 5V power rail, the LTM4613 can be directly powered by V_{IN}. The gate driver current through the LDO is about 20mA. The internal LDO power dissipation can be calculated as:

$$P_{LDO\_LOSS} = 20mA \bullet (V_{IN} – 5V)$$

The LTM4613 also provides the external gate driver voltage pin DRV_{CC}. If there is a 5V rail in the system, it is recommended to connect the DRV_{CC} pin to the external 5V rail. This is especially true for higher input voltages. Do not apply more than 6V to the DRV_{CC} pin.

Radiated EMI Noise

High radiated EMI noise is a disadvantage for switching regulators by nature. Fast switching turn-on and turn-off make the large di/dt change in the converters, which act as the radiation sources in most systems. LTM4613 integrates the feature to minimize the radiated EMI noise to meet the most applications with low noise requirements. An optimized gate driver for the MOSFET and a noise cancellation network are installed inside the LTM4613 to achieve the low radiated EMI noise. Figure 7 shows a typical example for the LTM4613 to meet the EN55022 Class B radiated emission limit.

Thermal Considerations and Output Current Derating

In different applications, LTM4613 operates in a variety of thermal environments. The maximum output current is limited by the environment thermal condition. Sufficient cooling should be provided to help ensure reliable operation. When the cooling is limited, proper output current derating is necessary, considering ambient temperature, airflow, input/output condition, and the need for increased reliability.

The thermal resistances reported in the Pin Configuration section of the data sheet are consistent with those parameters defined by JESD51-9. They are intended for use with finite element analysis (FEA) software modeling tools that leverage the outcome of thermal modeling, simulation and correlation to hardware evaluation performed on a µModule package mounted to a hardware test board. This is also defined by JESD51-9, "Test Boards for Area Array Surface Mount Package Thermal Measurements." The motivation for providing these thermal coefficients in found in JESD51-12, "Guidelines for Reporting and Using Electronic Package Thermal Information."

Many designers may opt to use laboratory equipment

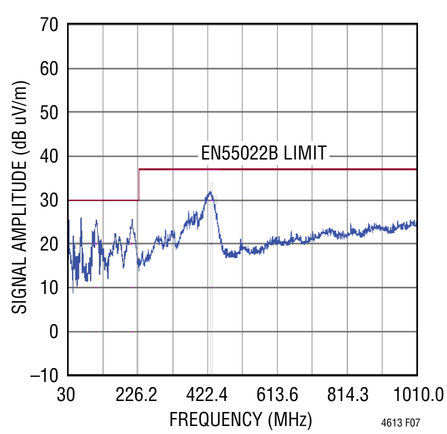


Figure 7. Radiated Emission Scan with $24V_{IN}$ to $12V_{OUT}$ at 8A Measured in 10 Meter Chamber

APPLICATIONS INFORMATION

and a test vehicle, such as the demo board, to anticipate the μModule regulator's thermal performance in their application at various electrical and environmental operating conditions to compliment any FEA activities. Without FEA software, the thermal resistances reported in the Pin Configuration section are in and of themselves not relevant to providing guidance of thermal performance. Instead, the derating curves provided in the data sheet can be used in a manner that yields insight and guidance pertaining to one's application usage, and can be adapted to correlate thermal performance to one's own application.

The Pin Configuration section of the data sheet typically gives four thermal coefficients, explicitly defined in JESD51-12. These coefficients are quoted or paraphrased below:

- θ_{JA}, the thermal resistance from junction-to-ambient, is the natural convection junction-to-ambient air thermal resistance measured in a one cubic foot sealed enclosure. This environment is sometimes referred to as "still air" although natural convection causes the air to move. This value is determined with the part mounted to a JESD51-9 defined test board, which does not reflect an actual application or viable operating condition.
- $\theta_{JCbottom}$, the thermal resistance from the junction to the bottom of the product case, is the junction-to-board thermal resistance with all of the component power dissipation flowing through the bottom of the package. In the typical μModule regulator, the bulk of the heat flows out of the bottom of the package, but there is always heat flow out into the ambient environment. As a result, this thermal resistance value may be useful for comparing packages, but the test conditions do not generally match the user's application.
- θ_{JCtop}, the thermal resistance from the junction to the top of the product case, is determined with nearly all of the component power dissipation flowing through the top of the package. As the electrical connections of the μModule regulator are on the bottom of the package, it is rare for an application to operate such that most of the heat flows from the junction to the top of the part. As in the case of $\theta_{JCbottom}$, this value may be useful for comparing packages, but the test conditions do not generally match the user's application.
- θ_{JB}, the thermal resistance from the junction to the printed circuit board, is the junction-to-board thermal resistance where almost all of the heat flows through the bottom of the μModule regulator and into the board. It is really the sum of the $\theta_{JCbottom}$ and the thermal resistance of the bottom of the part through the solder joints and through a portion of the board. The board temperature is measured a specified distance from the package, using a two-sided, two-layer board. This board is described in JESD51-9.

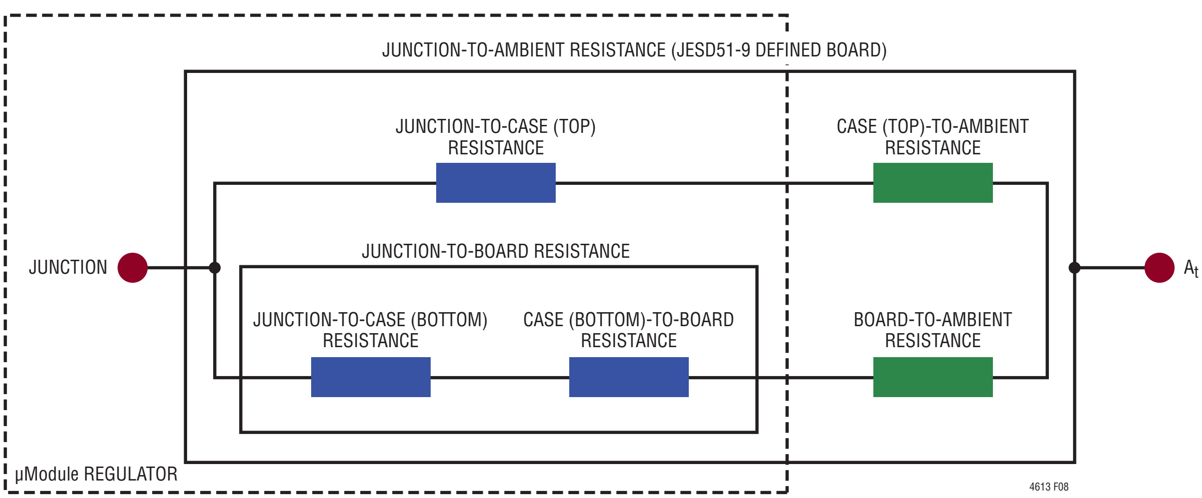


Figure 8. Graphical Representation of JESD51-12 Thermal Coefficients

APPLICATIONS INFORMATION

A graphical representation of the aforementioned thermal resistances is given in Figure 8. Blue resistances are contained within the µModule package, whereas green resistances are external to the µModule package.

As a practical matter, it should be clear to the reader that no individual or sub group of the four thermal resistance parameters defined by JESD51-12, or provided in the Pin Configuration section, replicates or conveys normal operating conditions of a µModule regulator. For example, in normal board-mounted applications, never does 100% of the device's total power loss (heat) thermally conduct exclusively through the top or exclusively through bottom of the package—as the standard defines for θ_{JCtop} and $\theta_{JCbottom}$, respectively. In practice, power loss is thermally dissipated in both directions away from the package. Granted, in the absence of a heat sink and airflow, the majority of the heat flow is into the board.

Within a SIP (System-In-Package) module, be aware that there are multiple power devices and components dissipating power, with a consequence that the thermal resistances relative to different junctions of components or die are not exactly linear with respect to total package power loss. To reconcile this complication without sacrificing modeling simplicity—but also, not ignoring practical realities—an approach has been taken using FEA software modeling along with laboratory testing in a controlled environment chamber to reasonably define and correlate the thermal resistance values supplied in this data sheet:

1. Initially, FEA software is used to accurately build the mechanical geometry of the µModule regulator and the specified PCB with all of the correct material coefficients, along with accurate power loss source definitions;
2. This model simulates a software-defined JEDEC environment consistent with JSED51-9 to predict power loss heat flow and temperature readings at different interfaces that enable the calculation of the JEDEC-defined thermal resistance values;
3. The model and FEA software is used to evaluate the µModule regulator with heat sinks and airflow;
4. Having solved for, and analyzed these thermal resistance values and simulated various operating conditions in the software model, a thorough laboratory evaluation replicates the simulated conditions with thermocouples within a controlled environment chamber while operating the device at the same power loss as that which was simulated.

An outcome of this process and due diligence yields a set of derating curves provided in other sections of this data sheet. After these laboratory tests have been performed and correlated to the µModule regulator model, the θ_{JB} and θ_{JA} are summed together to correlate quite well with the µModule regulator model, with no airflow or heat sinking, in a properly defined chamber. This $\theta_{JB} + \theta_{JA}$ value is shown in the Pin Configuration section, and should accurately equal the θ_{JA} value in this section, because approximately 100% of power loss flows from the junction through the board into ambient with no airflow or top mounted heat sink.

The power loss curves in Figures 9 and 10 can be used in coordination with the load current derating curves in Figures 11 to 16 for calculating an approximate θ_{JA} for the module. Each figure has three curves that are taken at three different airflow conditions. Graph designation delineates between no heat sink, and a BGA heat sink. Each of the load current derating curves will lower the maximum load current as a function of the increased ambient temperature to keep the maximum junction temperature of the power module at 125°C maximum. This will maintain the maximum operating temperature below 125°C. Table 3 provides the approximate θ_{JA} for Figures 11 to 16. A complete explanation of the thermal characteristics is provided in the thermal application note, AN110.

APPLICATIONS INFORMATION

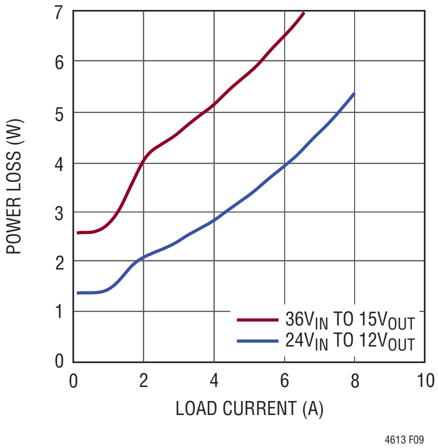


Figure 9. Power Loss at $12V_{OUT}$ and $15V_{OUT}$

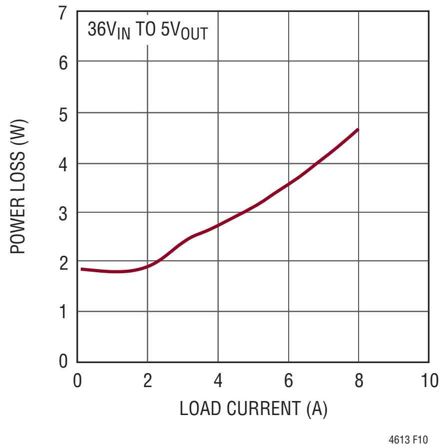


Figure 10. Power Loss at $5V_{OUT}$

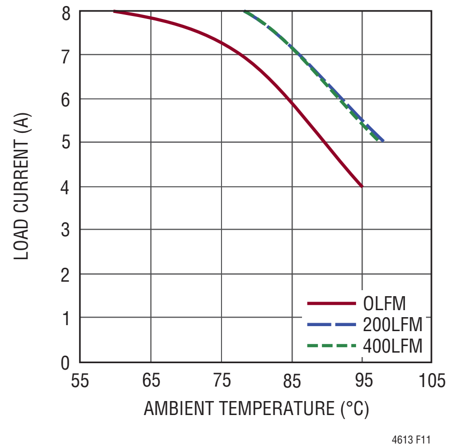


Figure 11. No Heat Sink with $36V_{IN}$ to $5V_{OUT}$

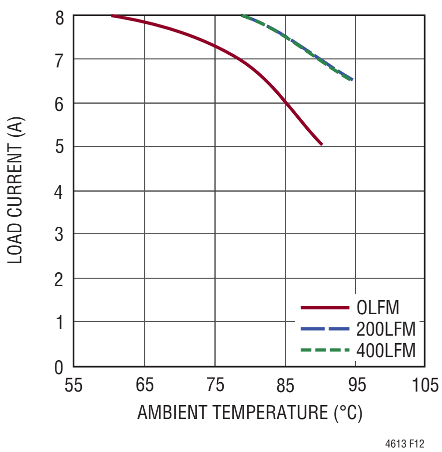


Figure 12. BGA Heat Sink with $36V_{IN}$ to $5V_{OUT}$

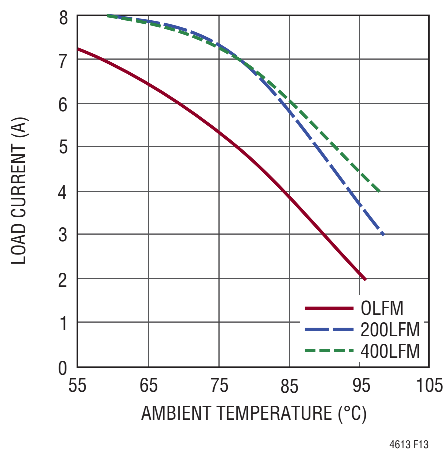


Figure 13. No Heat Sink with $24V_{IN}$ to $12V_{OUT}$

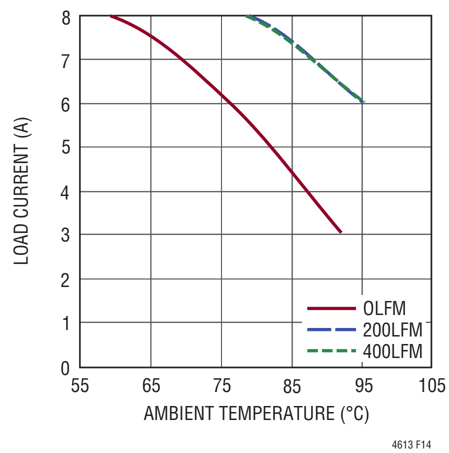


Figure 14. BGA Heat Sink with $24V_{IN}$ to $12V_{OUT}$

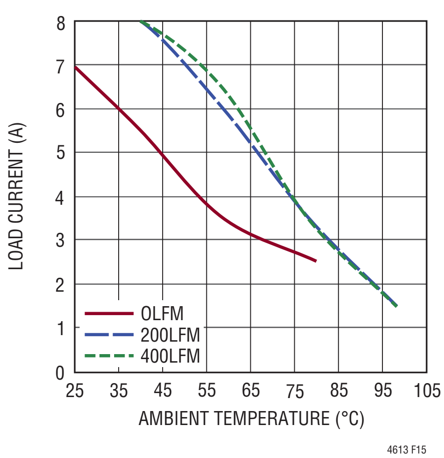


Figure 15. No Heat Sink with $36V_{IN}$ to $15V_{OUT}$

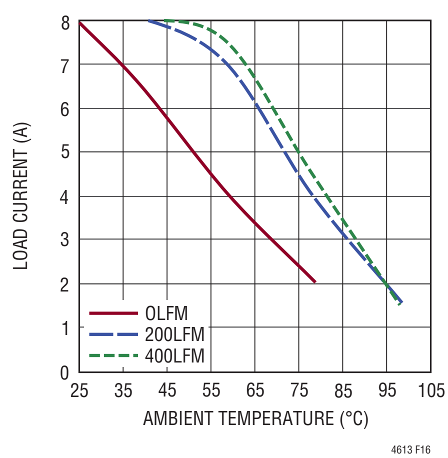


Figure 16. BGA Heat Sink with $36V_{IN}$ to $15V_{OUT}$

APPLICATIONS INFORMATION

Table 3. 12V and 15V Outputs

DERATING CURVE	V_{IN} (V)	POWER LOSS CURVE	AIRFLOW (LFM)	HEAT SINK	θ_{JA} (°C/W)
Figures 13, 15	24, 36	Figure 9	0	None	≈14
Figures 13, 15	24, 36	Figure 9	200	None	≈10
Figures 13, 15	24, 36	Figure 9	400	None	≈10
Figures 14, 16	24, 36	Figure 9	0	BGA Heat Sink	≈13
Figures 14, 16	24, 36	Figure 9	200	BGA Heat Sink	≈8
Figures 14, 16	24, 36	Figure 9	400	BGA Heat Sink	≈8

Table 4. 5V Output

DERATING CURVE	V_{IN} (V)	POWER LOSS CURVE	AIRFLOW (LFM)	HEAT SINK	θ_{JA} (°C/W)
Figure 11	36	Figure 10	0	None	≈11
Figure 11	36	Figure 10	200	None	≈9
Figure 11	36	Figure 10	400	None	≈9
Figure 12	36	Figure 10	0	BGA Heat Sink	≈11
Figure 12	36	Figure 10	200	BGA Heat Sink	≈8.5
Figure 12	36	Figure 10	400	BGA Heat Sink	≈8.5

Heat Sink Manufacturer

Wakefield Engineering	Part No: LTN20069	Phone: 603-635-2800

Safety Considerations

The LTM4613 modules do not provide isolation from V_{IN} to V_{OUT}. There is no internal fuse. If required, a slow blow fuse with a rating twice the maximum input current needs to be provided to protect each unit from catastrophic failure.

Layout Checklist/Example

The high integration of LTM4613 makes the PCB board layout very simple and easy. However, to optimize its electrical and thermal performance, some layout considerations are still necessary.

- Use large PCB copper areas for high current path, including V_{IN}, PGND and V_{OUT}. It helps to minimize the PCB conduction loss and thermal stress.
- Place high frequency ceramic input and output capacitors next to the V_D, PGND and V_{OUT} pins to minimize high frequency noise.
- Place a dedicated power ground layer underneath the unit.
- Use round corners for the PCB copper layer to minimize the radiated noise.
- To minimize the EMI noise and reduce module thermal stress, use multiple vias for interconnection between top layer and other power layers.
- Do not put vias directly on pads.
- If vias are placed onto the pads, the the vias must be capped.
- Interstitial via placement can also be used if necessary.
- Use a separated SGND ground copper area for components connected to signal pins. Connect the SGND to PGND underneath the unit.
- Place one or more high frequency ceramic capacitors close to the connection into the system board.

Figure 17 gives a good example of the recommended layout.

APPLICATIONS INFORMATION

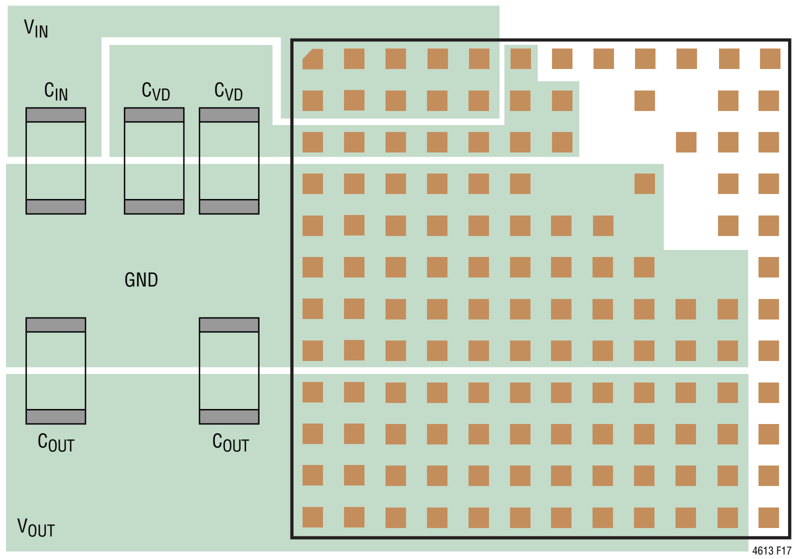


Figure 17. Recommended PCB Layout

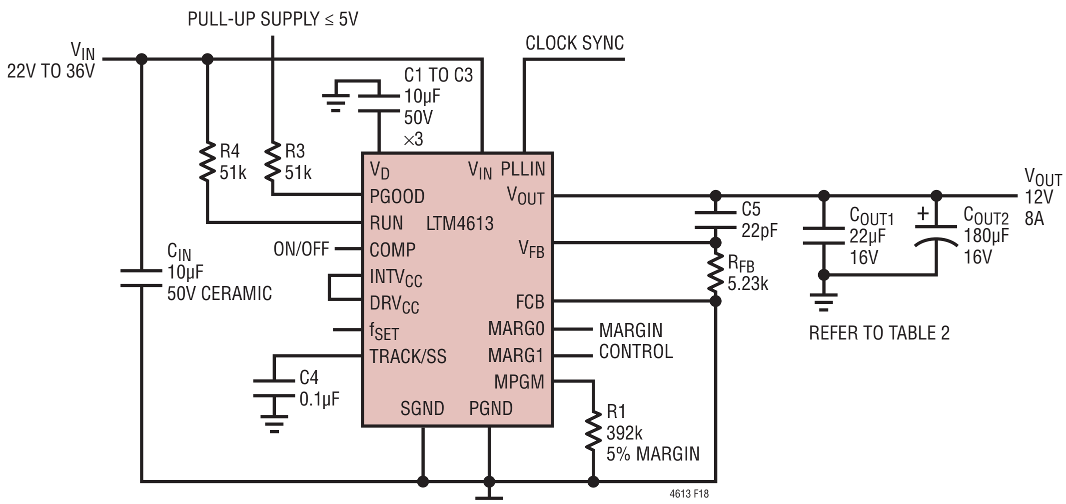


Figure 18. Typical 22V to 36V$_{IN}$, 12V at 8A Design

APPLICATIONS INFORMATION

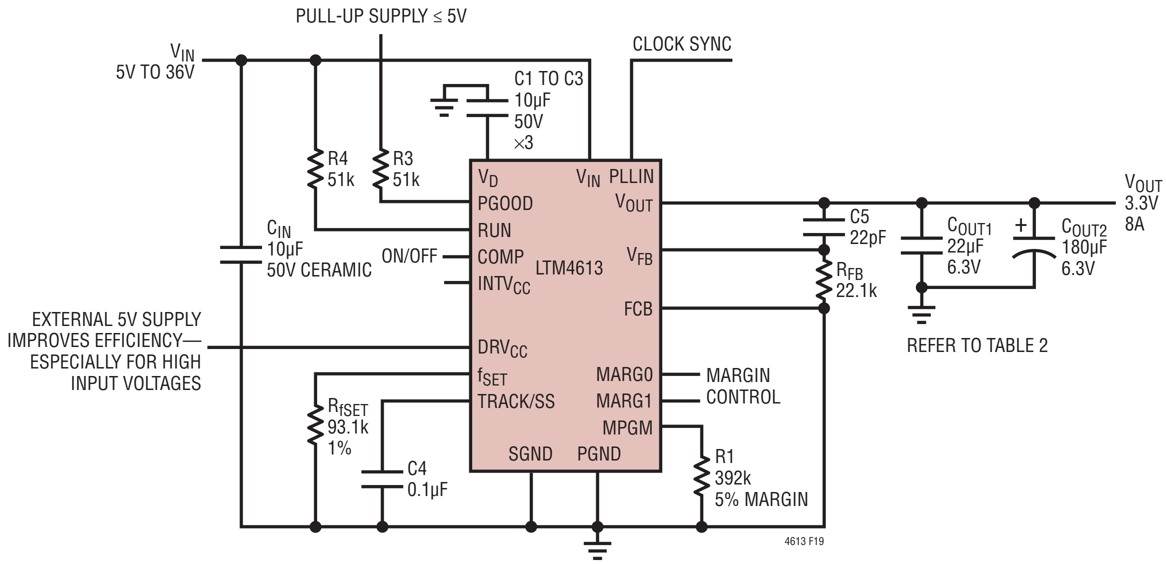


Figure 19. Typical 5V to 36V_{IN}, 3.3V at 8A Design with 400kHz Frequency

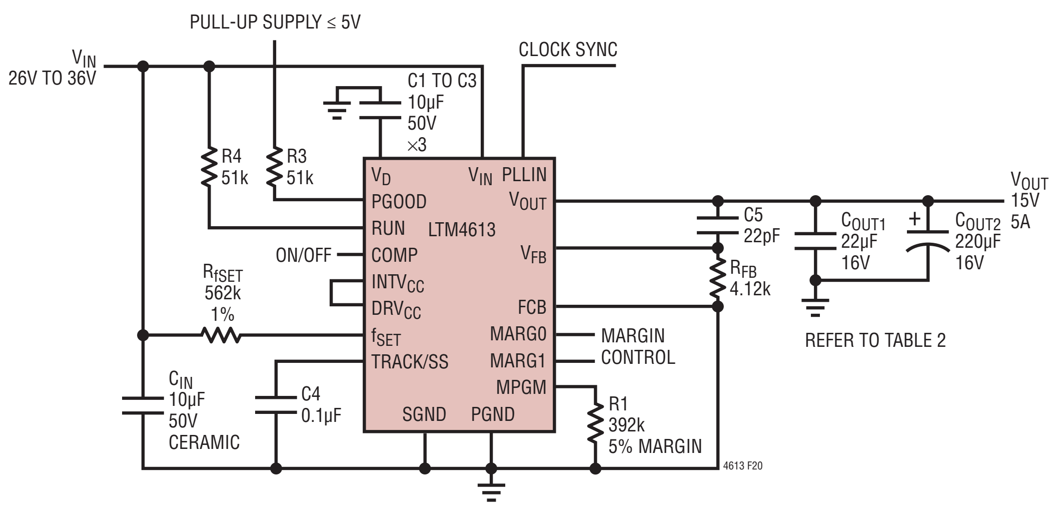


Figure 20. 26V to 36V_{IN}, 15V at 5A Design with 600kHz Frequency

APPLICATIONS INFORMATION

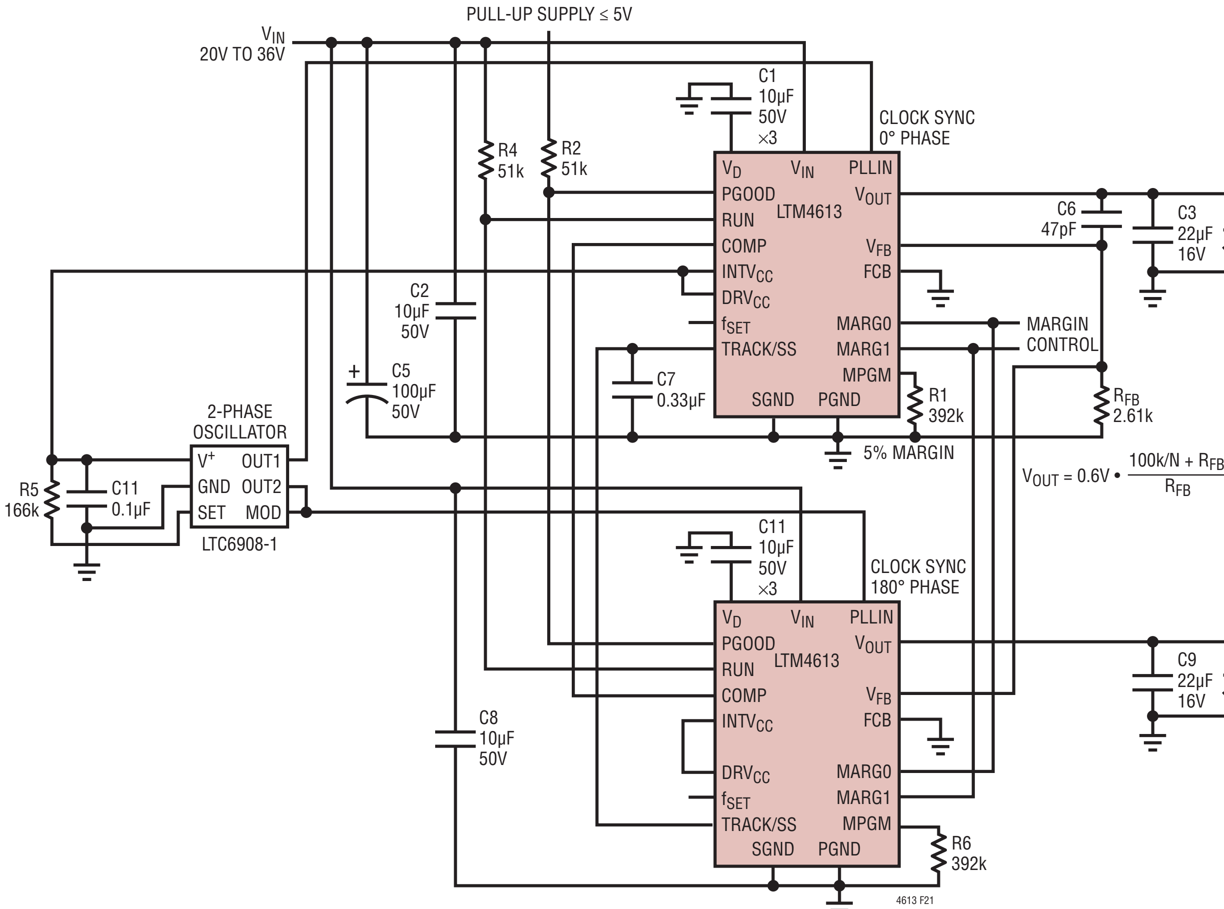


Figure 21. 2-Phase, Parallel 12V at 16A Design with 600kHz Frequency

APPLICATIONS INFORMATION

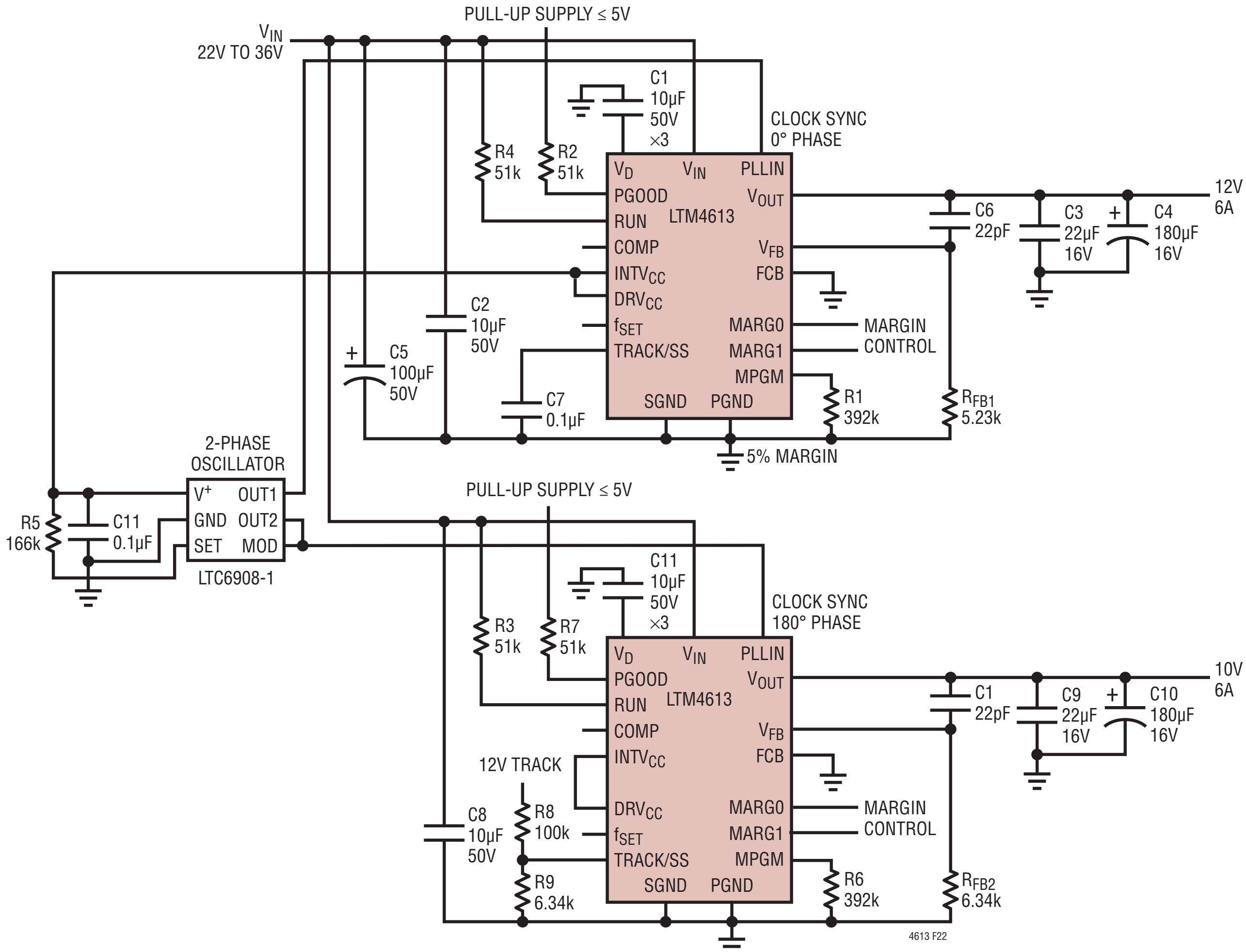


Figure 22. 2-Phase, 12V and 10V at 6A Design with 600kHz Frequency and Output Voltage Tracking

APPLICATIONS INFORMATION

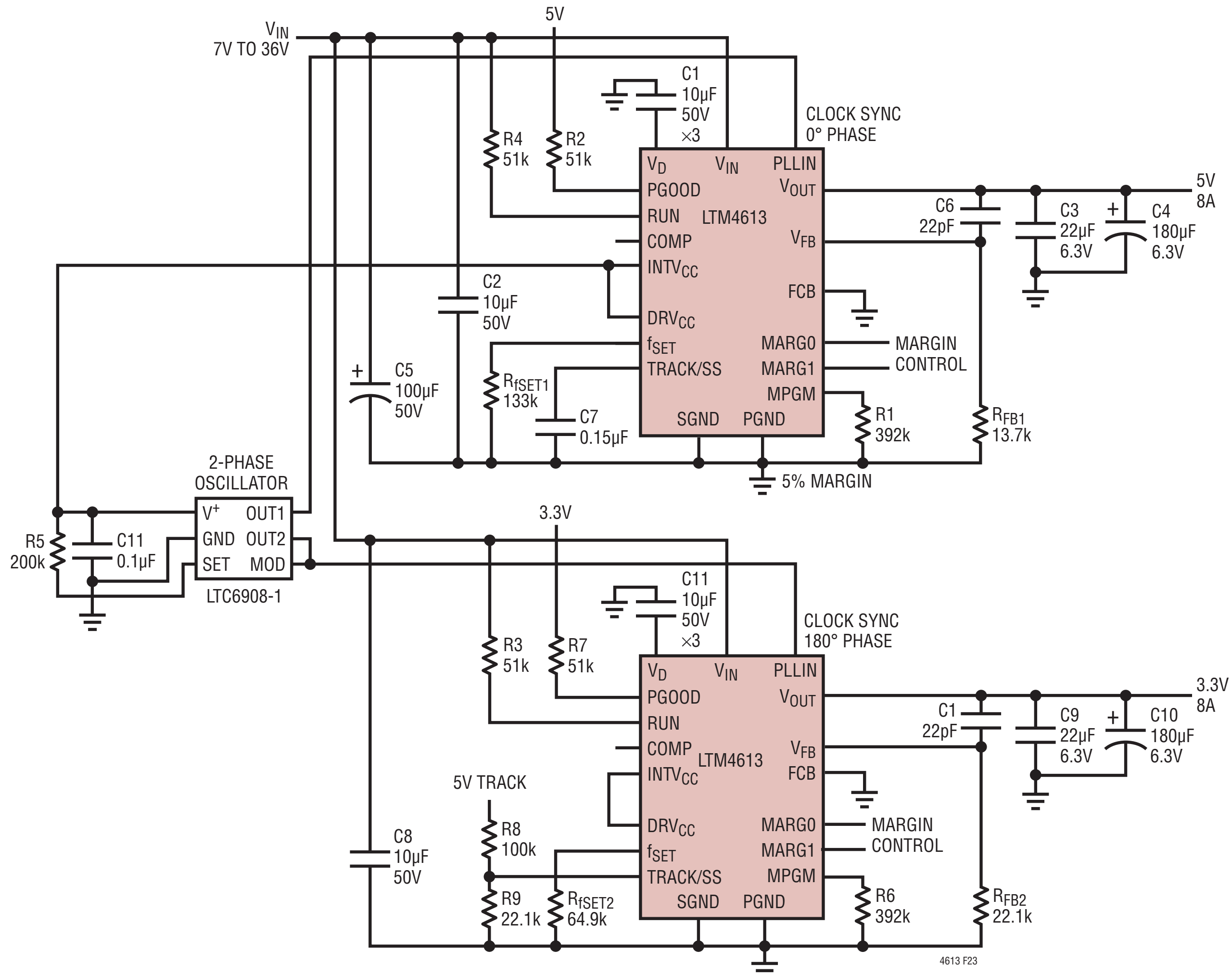


Figure 23. 2-Phase, 5V and 3.3V at 8A Design with 500kHz Frequency and Output Voltage Tracking

PACKAGE DESCRIPTION

Pin Assignment Tables
(Arranged by Pin Function)

PIN	NAME
A1	V_{IN}
A2	V_{IN}
A3	V_{IN}
A4	V_{IN}
A5	V_{IN}
B1	V_{IN}
B2	V_{IN}
B3	V_{IN}
B4	V_{IN}
B5	V_{IN}

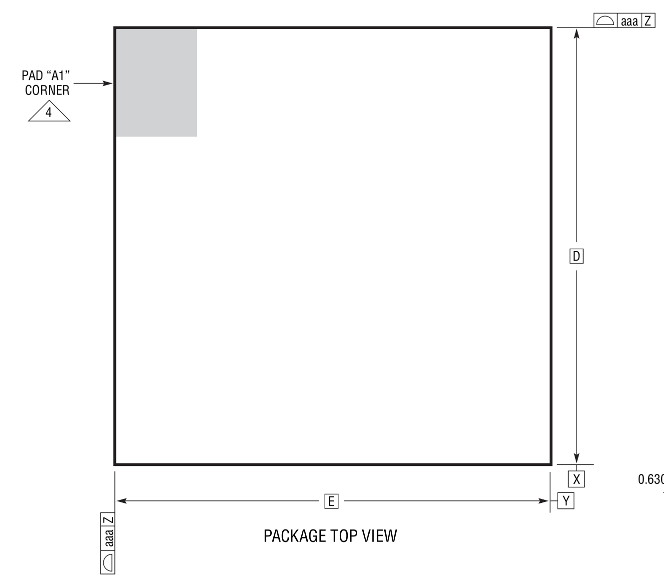
PIN	NAME
D1	PGND
D2	PGND
D3	PGND
D4	PGND
D5	PGND
D6	PGND
E1	PGND
E2	PGND
E3	PGND
E4	PGND
E5	PGND
E6	PGND
E7	PGND
E8	PGND
F1	PGND
F2	PGND
F3	PGND
F4	PGND
F5	PGND
F6	PGND
F7	PGND
F8	PGND
F9	PGND
G1	PGND
G2	PGND
G3	PGND
G4	PGND
G5	PGND
G6	PGND
G7	PGND
G8	PGND
G9	PGND
G10	PGND
G11	PGND
H1	PGND
H2	PGND
H3	PGND
H4	PGND
H5	PGND
H6	PGND
H7	PGND
H8	PGND
H9	PGND
H10	PGND
H11	PGND

PIN	NAME
J1	V_{OUT}
J2	V_{OUT}
J3	V_{OUT}
J4	V_{OUT}
J5	V_{OUT}
J6	V_{OUT}
J7	V_{OUT}
J8	V_{OUT}
J9	V_{OUT}
J10	V_{OUT}
J11	V_{OUT}
K1	V_{OUT}
K2	V_{OUT}
K3	V_{OUT}
K4	V_{OUT}
K5	V_{OUT}
K6	V_{OUT}
K7	V_{OUT}
K8	V_{OUT}
K9	V_{OUT}
K10	V_{OUT}
K11	V_{OUT}
L1	V_{OUT}
L2	V_{OUT}
L3	V_{OUT}
L4	V_{OUT}
L5	V_{OUT}
L6	V_{OUT}
L7	V_{OUT}
L8	V_{OUT}
L9	V_{OUT}
L10	V_{OUT}
L11	V_{OUT}
M1	V_{OUT}
M2	V_{OUT}
M3	V_{OUT}
M4	V_{OUT}
M5	V_{OUT}
M6	V_{OUT}
M7	V_{OUT}
M8	V_{OUT}
M9	V_{OUT}
M10	V_{OUT}
M11	V_{OUT}

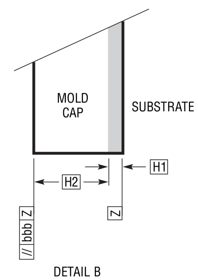
PIN	NAME
A6	V_D
A7	$INTV_{CC}$
A8	PLLIN
A9	TRACK/SS
A10	RUN
A11	COMP
A12	MPGM
B6	V_D
B7	V_D
B8	–
B9	RUN
B10	–
B11	MPGM
B12	f_{SET}
C1	V_D
C2	V_D
C3	V_D
C4	V_D
C5	V_D
C6	V_D
C7	V_D
C8	–
C9	–
C10	DRV_{CC}
C11	MARG1
C12	MARG0
D7	–
D8	–
D9	SGND
D10	–
D11	COMP
D12	MARG1
E9	–
E10	–
E11	DRV_{CC}
E12	DRV_{CC}
F10	–
F11	–
F12	V_{FB}
G12	PGOOD
H12	SGND
J12	NC
K12	NC
L12	NC
M12	FCB

PACKAGE DESCRIPTION

LGA Package
133-Lead (15mm × 15mm × 4.32mm)
(Reference LTC DWG # 05-08-1884 Rev Ø)

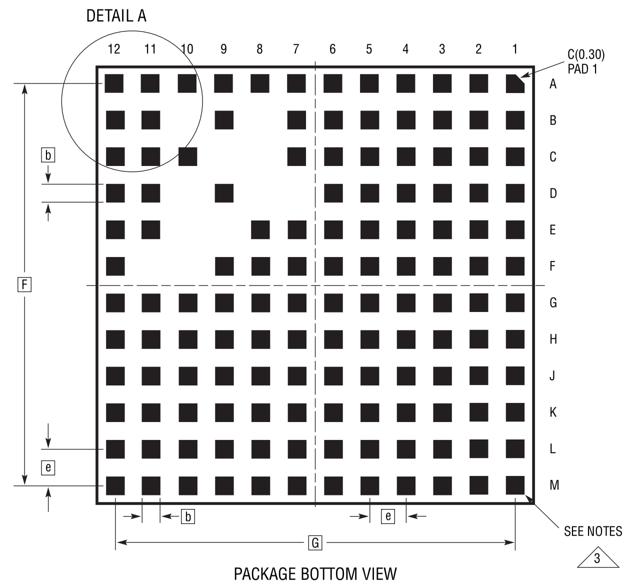


PACKAGE TOP VIEW

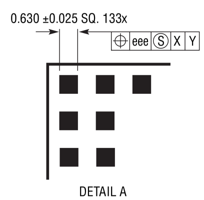


DETAIL B

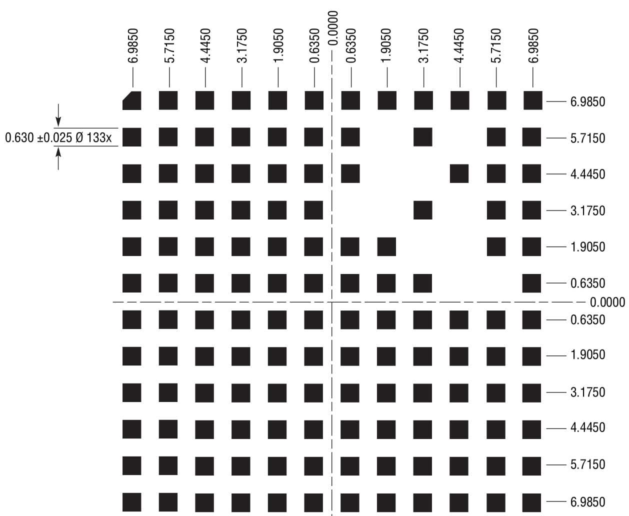
DETAIL B



PACKAGE BOTTOM VIEW



DETAIL A

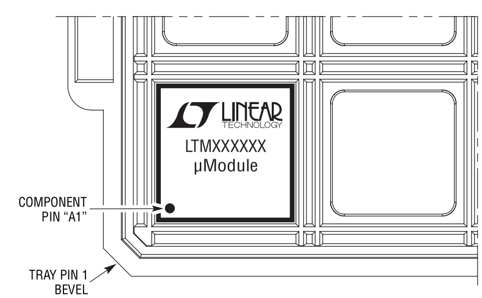


SUGGESTED PCB LAYOUT
TOP VIEW

SYMBOL	MIN	NOM	MAX	NOTES
	DIMENSIONS			
A	4.22	4.32	4.42	
b	0.60	0.63	0.66	
D		15.0		
E		15.0		
e		1.27		
F		13.97		
G		13.97		
H1	0.27	0.32	0.37	
H2	3.95	4.00	4.05	
aaa			0.15	
bbb			0.10	
eee			0.05	

TOTAL NUMBER OF LGA PADS: 133

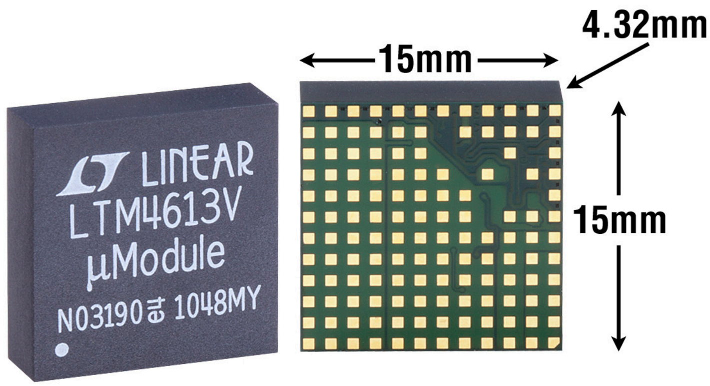
NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994
2. ALL DIMENSIONS ARE IN MILLIMETERS
3. LAND DESIGNATION PER JESD MO-222, SPP-010
4. DETAILS OF PAD #1 IDENTIFIER ARE OPTIONAL, BUT MUST BE LOCATED WITHIN THE ZONE INDICATED. THE PAD #1 IDENTIFIER MAY BE EITHER A MOLD OR MARKED FEATURE
5. PRIMARY DATUM -Z- IS SEATING PLANE
6. THE TOTAL NUMBER OF PADS: 133



PACKAGE IN TRAY LOADING ORIENTATION

LGA 133 0610 REV Ø

PACKAGE PHOTOGRAPH



RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTM4606	EN55022B Compliant 28V_{IN}, 6A DC/DC µModule Regulator	EN55022 Class B Certified with PLL, Output Tracking and Margining,
LTM4600	10A DC/DC µModule Regulator	Basic 10A DC/DC µModule Regulator, LGA Package
LTM4600HVMP	Military Plastic 10A DC/DC µModule Regulator	Guaranteed Operation from –55°C to 125°C Ambient, LGA Package
LTM4601/ LTM4601A	12A DC/DC µModule Regulator with PLL, Output Tracking/ Margining and Remote Sensing	Synchronizable, PolyPhase Operation, LTM4601-1/LTM4601A-1 Version Has No Remote Sensing, LGA Package
LTM4602	6A DC/DC µModule Regulator	Pin Compatible with the LTM4600, LGA Package
LTM4603	6A DC/DC µModule Regulator with PLL and Output Tracking/Margining and Remote Sensing	Synchronizable, PolyPhase Operation, LTM4603-1 Version Has No Remote Sensing, Pin Compatible with the LTM4601, LGA Package
LTM4604A	Low V_{IN} 4A DC/DC µModule Regulator	2.375V ≤ V_{IN} ≤ 5.5V, 0.8V ≤ V_{OUT} ≤ 5V, 9mm × 15mm × 2.3mm LGA Package
LTM4608A	Low V_{IN} 8A DC/DC µModule Regulator	2.7V ≤ V_{IN} ≤ 5.5V; 0.6V ≤ V_{OUT} ≤ 5V; 9mm × 15mm × 2.8mm LGA Package
LTM8020	High V_{IN} 0.2A DC/DC Step-Down µModule Regulator	4V ≤ V_{IN} ≤ 36V, 1.25V ≤ V_{OUT} ≤ 5V 6.25mm × 6.25mm × 2.3mm LGA Package
LTM8021	High V_{IN} 0.5A DC/DC Step-Down µModule Regulator	3V ≤ V_{IN} ≤ 36V, 0.8V ≤ V_{OUT} ≤ 5V 6.25mm × 11.25mm × 2.8mm LGA Package
LTM8022/ LTM8023	36V_{IN}, 1A and 2A DC/DC µModule Regulator	Pin Compatible; 3.6V ≤ V_{IN} ≤ 36V; 9mm × 11.25mm × 2.8mm LGA Package
LTM4612	EN55022B Compliant 36V_{IN}, 5A µModule Regulator	PLL Input, 5V ≤ V_{IN} ≤ 36V, 15mm × 15mm × 2.8mm LGA Package

Linear Technology Corporation
1630 McCarthy Blvd., Milpitas, CA 95035-7417
(408) 432-1900 ● FAX: (408) 434-0507 ● www.linear.com
LT 0411 • PRINTED IN USA