AN5107
Application note

7.5 W non-isolated buck topology, constant-current LED driver based on VIPer0P

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Introduction

The STEVAL–LLL003V1 evaluation board is a constant current LED driver, based on non–isolated buck topology using VIPer0P.

The board delivers 130 mA ± 2.5% at an output load of 15 – 21 white LEDs.

The application core is the new VIPer0P offline high voltage converter which smartly integrates an 800 V avalanche rugged power MOSFET with current-mode control.

Thanks to the embedded E/A (EAGND) floating GND, the direct current regulation can be applied to the buck converter, improving the LED current accuracy.

The evaluation board features:

- Non-isolated buck topology
- Two input voltage ranges:
  - US range: 85-135 V_{AC} (jumper J2 - closed, voltage doubler)
  - EU range: 185-275 V_{AC} (jumper J2 - open, bridge rectifier)
- 130 mA ±2.5% output constant current (15-21 white LEDs connected)
- 60 kHz fixed frequency operation
- ≅89% efficiency at maximum load
- Protections:
  - open/no-load circuit protection
  - short/overload circuit protection
  - thermal shutdown
- Soft start for improved system reliability
- Meets IEC55022 Class B conducted EMI even with reduced EMI filter, thanks to the frequency jittering feature
- Meets IEC61000-4-2(ESD), IEC61000-4-4 (Burst) and IEC61000-4-5 (Surge)
- RoHS compliant

The VIPer0P key features are:

- Embedded HV start-up
- Pulse frequency modulation (PFM) and internal circuitry ultra-low stand-by consumption
- 60 KHz fixed switching frequency with jittering
- On-board trans-conductance error amplifier internally referenced to 1.2 V±2% with separate ground to easily set a negative output
- Self-biasing option to avoid auxiliary winding and bias components
- Current mode PWM controller with drain current limit protection for easy compensation

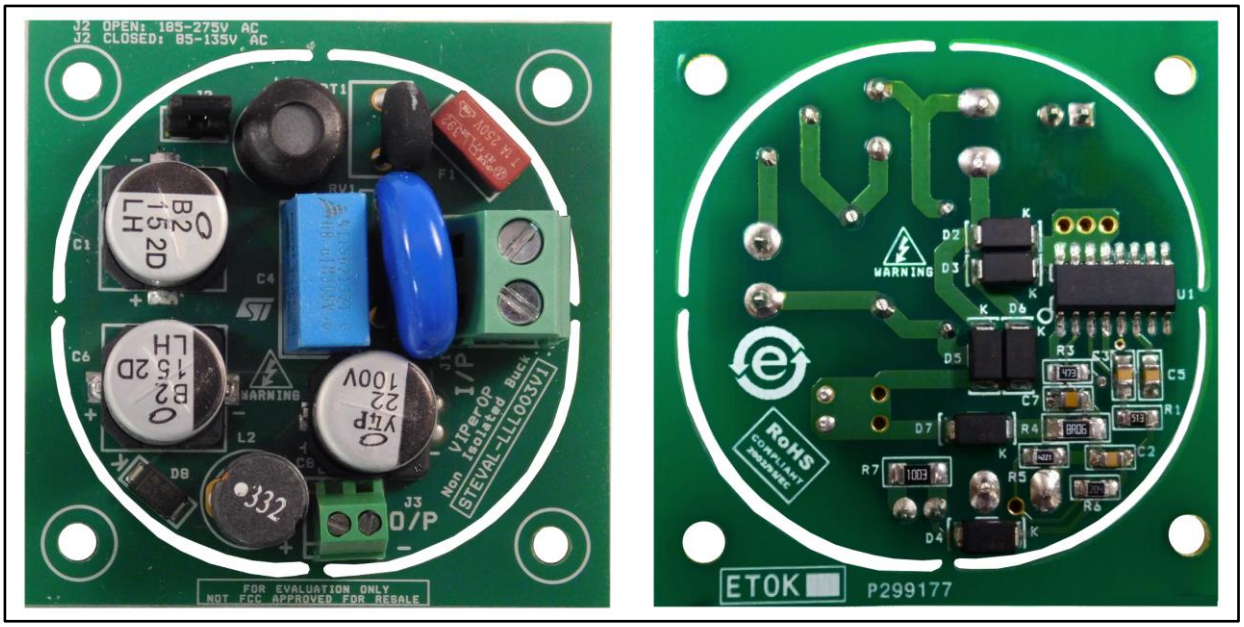
Enhanced system reliability is also ensured by the built-in soft start function and by the following set of protections:

- Pulse skip mode to avoid flux-runaway
- Delayed overload protection (OLP)

- Maximum duty cycle counter
- V_{CC} clamp
- Thermal shutdown

All the protections mentioned above have auto-restart mode, except for pulse-skip mode.

Figure 1: STEVAL-LLL003V1 evaluation board (top and bottom views)



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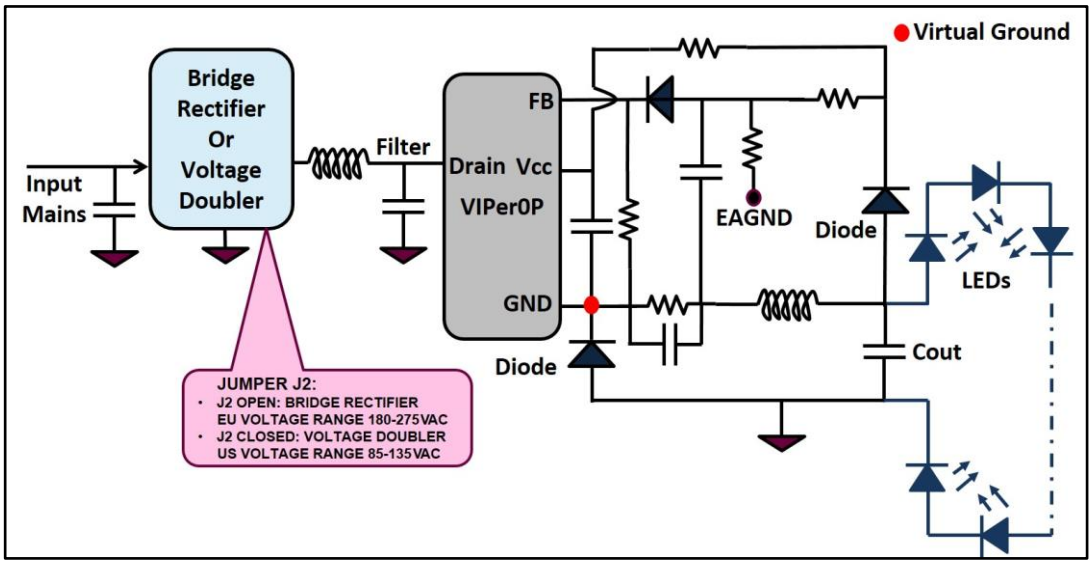
1 Board electrical specifications and block diagram

Table 1: STEVAL-LLL003V1 evaluation board electrical specifications

Parameter	Value/Range
Input voltage range	85 to 135 V_{AC} (J2 - Closed) 180 to 275 V_{AC} (J2 - Open)
Output current	130 mA ±2.5%
Load	15 to 21 white LEDs
Max. ambient operating temperature	60 °C
Fixed switching frequency	60 KHz
Maximum output power	8 W
Open/no-load circuit protection	✓
Short/overload circuit protection	✓
Thermal shutdown	✓
Soft start	✓

Figure 2: STEVAL-LLL003V1 evaluation board block diagram



The STEVAL-LLL003V1 evaluation board is a constant current LED driver. For any converter working in a continuous conduction mode (CCM), the duty cycle should be less than 50% at any given stage. In longer duty cycles (> 50%), as the error between inductor peak current and average current multiplies for successive charge/discharge cycles, inducing instability, slope compensation is needed in the control scheme.

The STEVAL-LLL003V1 evaluation board is based on VIPer0PL (zero-power off-line high voltage converter). It operates on a fixed frequency (i.e., 60 KHz) and there is an internal limit on the maximum drain current (i.e., I_{DLIM} = 400 mA).

To fulfill the requirement of 7.5 W at the output, the duty cycle exceeds > 50% at lower input mains voltages: to avoid control loop instability, the board is equipped with a voltage doubler. By changing jumper J2 position, the user can select the desired configuration and can evaluate the board at two different voltage ranges (see *jumper J2* for details).

The evaluation board can also be tuned for low power rating by changing few component values (refer to *Section 7: "Design calculations"*).[a]

Table 2: STEVAL-LLL003V1 evaluation board jumper J2: input mains voltage operating range selection

Jumper J2	Configuration	Input mains voltage range
Open	Bridge rectifier	Europe voltage range 180 – 275 V_{AC}
Closed	Voltage doubler	US voltage range 85 – 135 V_{AC}

The evaluation board input mains voltage is given by jumper J2 position.

In case jumper J2 is closed (voltage doubler configuration) and the board operates with 230 V_{AC} input mains, C1 and C6 capacitors will be damaged, leading to board failure.

[a] At low output power, the evaluation board works in wide range (85-275 V_{AC}) with normal bridge configuration.

2 Circuit description

The STEVAL-LLL003V1 LED driver is based on non-isolated buck topology. The input section includes a resistor RT1 for inrush current limiting and a filter for EMC suppression. The user can select the normal bridge rectifier or voltage doubler configuration on the basis of the operating input mains voltage.

At power-up, as V_{DRAIN} exceeds V_{HV_START}, the internal HV current generator charges the V_{CC} capacitor C3 to V_{CCon}: the Power MOSFET starts switching operation and the current generator is turned off. The IC is powered by C3. When V_{OUT} reaches its steady-state value, the IC is biased from the output resistor R1. This **external biasing** can be applied when the output voltage is high enough to keep C3 voltage above the V_{CSon} threshold (the maximum value, V_{CSon_max}, is 4.5 V).

The FB pin is the inverting input of an error amplifier and is an accurate 1.2 V voltage reference with respect to EAGND. This pin is a separate ground which can float down to -20 V with respect to the ground of the device (SGND). During normal operation, the FB pin is controlled by the voltage drop across R4. In an open circuit, the voltage loop (R6, R5 and D8) limits the output voltage at around 80 V.

The VIPer0P embeds a fixed frequency oscillator with jittering, which distributes the energy of each switching frequency harmonic over a number of frequency bands, having the same energy on the whole but smaller amplitudes. This helps to reduce the conducted emissions, especially when measured with the average detection method or, equivalently, to pass the EMI tests with an input filter smaller than the one needed in the absence of a jittering feature.

The VIPer0P embeds a pulse skip circuit:

- Each time the drain peak current exceeds I_{DLIM} level within t_{ON_MIN}, the switching cycle is skipped. The cycles can be skipped until the minimum switching frequency is reached.[a]
- Each time the drain peak current does not exceed I_{DLIM} within t_{ON_MIN}, a switching cycle is restored. The cycles can be restored until the nominal switching frequency is reached.[b]

If the converter is indefinitely operated at F_{OSC_MIN}, the VIPer0P is turned off after t_{OVL_MAX}[c] and then automatically restarted with soft-start phase, after $t_{RESTART}$[d]. The protection is intended to avoid the **flux runaway** condition often present at converter startup due to the fact that the primary MOSFET, which is turned on by the internal oscillator, cannot be turned off before the minimum **on-time**. During the on-time, the inductor is charged via the input voltage and, if it cannot be discharged by the same amount during the off-time, the average inductor current drastically increases over every switching cycle. This current can reach dangerously high values unless the output capacitor is not charged enough to ensure the inductor discharge rate needed for the volt-second balance.

This condition is common at converter startup due to the low output voltage.

[a] F_{OSC_MIN} = 15 kHz (typical).

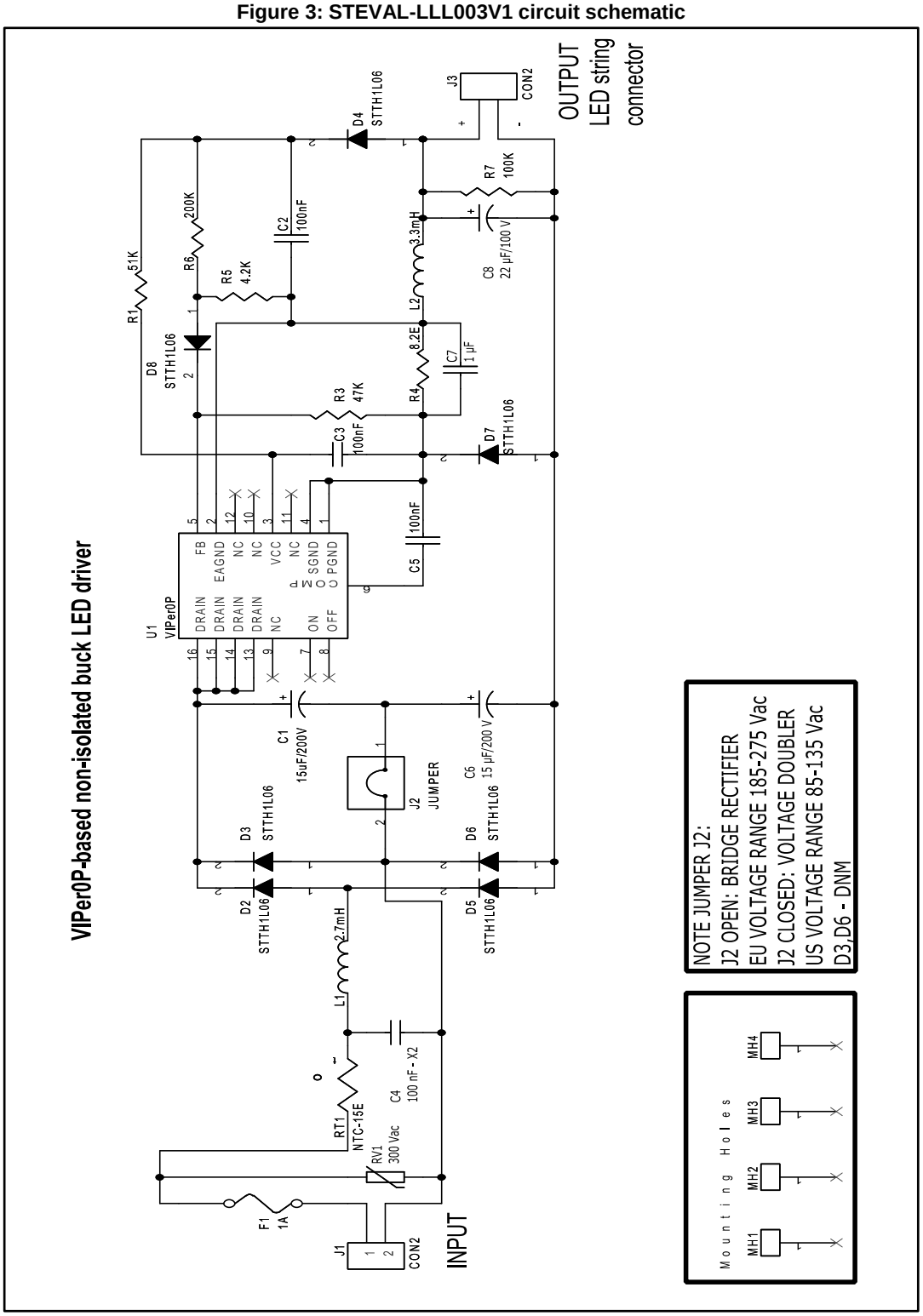
[b] F_{OSC} = 60 or 120 kHz (typical).

[c] 200 ms or 400 ms typ., depending on F_{OSC}

[d] 1 second (typical).

3 Schematic diagram

Figure 3: STEVAL-LLL003V1 circuit schematic



4 Bill of materials

Table 3: STEVAL-LLL003V1 bill of materials

Item	Q.ty	Ref.	Part/Value	Description	Manufacturer	Order code
1	1	U1	Viper0P SO 16 narrow	Zero-power off-line high voltage converter	ST	*VIPER0P*
2	7	D2, D3, D4, D5, D6, D7, D8	600 V/1 A SMA	Ultrafast high voltage rectifier	ST	STTH1L06A
3	1	R1	51 K ±5% SMD-0805	Resistor	ANY	ANY
4	1	R3	47 K ±5% SMD-0805	Resistor	ANY	ANY
5	1	R4	8.2 E ±1% SMD-1206	Resistor	ANY	ANY
6	1	R5	4.2 K ±5% SMD-0805	Resistor	ANY	ANY
7	1	R6	200 K ±5% SMD-0805	Resistor	ANY	ANY
8	1	R7	100 K ±5% SMD-0805	Resistor	ANY	ANY
9	2	C1, C6	15 µF 200 V ±20% SMD	Electrolytic capacitors	Nichicon	ULH2D150MNL1GS
10	3	C2, C3, C5	100 nF 25 V ±10% SMD-0805	Ceramic capacitors	ANY	ANY
11	1	C4	100 nF - X2 305 V ±20% Radial	Polypropylene(PP)	EPCOS (TDK)	B32921C3104M
12	1	C7	1 µF 16 V SMD-0805	Ceramic capacitor	ANY	ANY
13	1	C8	22 µF 100 V ±20% SMD	Electrolytic capacitor	Nichicon	UUX2A220MNL1GS
14	1	L1	2.7 mH 0.3 A ±10% through hole	Unshielded wirewound inductor	Bourns Inc.	RLB9012-272KL
15	1	L2	3.3 mH 300 mA ±5% through hole	Unshielded wirewound inductor	Wurth Electronics Inc.	744772332
16	1	RT1	NTC-15E 0.2 Through Hole	Inrush current limiter	EPCOS (TDK)	B57153S150M

Item	Q.ty	Ref.	Part/Value	Description	Manufacturer	Order code
17	1	RV1	300 Vac through hole	DISC 14MM	EPCOS (TDK)	S14K300
18	1	F1	1 A 300 Vac through hole	Fuse	Littelfuse Inc.	39211000000
19	1	J1	CON2 input through hole	Jumper	ANY	ANY
20	1	J3	CON2 output through hole	Jumper	TE Connectivity AMP Connectors	282834-2
21	1	J2		Jumper	ANY	ANY

5 Testing the board

The board can be tested on Europe voltage range or US voltage range on the basis of jumper J2 position. The string of white LEDs can be connected at the output connector J3 (for the board electrical specifications, refer to *Table 2: "STEVAL-LLL003V1 evaluation board jumper J2: input mains voltage operating range selection"*).

5.1 Efficiency

The active mode efficiency is defined as the average of the efficiency measured at 25%, 50%, 75% and 100% of the maximum load, at nominal input voltages (115 V_{AC} and 230 V_{AC}). External power supplies need to comply with the Code of Conduct, version 5 "Active mode efficiency" criterion which, for a power throughput of 7.5 W, states an active mode efficiency higher than 80% (CoC5). Another applicable standard is the DOE (department of energy) recommendation, whose active mode efficiency requirement for the same power throughput is 79.8%.

The table below shows that the board is compliant with the above standards.

Table 4: STEVAL-LLL003V1 evaluation board: active mode efficiency

Active mode efficiency			
CoC5 requirements (P_{OUT} = 7.5 W)	**DOE requirement (P_{OUT} = 7.5 W)**	**Board performance**	
80%	79.80%	V_{IN} = 110 V_{AC}	86.1%
		V_{IN} = 230 V_{AC}	87.5%

Figure 4: Efficiency vs. input voltage (Europe voltage range) with different number of LEDs

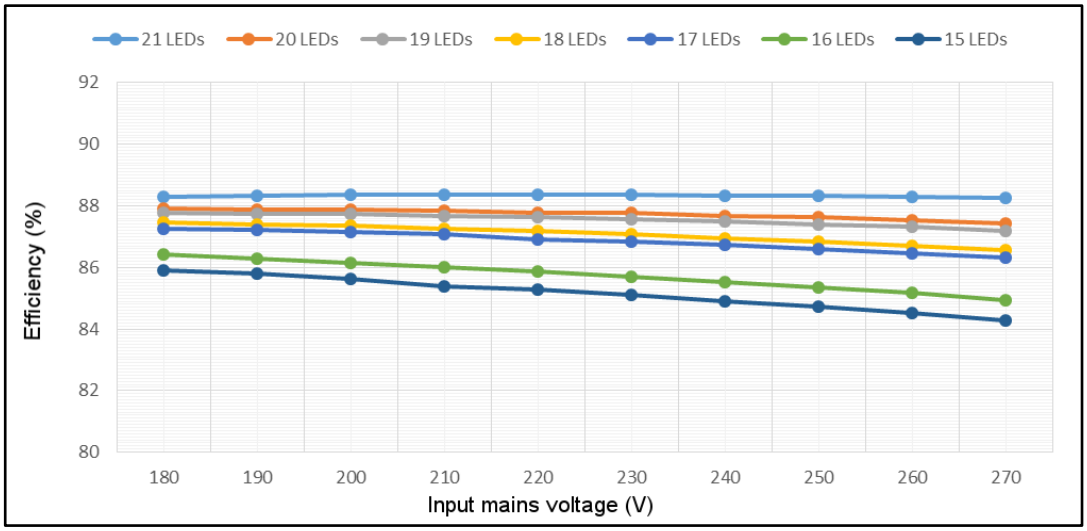


Figure 5: Efficiency vs. input voltage (US voltage range) with different number of LEDs

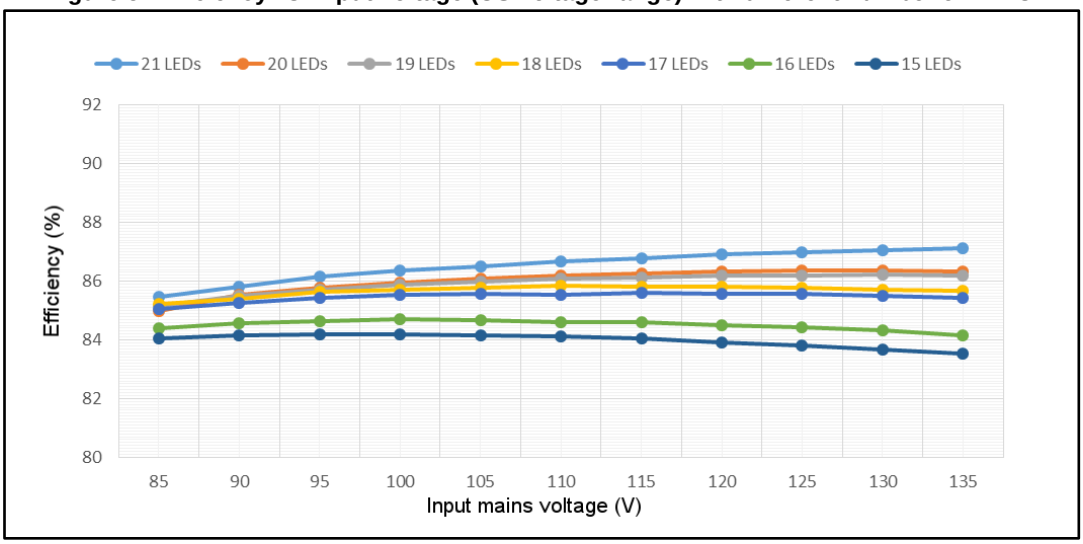


Figure 6: LED current vs. input voltage (Europe voltage range) with different number of LEDs

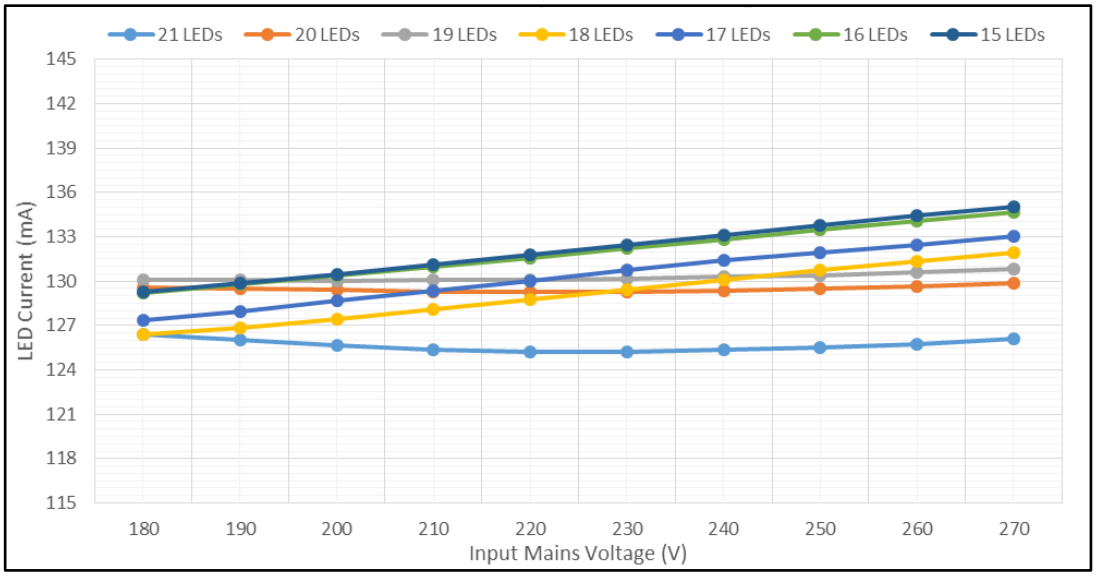
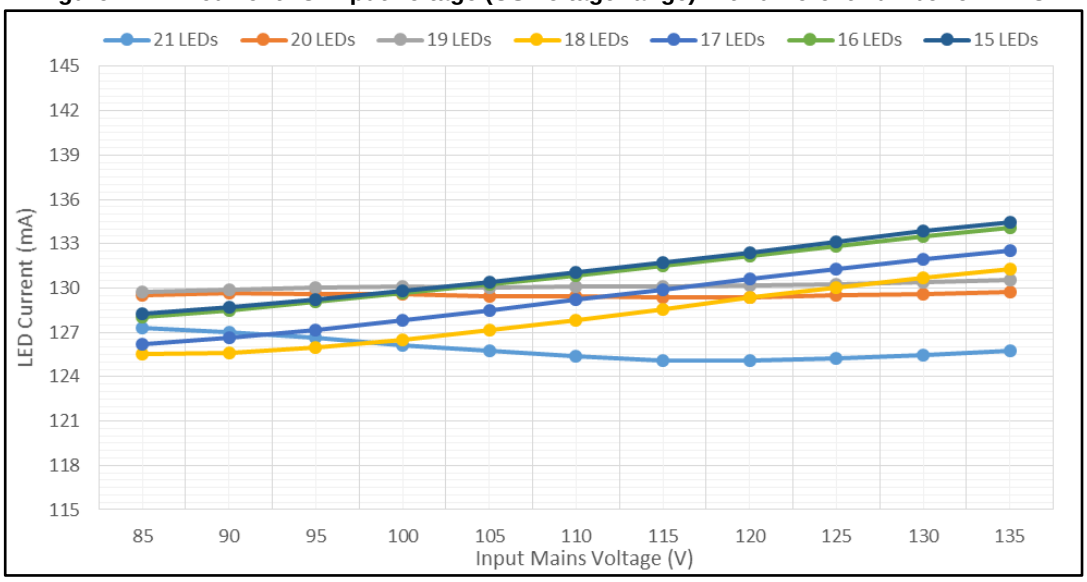


Figure 7: LED current vs. input voltage (US voltage range) with different number of LEDs



The STEVAL-LLL003V1 evaluation board is equipped with open circuit and short circuit protections.

Table 5: STEVAL-LLL003V1 evaluation board: open/no load condition

Input mains voltage	Evaluation board P_{IN} consumption (mW)	Output voltage (V)
110 V_{AC}	210 mW	85.35 V
230 V_{AC}	225 mW	85.46 V

5.2 Typical waveforms

In the STEVAL-LLL003V1 evaluation board, the system ground is different from the VIPer0P ground. The VIPer0P ground can be considered a virtual ground (VGND).

The following figures show the MOSFET source voltage, drain current and output voltage waveforms for the different input voltages.

Figure 8: VIPer0P drain current vs. source vs. output voltage at 85 VAC

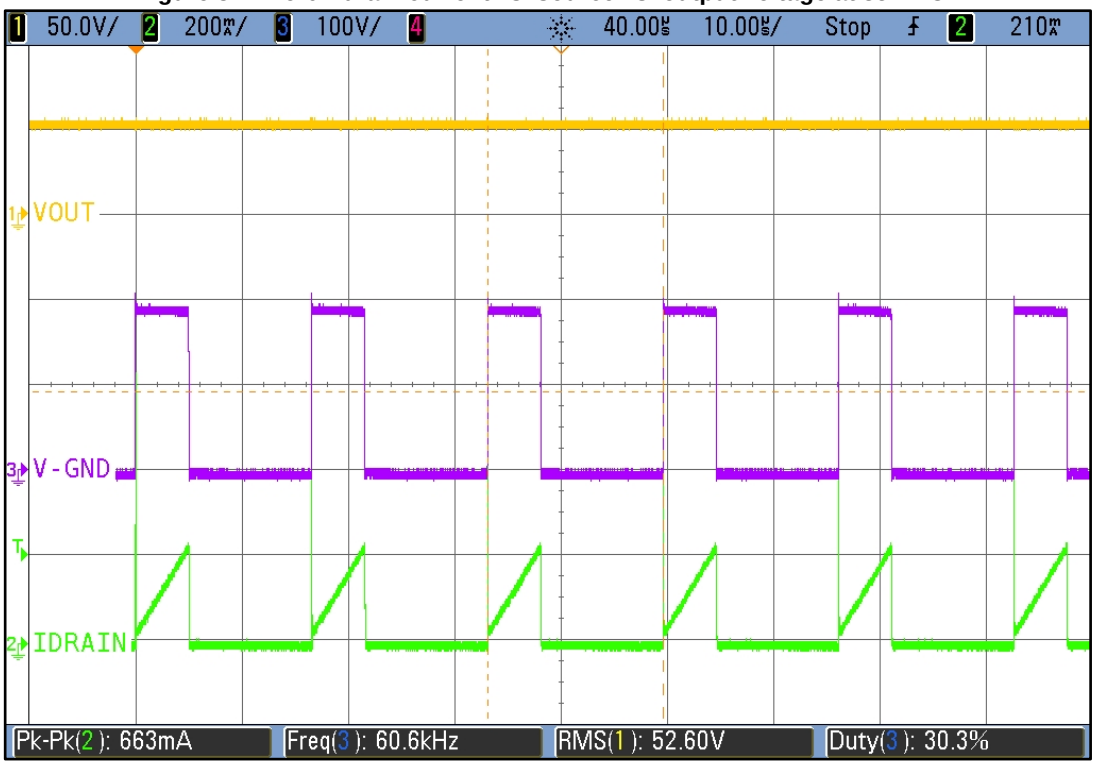


Figure 9: VIPer0P drain current vs. source vs. output voltage at 85 VAC - Zoom

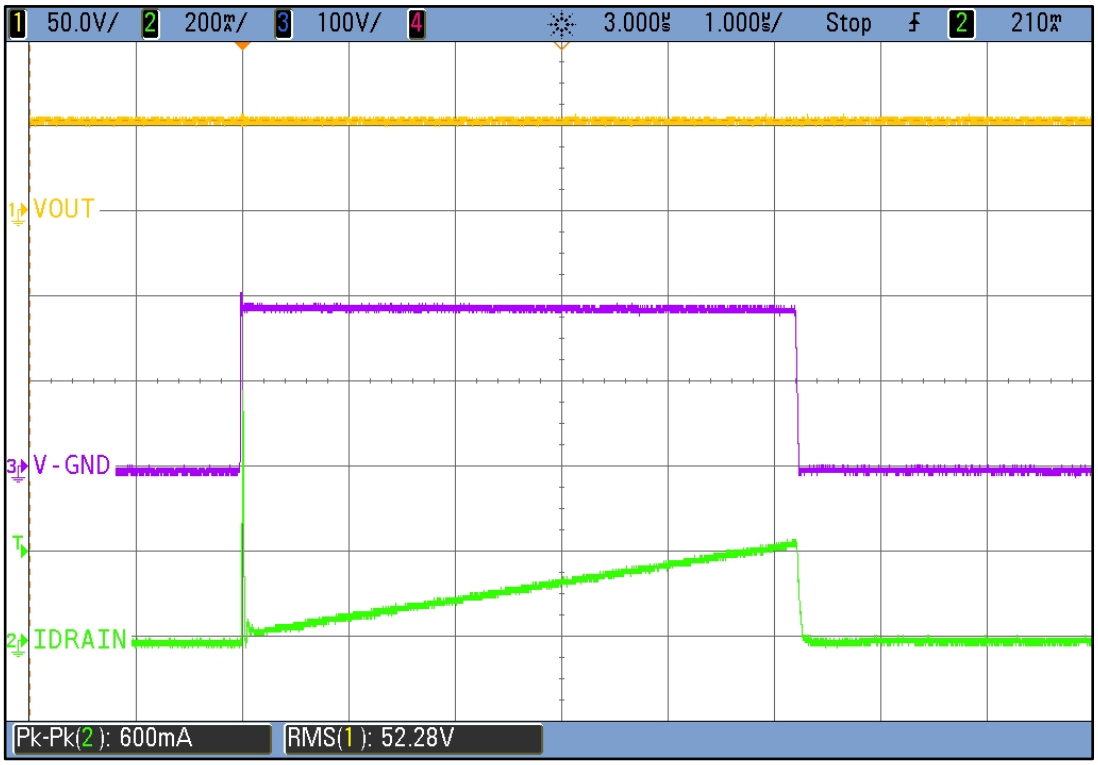


Figure 10: VIPer0P drain current vs. source vs. output voltage at 110 VAC

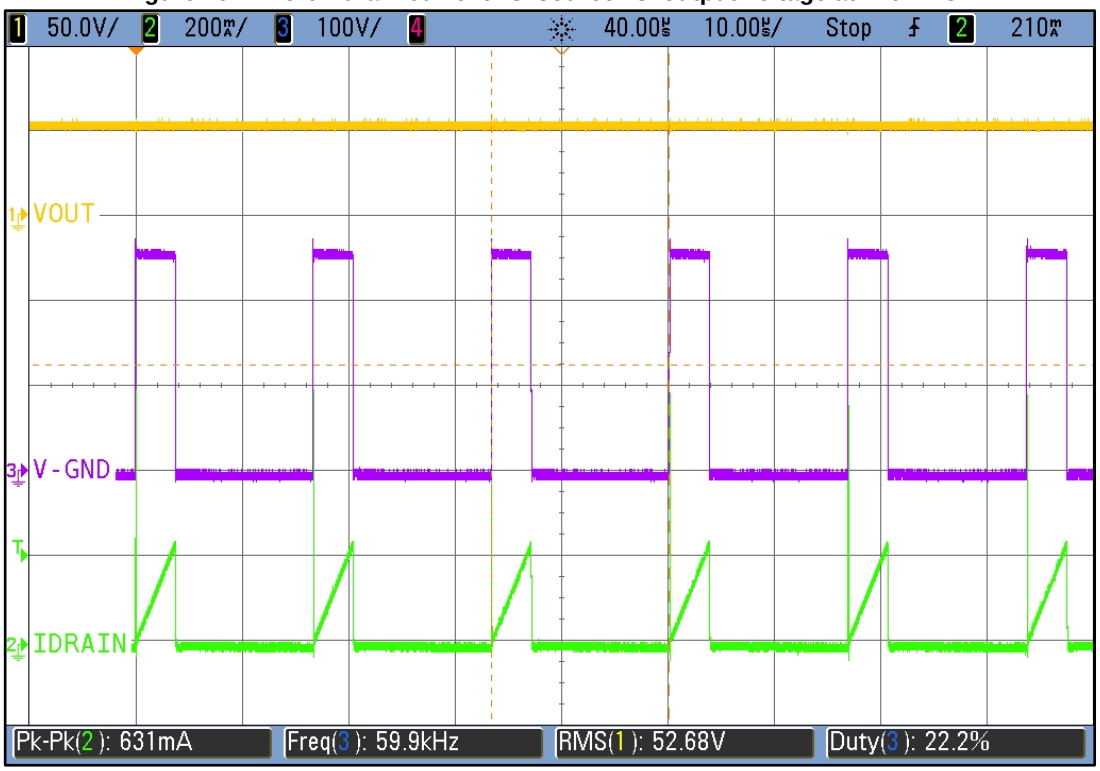


Figure 11: VIPer0P drain current vs. source vs. output voltage at 110 VAC - Zoom

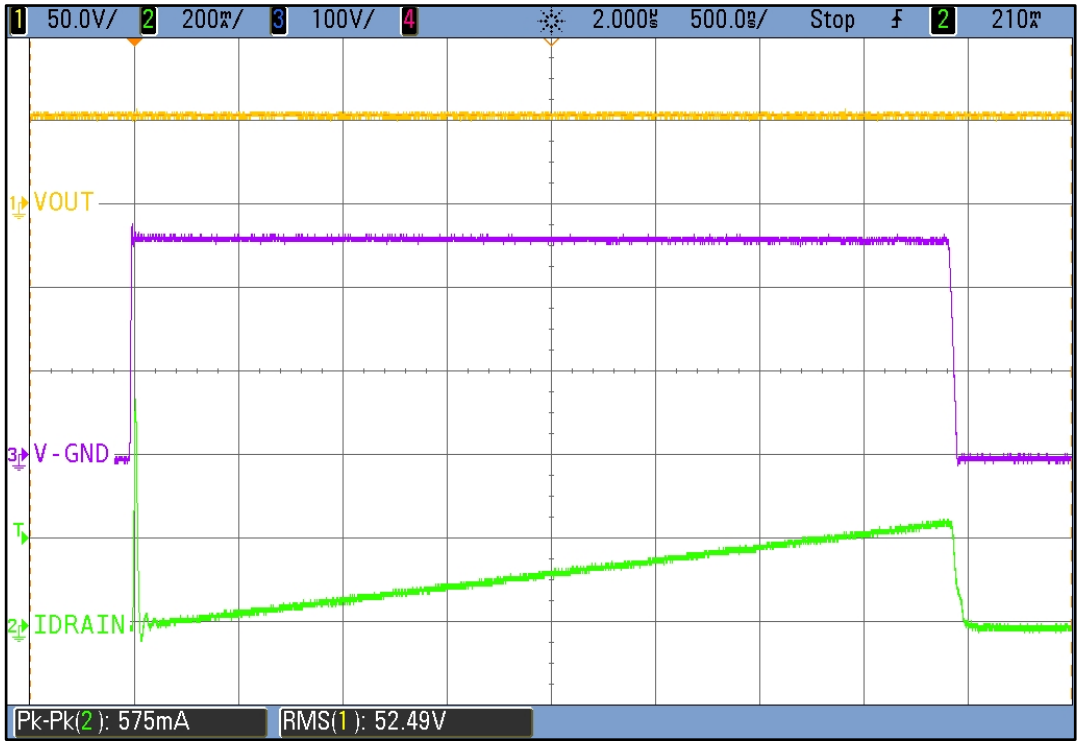


Figure 12: VIPer0P drain current vs. source vs. output voltage at 230 VAC

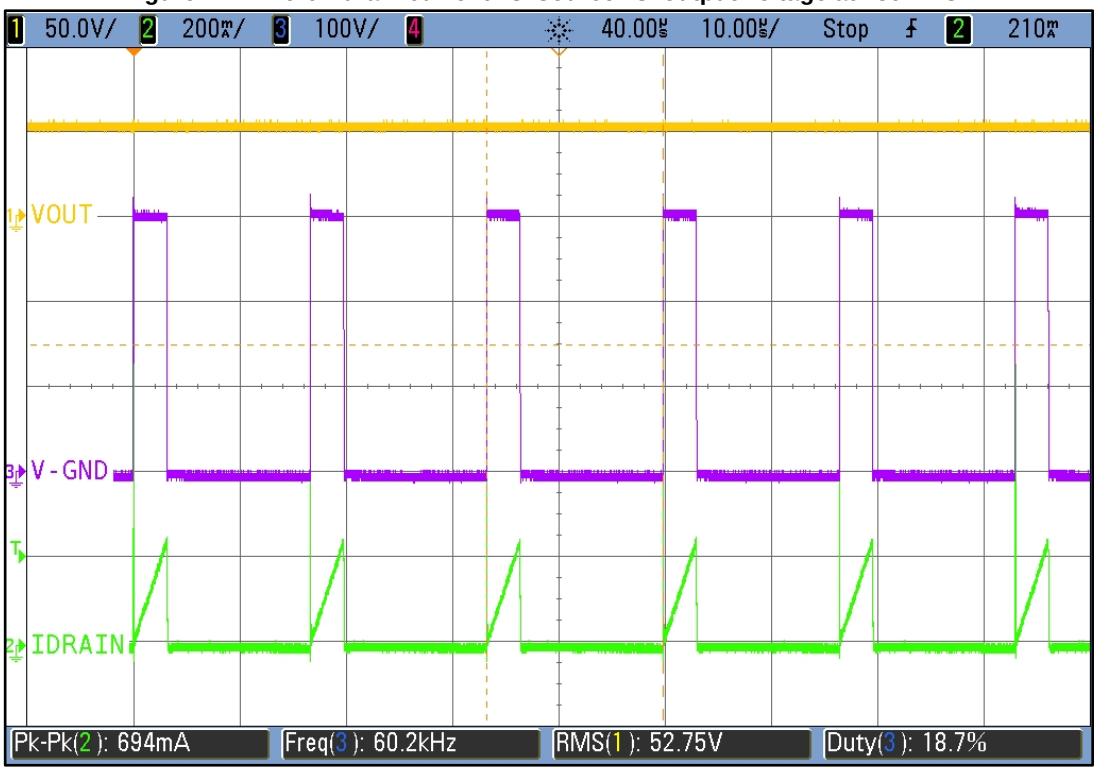


Figure 13: VIPer0P drain current vs. source vs. output voltage at 230 VAC - Zoom

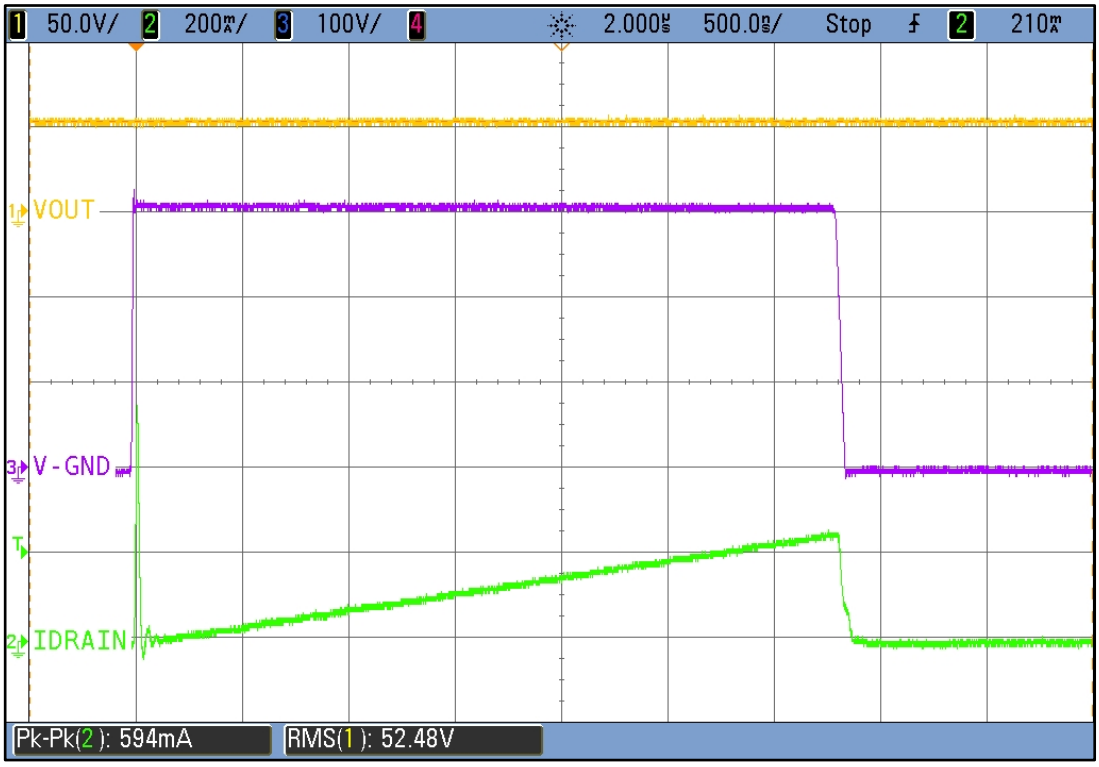


Figure 14: VIPer0P drain current vs. source vs. output voltage at 265 VAC

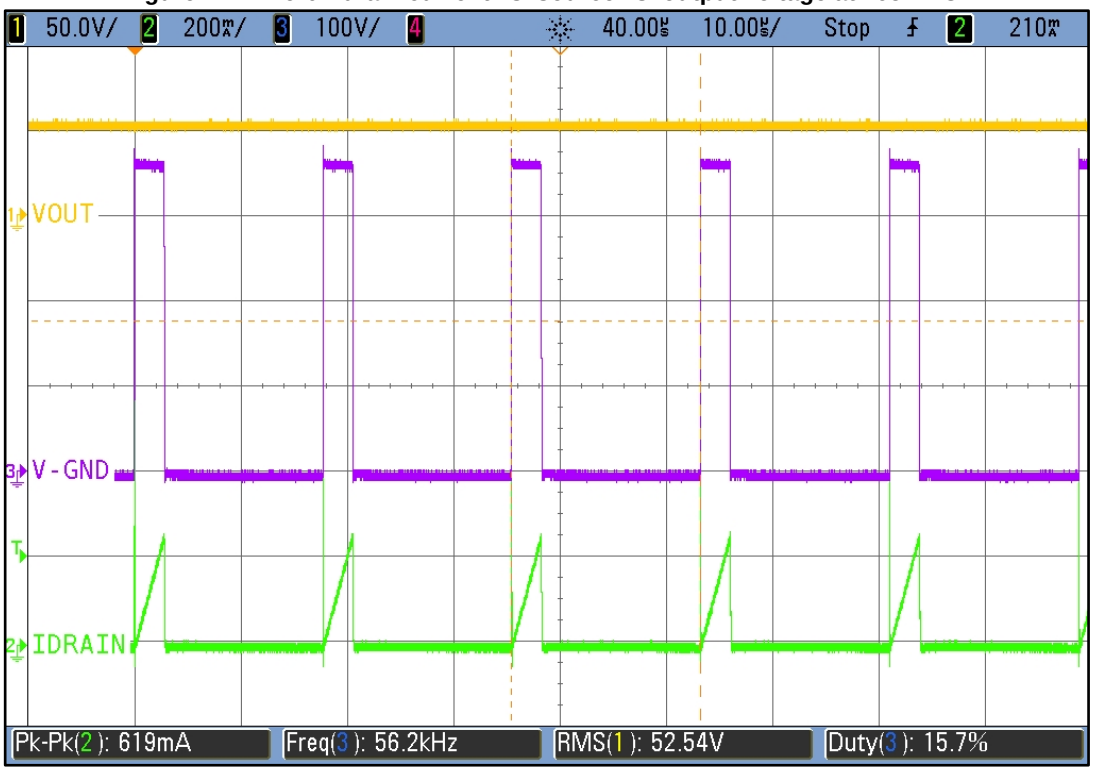
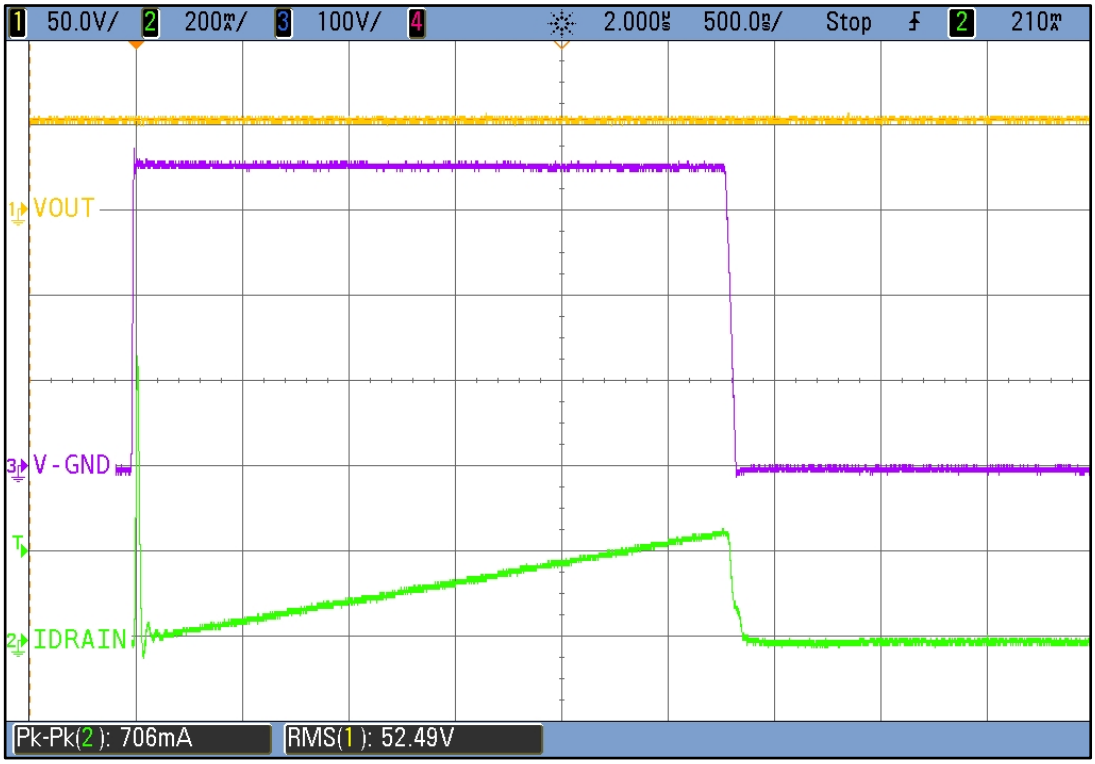


Figure 15: VIPer0P drain current vs. source vs. output voltage at 265 VAC - Zoom



6 Functional check

6.1 Startup

An internal soft-start function progressively increases the cycle-by-cycle current limitation set point from zero to I_{DLIM} in 8 steps. This limits the drain current during the output voltage rise, thus reducing the stress on the secondary diode.

The t_{SS} soft-start time needed for the current limitation to reach its final value is internally set at 8 ms. This function is activated for any converter startup attempt or after a fault event.

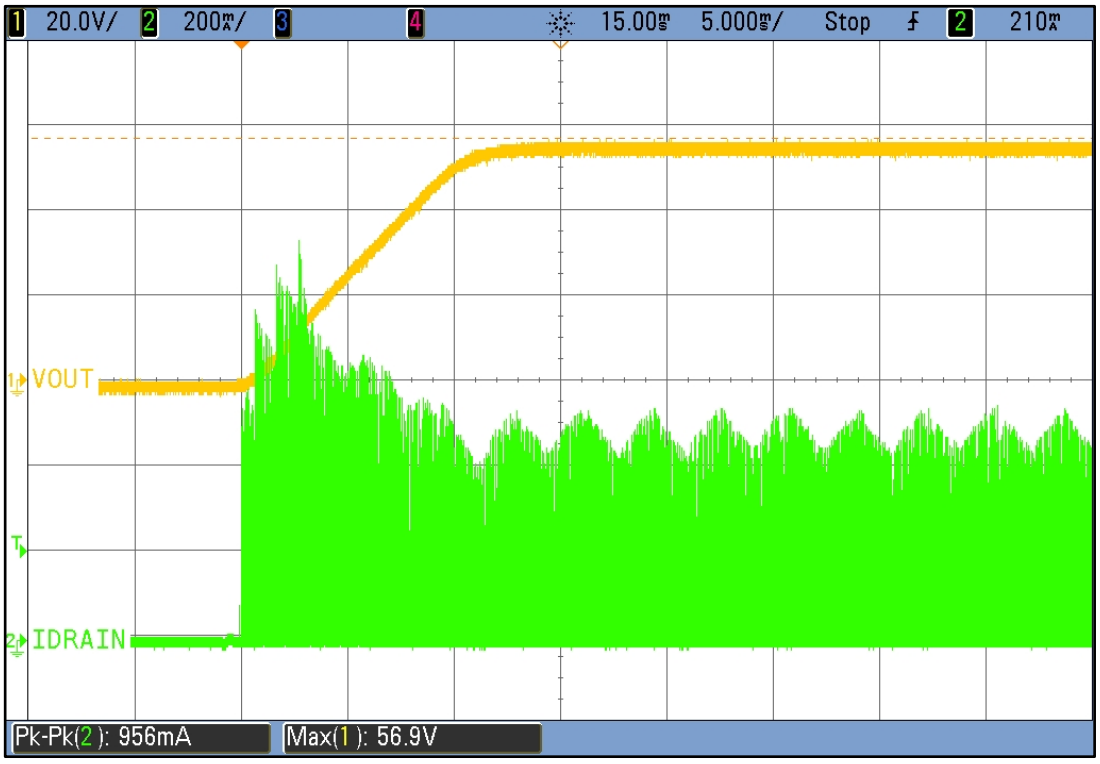
The IC has a pulse skipping feature which skips a switching cycle whenever the OCP comparator is triggered within the minimum on-time. The switching frequency is thus halved, down to the minimum allowed value of F_{OSC_MIN} (15 kHz typ.).

By allowing a longer inductor discharge time, this feature helps to prevent current runaway[a]

Whenever the OCP comparator is not triggered inside the minimum on-time, a switching cycle is restored, thus doubling the switching frequency up to the nominal frequency F_{OSC}.

The following figures show the VIPer0P startup sequence at different input main voltages with maximum load at the output.

Figure 16: Startup - VIPer0P drain current vs. output voltage at 85 VAC



[a] The possible uncontrolled increase in drain current during the very first cycles of converter startup due to the initial inability of the system to maintain the volt-second balance when there is a large input-to-output voltage differential.

Figure 17: Startup - VIPer0P drain current vs. output voltage at 110 VAC

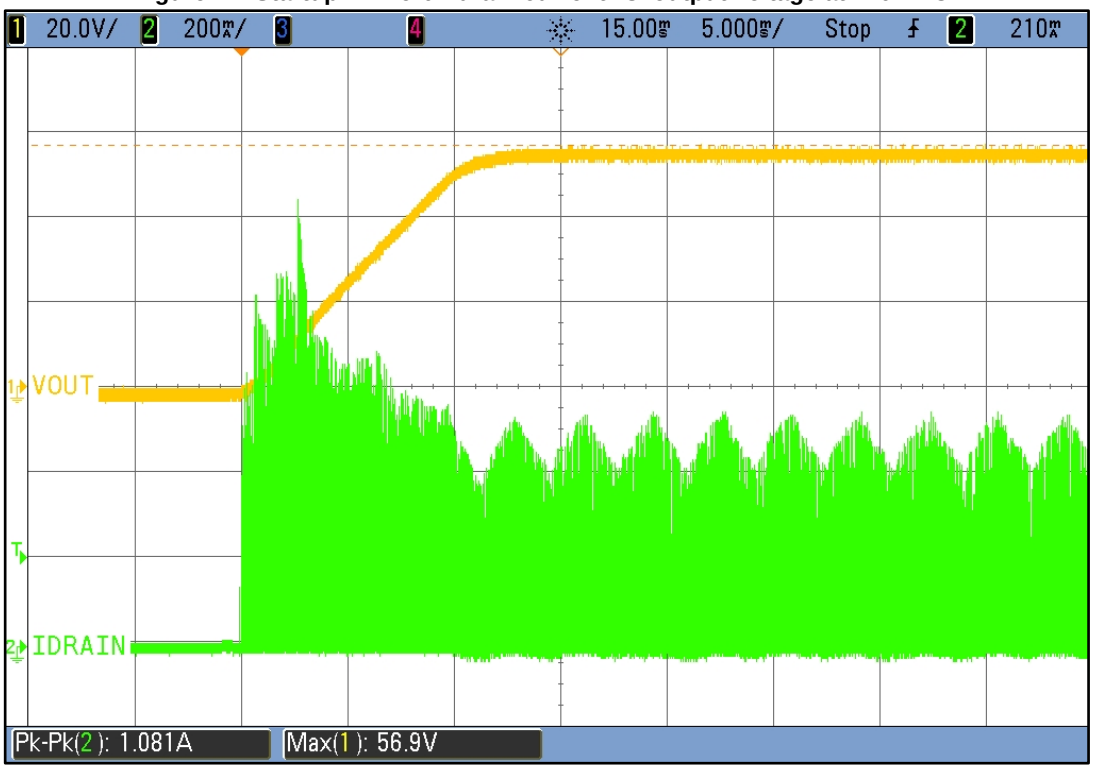


Figure 18: Startup - VIPer0P drain current vs. output voltage at 230 VAC

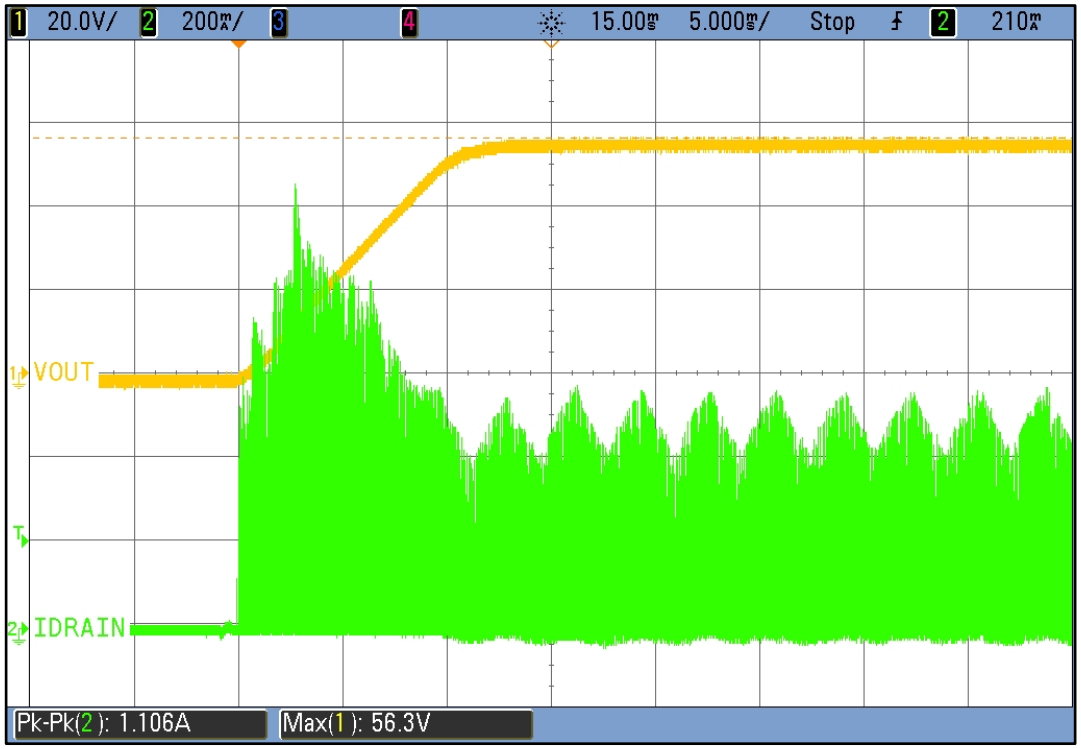
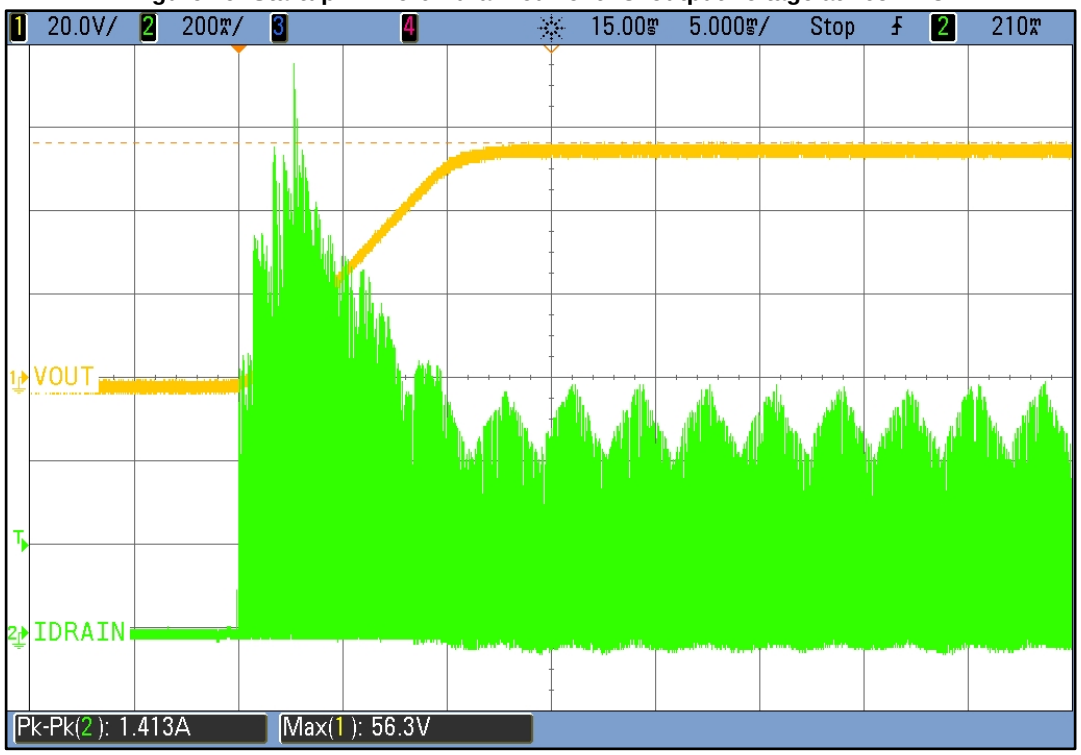


Figure 19: Startup - VIPer0P drain current vs. output voltage at 265 VAC



6.2 Short-circuit and overload protection

To manage the overload condition, the IC embeds the following main blocks: the OCP comparator to turn the power MOSFET off when the drain current reaches its limit (I_{DLIM}), the up and down OCP counter to define the turn off delay time in case of continuous overload (t_{OVL} = 50 ms typ.) and the timer to define the restart time after protection tripping ($t_{RESTART}$ = 1 second, typ.).

In case of short circuit or overload, the control level on the PWM comparator inverting input is greater than the reference level fed into the OCP comparator inverting input. As a result, the cycle-by-cycle power switch turn off is triggered by the OCP comparator in place of the PWM comparator.

Every cycle this condition is met:

- the OCP counter is incremented
- if the fault condition persists for a time greater than t_{OVL} (corresponding to the counter end-of-count), the protection is tripped and the PWM is disabled for $t_{RESTART}$
- the OCP resumes switching with soft-start and, if the fault is still present, it is disabled again after t_{OVL}

The OLP management prevents that the IC could be indefinitely operated at I_{DLIM} and the low repetition rate of the converter restart attempts avoids the IC overheating in case of repeated fault events.

After the fault removal, the IC resumes working normally. Under fault condition, the V_{CC} ranges between V_{CSon} and V_{CCon} levels, due to the periodical activation of the HV current source recharging the V_{CC} capacitor.

Figure 20: Short-circuit condition

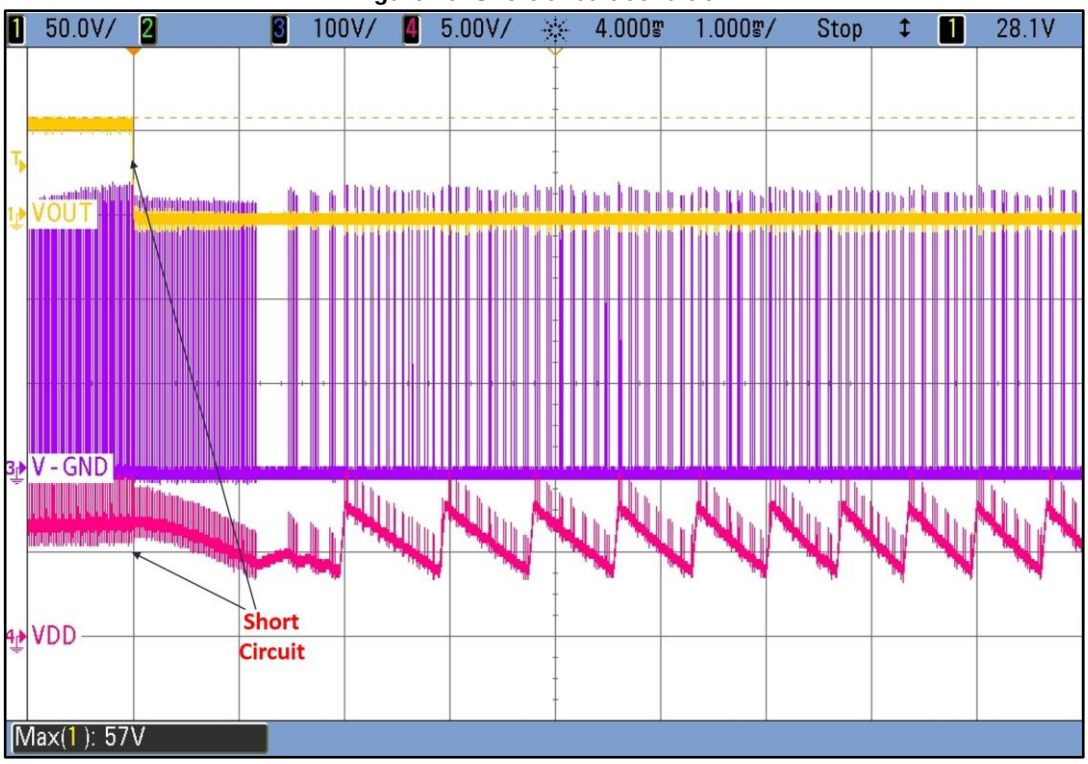
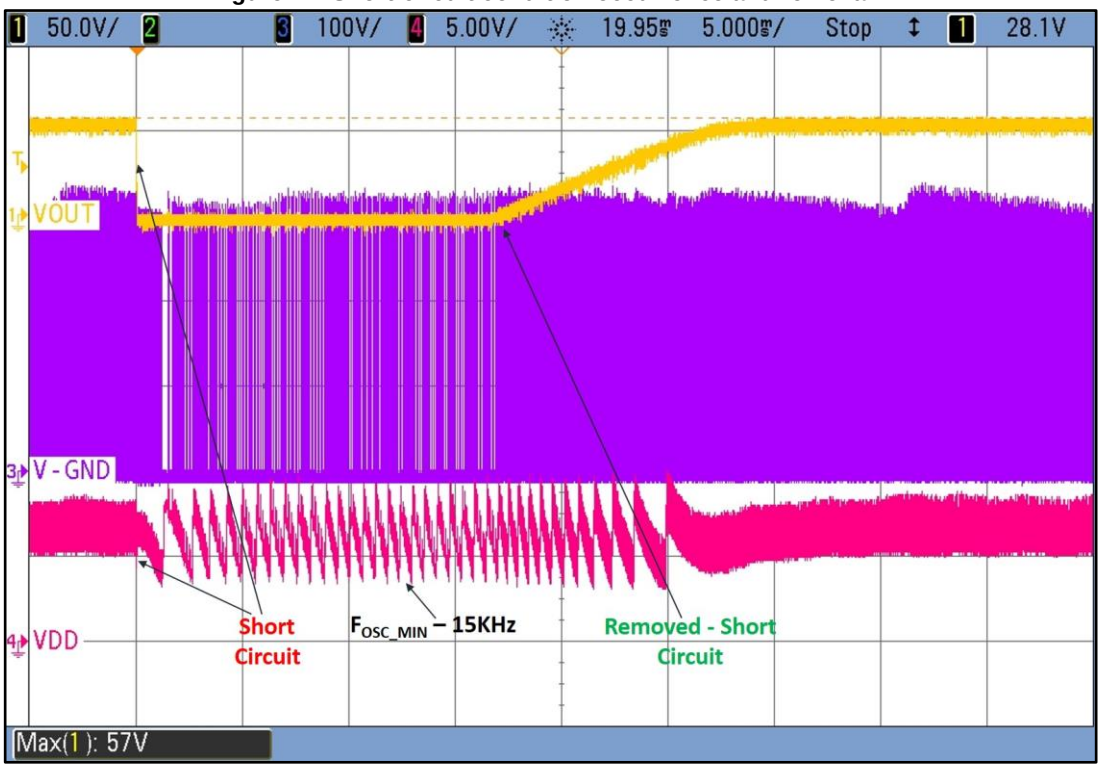


Figure 21: Short-circuit condition occurrence and removal



6.3 Open circuit protection

The STEVAL-LLL003V1 evaluation board is equipped with open circuit protection. In VIPer0P, the FB pin is internally referenced to 1.2 V with respect to EAGND. During normal operation, the FB pin is controlled by the voltage drop across R4. In case of open circuit, the voltage loop (R6, R5 and D8) limits the output voltage to around 80 V.

Figure 22: Open circuit condition

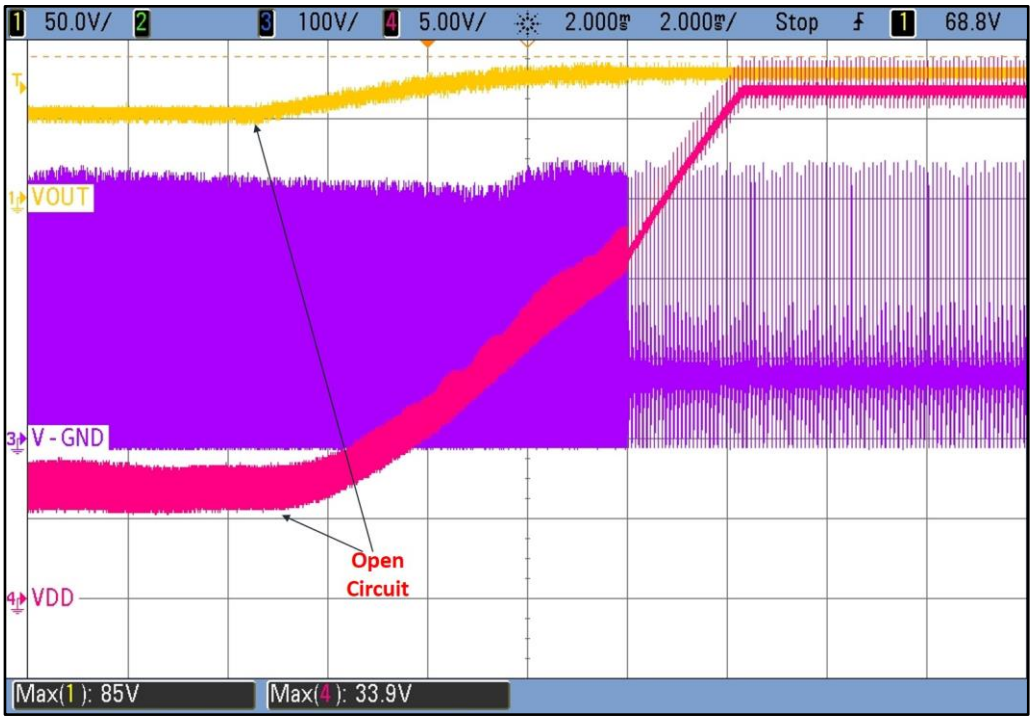
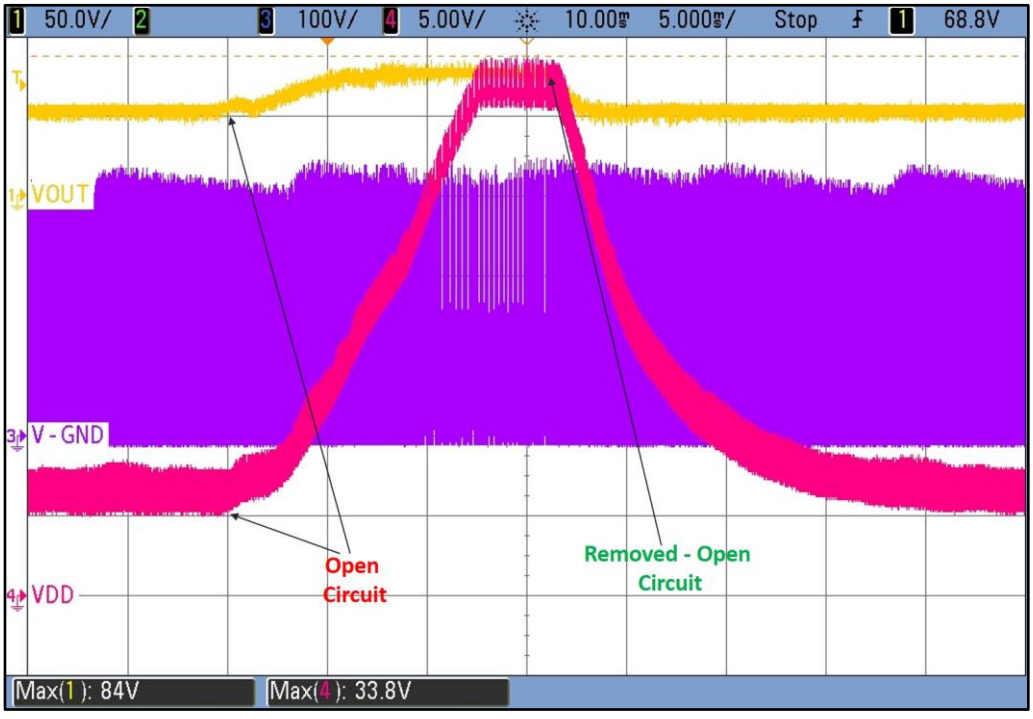


Figure 23: Open circuit condition occurrence and removal



7 Design calculations

The integrated HV startup, sense FET, error amplifier and oscillator with jitter allow a complete application to be designed with a minimum number of components.

To achieve optimal performance, the buck inductor (L2) value should be optimized. The best efficiency and EMI is achieved when the SMPS works close to the boundary between continuous conduction mode (CCM) and discontinuous conduction mode (DCM).

The peak current value should not cross the OC limit internally set in the VIPer0P device.

7.1 Inductor

The inductance minimum value can be calculated by:

Equation 1

$$L_{min2} = \frac{2I_{OUT} \cdot V_{OUT}}{fI_{pkmax}^2} \cdot \left(1 - \frac{V_{OUT}}{V_{INMAX}}\right)$$

The value related to boundary operation can be calculated by:

Equation 2

$$L_2 = \frac{V_{OUT}}{2I_{OUT} \cdot f} \cdot \left(1 - \frac{V_{OUT}}{V_{IN}}\right)$$

The VIPer0PLD device operates at 60 KHz (for details refer to *Table 1: "STEVAL-LLL003V1 evaluation board electrical specifications"*).

By substituting the values, L2 is calculated by:

Equation 3

$$L_2 = \frac{60}{2 \cdot 130mA \cdot 60KHz} \cdot \left(1 - \frac{60}{265 \cdot 1.414}\right) = 3.23mH$$

7.2 LED current

The LED current is defined by sense resistor R4. The value can be calculated by:

Equation 4

$$R_4 = \frac{1.2}{I_{OUTnominal}} \cdot (\Omega)$$

8 Board layout

Figure 24: STEVAL-LLL003V1 evaluation board top layer

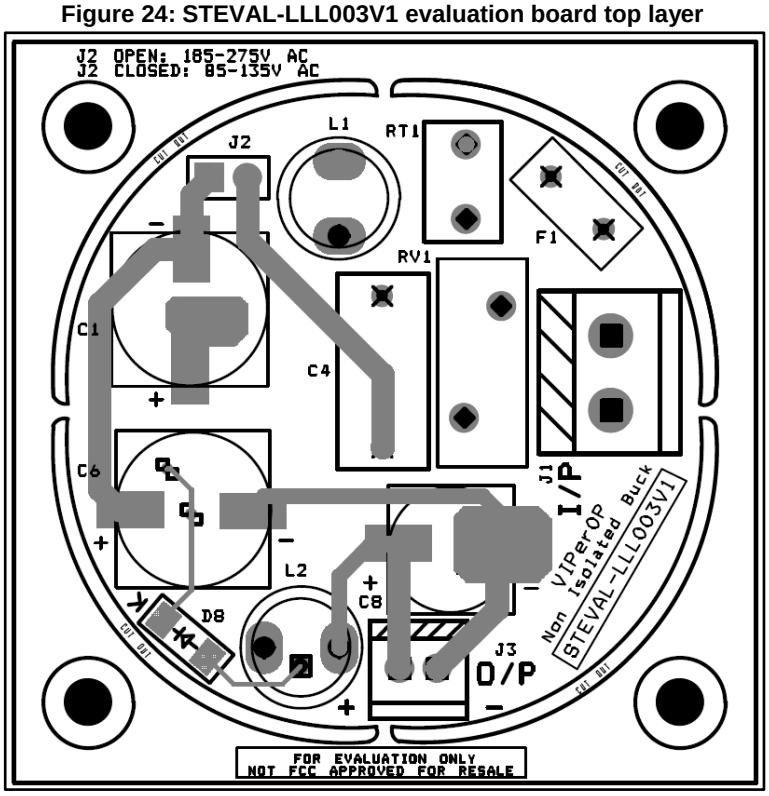
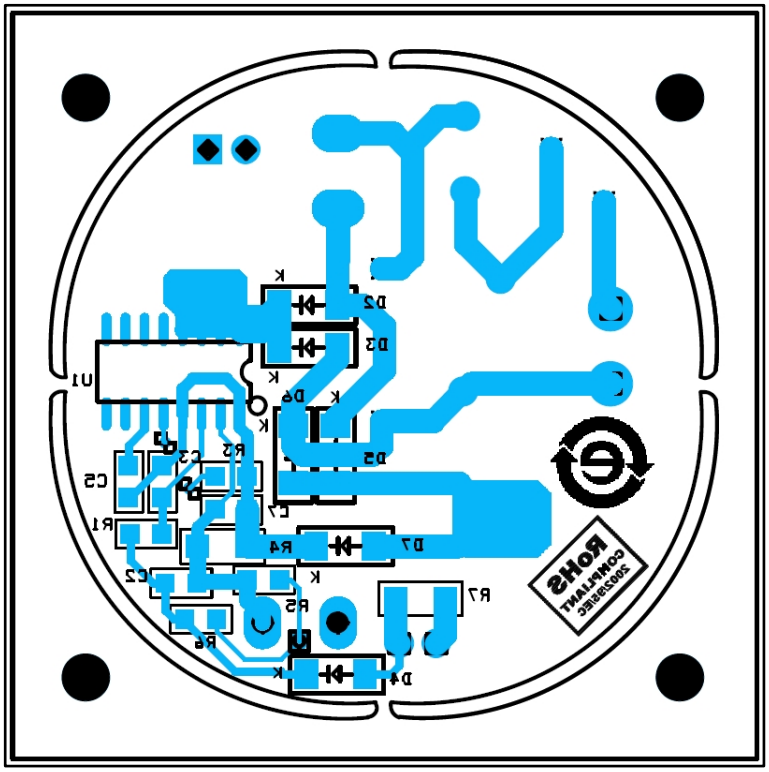


Figure 25: STEVAL-LLL003V1 evaluation board bottom layer



9 Thermal measurements

A thermal analysis of the board was performed using an IR camera at 110 V_{AC} and 230 V_{AC} mains input, under full load condition with an ambient temperature of 25°C. The results are shown in the following figures.

Figure 26: STEVAL-LLL003V1 thermal measurement at 110 VAC (top side)

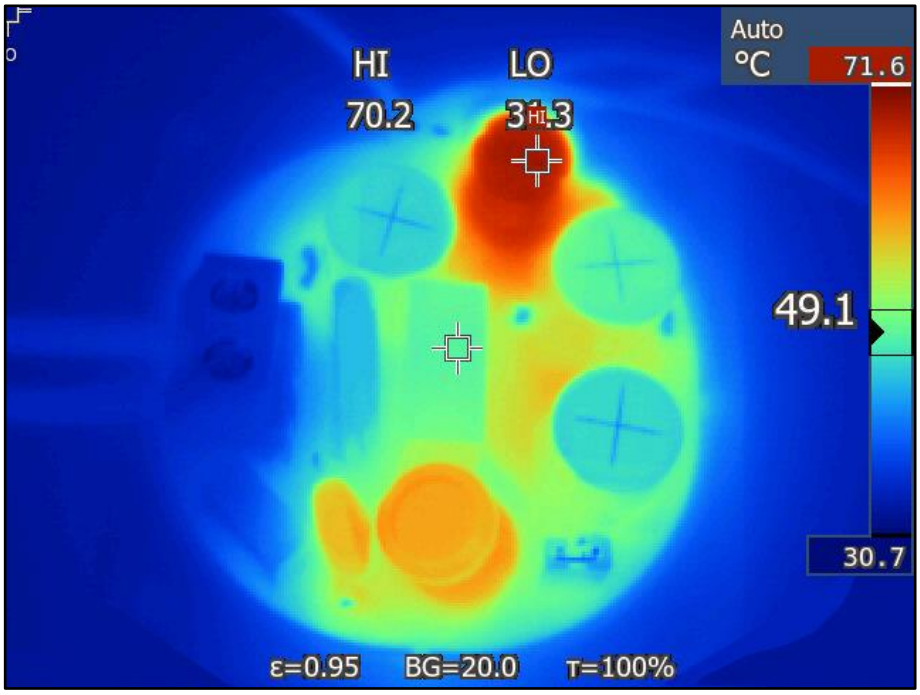
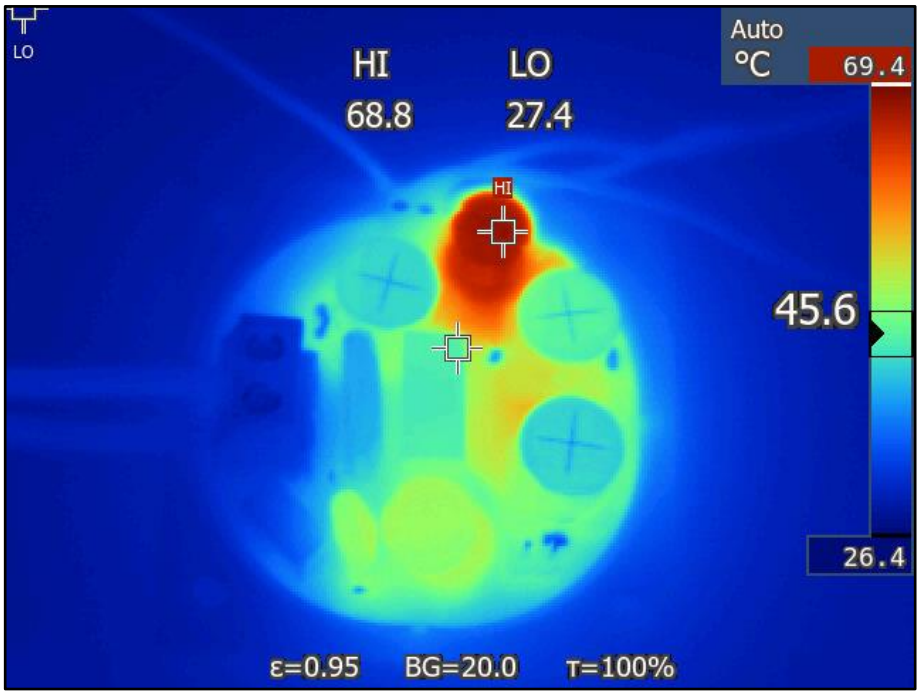


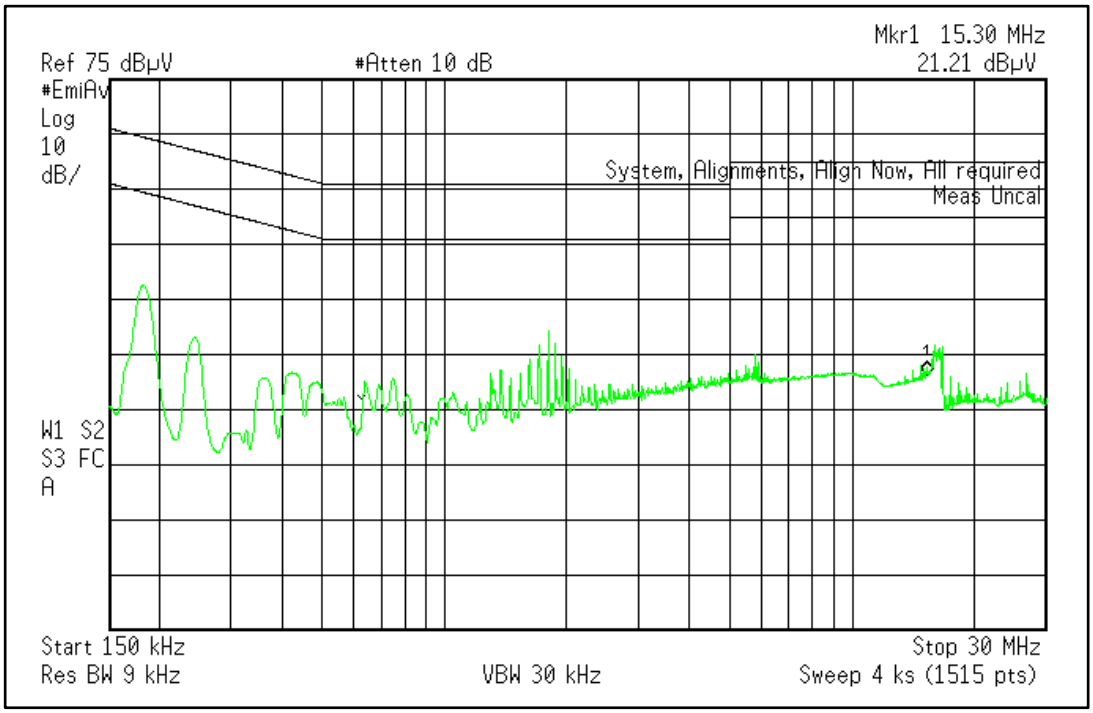
Figure 27: STEVAL-LLL003V1 thermal measurement at 230 VAC (top side)



10 EMI measurements

A pre-compliance test to EN55022 (Class B) European normative has been performed using an EMC analyzer and a LISN. The results are shown below.

Figure 28: Average measurements at 230 Vac, full load, TAMB = 25°C



11 Immunity tests

The board was submitted to immunity tests according to IEC61000 and their results are classified according to the standard criteria:

- A: normal performance
- B: temporary degradation or loss of function or performance, with automatic return to normal operation
- C: temporary degradation or loss of function, with external intervention to recover normal operation
- D: degradation or loss of function, necessary substitution of damaged components to recover normal operation

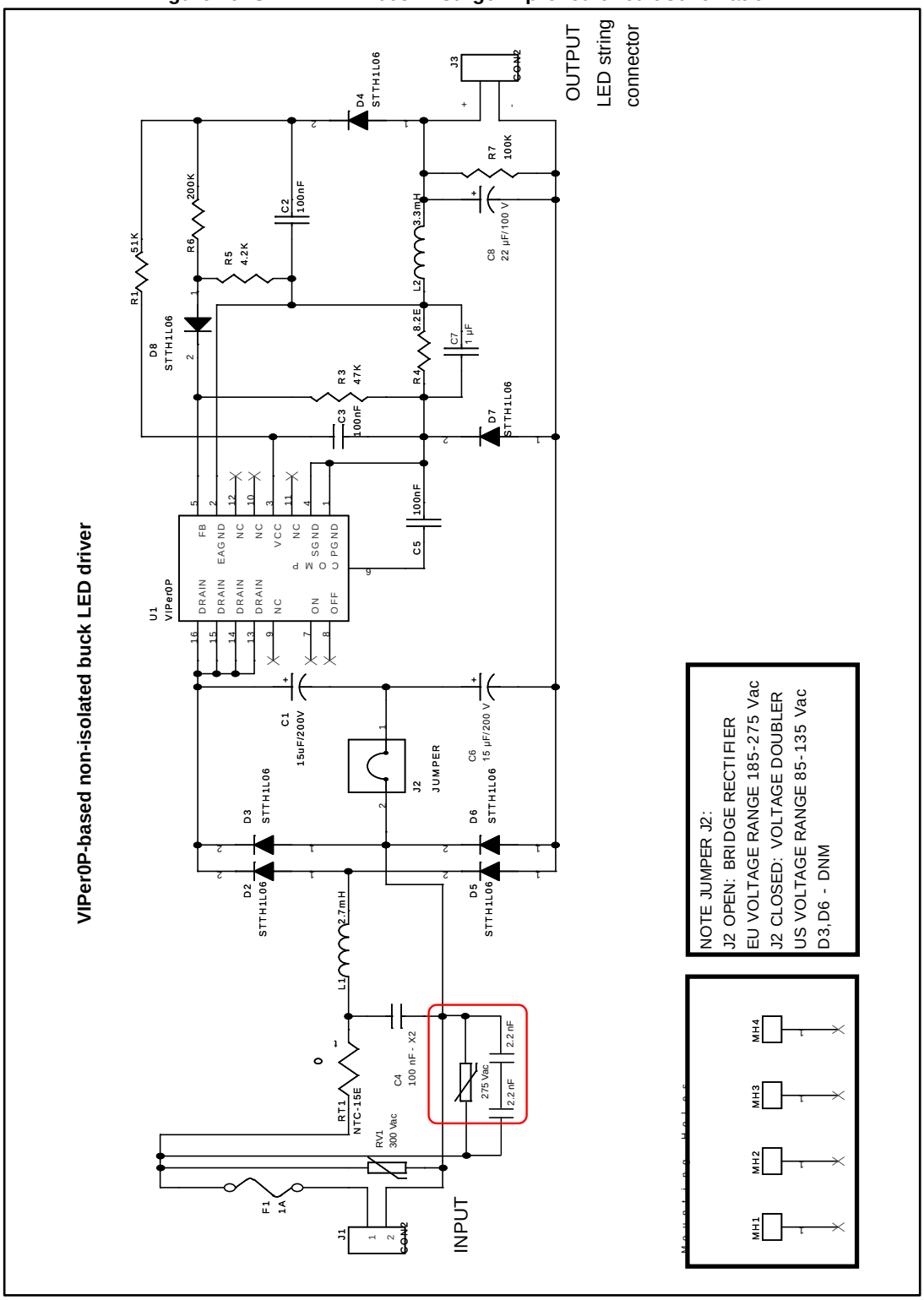
11.1 Surge immunity test (IEC 61000-4-5)

The test conditions are:

- repetition rate: 1 minute (5 positive and 5 negative surges)
- applied to input lines vs. EARTH – common mode
- applied to both input lines (L vs. N) - differential mode
- reference plane connected to Protected Earth according to the normative

In order to pass the test, the STEVAL-LLL003V1 schematic diagram has been modified with the additions highlighted in the figure below, consisting of an input filter made up of a 275 V_{AC} varistor and two 2.2 nF Y1 capacitor in series. The common point of the capacitors is the Protected Earth, which during the tests has to be connected to the reference plane, according to the normative.

Figure 29: STEVAL-LLL003V1 surge improved circuit schematic



The input voltage has been set to 230 V_{AC} and the output at full load, proper operation has been checked through the blinking of a LED connected to the output. Test results are listed in the following tables.

Table 6: Common mode surge test results

Noise injection	Surge level	Polarity	Result	Criterion
L vs. PE	2 kV	Positive	PASS	A
N vs. PE	2 kV	Positive	PASS	A
L vs. PE	2 kV	Negative	PASS	A
N vs. PE	2 kV	Negative	PASS	A

Table 7: Differential mode surge test results

Noise injection	Surge level	Polarity	Result	Criterion
L vs. N	2 kV	Positive	PASS	A
L vs. N	2 kV	Negative	PASS	A

Performed tests show that the board withstands the lightning disturbances applied to input line in common mode and differential mode for each severity level.

11.2 ESD immunity test (IEC 61000-4-2)

The test conditions are:

- Contact discharge and air discharge methods
- Discharge circuit150 pF/330 Ω
- Polarity: positive/negative

The setting of *Figure 29: "STEVAL-LLL003V1 surge improved circuit schematic"*allowed passing also the ESD test.

The purpose of the input filter (varistor and the 2.2 nF Y1 capacitors) is only to provide the Protected Earth (common point of the capacitors) for the ESD signal correct coupling according to the IEC 61000-4-2 normative.

The input voltage has been set to 230 V_{AC} and the output at full load, proper operation has been checked through the blinking of a LED connected to the output.

The test results are listed in the following tables.

Table 8: ESD contact discharge test results

Noise injection	ESD level	Polarity	Result	Criterion
L vs. PE	10 kV	Positive	PASS	A
L vs. PE	10 kV	Negative	PASS	A
N vs. PE	10 kV	Positive	PASS	A
N vs. PE	10 kV	Negative	PASS	A

Table 9: ESD air discharge test results

Noise injection	ESD level	Polarity	Result	Criterion
Horizontal coupling plane	20 kV	Positive	PASS	A
Horizontal coupling plane	20 kV	Negative	PASS	A
Vertical coupling plane	20 kV	Positive	PASS	A
Vertical coupling plane	20 kV	Negative	PASS	A

11.3 Burst immunity test (IEC 61000-4-4)

The test conditions are:

- polarity: positive/negative
- burst duration: 15 ms ±20% at 5 kHz
- burst period: 300 ms ±20%
- duration time: 1 minute
- applied to: AC lines through integrated capacitive coupling clamp

The test can be passed with the original setting (*Figure 3: "STEVAL-LLL003V1 circuit schematic"*).

The input voltage has been set to 230 V_{AC} and the output at full load; proper operation has been checked through a current probe connected to the output.

The test results are listed in the following table.

Table 10: Burst test results

Noise injection	Burst level	Polarity	Result	Criterion
L/PE	4 kV	Positive	PASS	A
N/PE	4 kV	Positive	PASS	A
L/N	4 kV	Positive	PASS	A
L/PE	4 kV	Negative	PASS	A
N/PE	4 kV	Negative	PASS	A
L/N	4 kV	Negative	PASS	A

12 References

1. VIPer0P datasheet
2. IEC 61000-4-2
3. IEC 61000-4-4
4. IEC 61000-4-5

13 Revision history

Table 11: Document revision history

Date	Version	Changes
27-Nov-2017	1	Initial release

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