AN5057
Application note

12 V, 7.8 W isolated flyback converter based on VIPer114LS

Introduction

The STEVAL-ISA197V1 evaluation board is a 12 V, 7.8 W power supply in isolated flyback topology with VIPer114LS, the latest innovative IC by STMicroelectronics for building smart power supplies with green energy management.

The board features:

- Five-star energy efficient when operating at no load ($P_{IN\_NO\_LOAD}$ < 20 mW at 230 V_{AC})
- Compliant with the 10% load efficiency and 4-point average active mode efficiency targets prescribed by the European CoC ver.5 Tier 2
- Meets IEC55022 Class B conducted EMI even with reduced EMI filter, thanks to the frequency jittering feature
- RoHS compliant

The available protections are:

- Pulse skip mode to avoid flux-runaway
- Delayed overload protection (OLP)
- Max duty cycle counter
- V_{CC} clamp
- Input or output overvoltage protection
- Thermal shutdown

Except for pulse-skip mode, all protections are in auto-restart mode.

The VIPer114LS features:

- 800 V avalanche rugged Power MOSFET
- Embedded HV start-up
- Pulse frequency modulation (PFM) and ultra-low stand-by consumption of the internal circuitry under light load condition
- 60 kHz fixed switching frequency with jittering
- Embedded error amplifier internally referenced to 1.2 V ±2%
- Self-supply option to avoid auxiliary winding and bias components
- Current mode PWM controller with drain current limit protection for easy compensation

Figure 1: STEVAL-ISA197V1 evaluation board (top view)

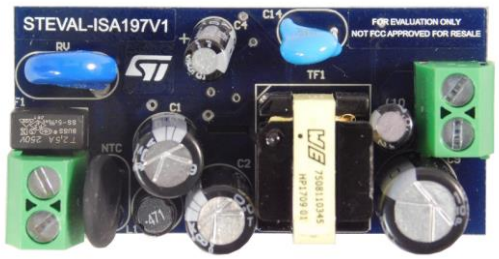
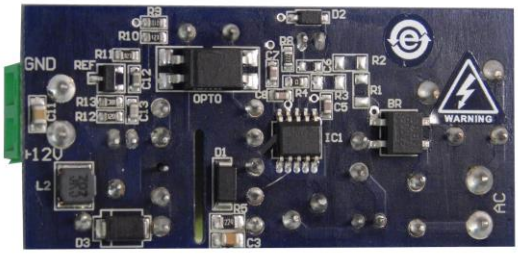


Figure 2: STEVAL-ISA197V1 evaluation board (bottom view)



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1 Board electrical specifications and design

Table 1: STEVAL-ISA197V1 electrical specifications

Parameter	Min.	Typ.	Max.	Unit
AC main input voltage	90		265	V_{AC}
Main frequency (f_L)	50		60	Hz
Output Voltage	11.4	12	12.6	V
Output Current			0.65	A
Rated output power		7.8		W
Output ripple voltage			100	mV
Standby input power at 230 V_{AC}			20	mW
Active mode efficiency	80.7			%
Active mode efficiency at 10% nameplate O/P	70.7			%
Ambient operating temperature			60	ºC

The power supply is set in isolated flyback topology (see *Section 1.1: "Schematic diagram"* for the STEVAL-ISA197V1 schematic diagram and *Section 1.2: "Bill of materials"* for the BOM).

The input section includes a diode bridge (BR), an NTC resistor for inrush current limiting and a π filter (C1, L1, C2) for EMC suppression.

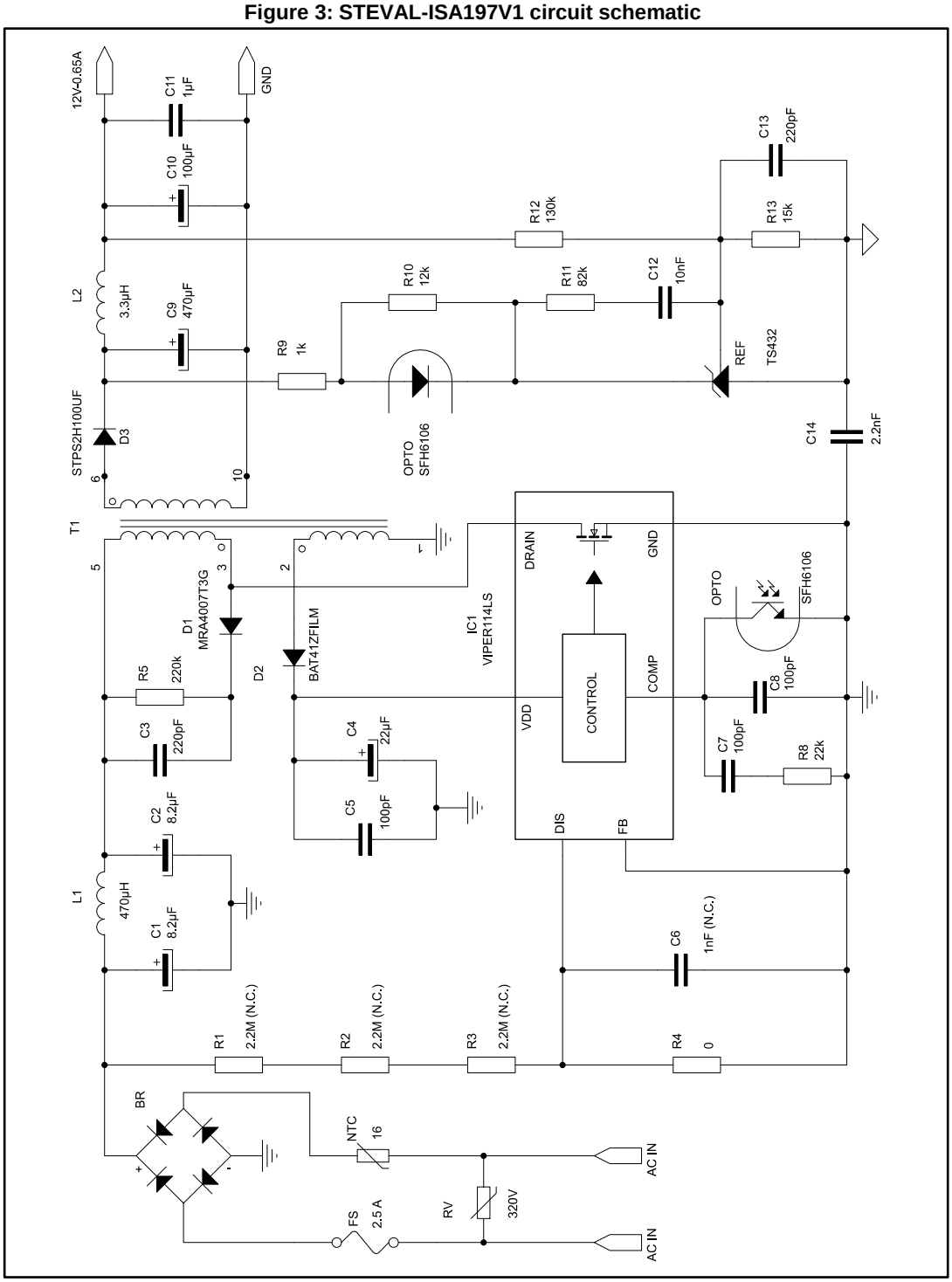
A clamp network (D1, R5, C3) is used for leakage inductance demagnetization.

The resistors R1, R2, R3 and R4 (with C6 in parallel) create a voltage divider from the rectified input mains to DIS voltage which can be used to perform an input overvoltage protection (for further details refer to *Section 5.4: "Input overvoltage protection"*).

As a default setting, R4 = 0 while R1, R2, R3 and C6 are not mounted to minimize the input power consumption at no load and light load.

1.1 Schematic diagram

Figure 3: STEVAL-ISA197V1 circuit schematic



1.2 Bill of materials

Table 2: STEVAL-ISA197V1 bill of materials

Item	Q.ty	Ref.	Part/Value	Description	Manufacturer	Order code
1	1	IN		Input connector	TE Connectivity	282837-2
2	1	OUT		Output connector	TE Connectivity	282837-2
3	1	RV		MOV	EPCOS	B72210S0321K101
4	1	BR	MBS	Bridge rectifier	Taiwan Semiconductor	RMB6S
5	1	FS	2.5 A	Fuse	Cooper Bussmann	SS-5-2-5A-BK
6	1	NTC	16 Ω		EPCOS	B57236S160M
7		R1		Not connected		
8		R2		Not connected		
9		R3		Not connected		
10	1	R4	0 Ω, 0603		Panasonic	ERJ3GEY0R00V
11	1	R5	220 kΩ ±5%, 0.33 W, 0805		TE Connectivity	CRGH0805J220K
12	1	R8	22 kΩ ±5%, 0.2 W, 0603		TE Connectivity	CRGH0603J22K
13	1	R9	1 kΩ ±5%, 0.1 W, 0603		Panasonic	ERJ3GEYJ102V
14	1	R10	12 kΩ ±5%, 0.1 W, 0603		Panasonic	ERJ3GEYJ123V
15	1	R11	82 kΩ ±5%, 0.2 W, 0603		TE Connectivity	CRGH0603J82K
16	1	R12	130 kΩ ±1%, 0.1 W, 0603		Panasonic	ERJ3EKF1303V
17	1	R13	15 kΩ ±1%, 0.1 W, 0603		TE Connectivity	CRG0603F15K
18	2	C1, C2	8.2 µF, 400 V, Ø 8 mm, p 3.5 mm	Electrolytic capacitor	Rubycon	400AX8.2M8X16
20	1	C3	220 pF, 1000 V, 0805	MLCC capacitor	Kemet	C0805C221KDRACTU
21	1	C4	22 µF, 50 V, Ø 5 mm, p 2 mm	Electrolytic capacitor	Rubycon	50YXM22MEFC5X11

Item	Q.ty	Ref.	Part/Value	Description	Manufacturer	Order code
22	3	C5, C7, C8	100 pF, 50 V, 0603	MLCC capacitor	Wurth Elektronik	885012206077
23		C6		Not connected		
26	1	C9	470 µF, 25 V, Ø 10 mm, p 5 mm	Electrolytic capacitor	Rubycon	25YXH470MEFC10X16
27	1	C10	100 µF, 25 V, Ø 5 mm, p 2 mm	Electrolytic capacitor	Rubycon	25YXJ100M5X11
28	1	C11	1 µF, 25 V, 0805	MLCC capacitor	Murata	GRM21BR71E105KA99L
29	1	C12	10 nF, 50 V, 0603	MLCC capacitor	Murata	GRM188R71H103KA01D
30	1	C13	220 pF, 50 V, 0603	MLCC capacitor	Wurth Elektronik	885012206079
31	1	C14	2.2 nF, 250 Vac, Ø 8 mm, p 5 mm	Ceramic X1/Y2 capacitor	Murata	DE2E3KY222MA2BM01F
32	1	D1	1 A, 1000 V, SMA	General purpose diode	ONSemiconductors	MRA4007T3G
33	1	D2	0.2 A, 100 V, SOD-123	Signal Schottky	ST	BAT41ZFILM
34	1	D3	2 A, 100 V, SMB	Power Schottky	ST	STPS2H100U
35	1	L1	470 µH, XS Ø 6 mm, h 8.5 mm		Wurth Elektronik	7447462471
36	1	L2	3.3 µH, (4x4) mm		Wurth Elektronik	74404042033
37	1	IC1	SSO10	Offline HV converter	ST	VIPer114LS
38	1	OPT	SMD	Optocoupler	Vishay	SFH6106-2T
39	1	REF	SOT23	Reference	ST	TS432ILT
40	1	T1		Flyback transformer	Wurth Elektronik	7508110345 Rev6A

1.3 Transformer

Table 3: Transformer characteristics

Parameter	Value
Manufacturer	Wurth Elektronik
Order code	7508110345 Rev6A
Primary inductance	2 mH ± 10%
Leakage inductance	45 µH Max
Primary turns (3-5)	133
Secondary turns (6-10)	23
Auxiliary turns (2-1)	12
Core	E16

Figure 4: Dimensional drawing, pin placement (distances, bottom view) and electrical diagrams

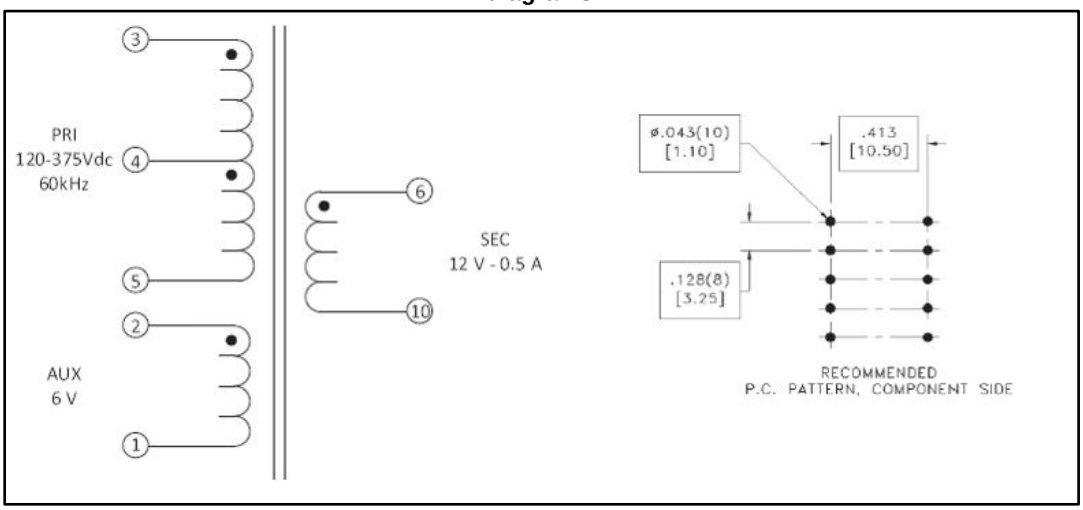
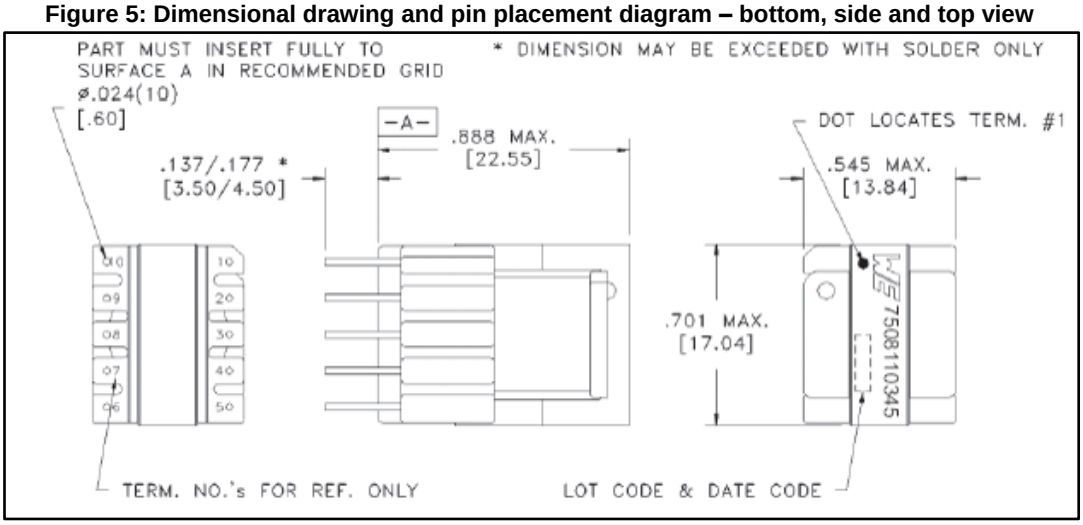


Figure 5: Dimensional drawing and pin placement diagram – bottom, side and top view



2 Performance data

2.1 Output voltage characteristics

The STEVAL-ISA197V1 output voltage has been measured in different line and load conditions.

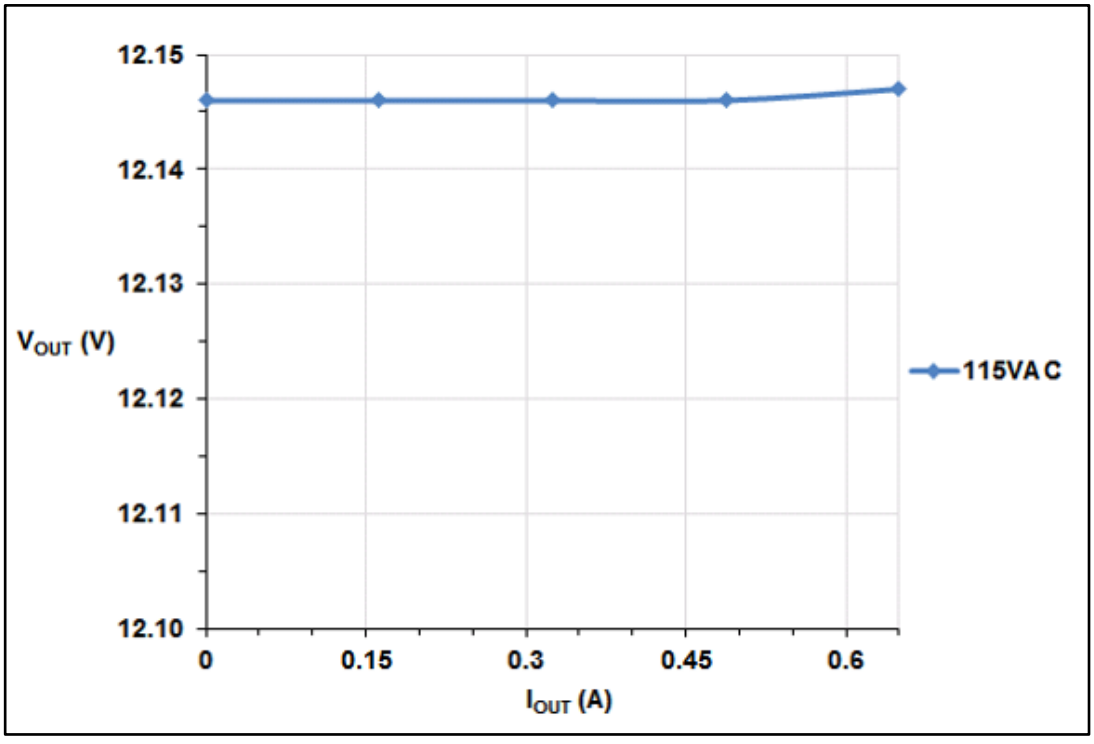
The table below shows measurement results: the output voltage variation is negligible versus the load and line variation.

As the output voltage is little affected by line variations, *Figure 6: "Output voltage load regulation at 115 V_{AC}"* just shows the load regulation at 115 V_{AC}.

Table 4: Output voltage line-load regulation

V_{IN} [V_{AC}]	V_{OUT} (V)				
	No load	**0.163 A**	**0.325 A**	**0.488 A**	**0.65 A**
90	12.147	12.147	12.147	12.147	12.147
115	12.146	12.146	12.146	12.146	12.147
150	12.146	12.146	12.146	12.146	12.146
180	12.145	12.145	12.146	12.146	12.146
230	12.145	12.145	12.145	12.145	12.145
265	12.145	12.146	12.145	12.145	12.145

Figure 6: Output voltage load regulation at 115 V_{AC}



2.2 Efficiency measurements

Any external power supply (EPS) must be capable of meeting the international regulation agency limits. The European code of conduct (EC CoC version 5) limit is taken as a reference.

Since this power supply is considered a no-low voltage power supply, the formula to calculate the minimum average efficiency is:

Table 5: EC CoC version 5 energy-efficiency criteria for active mode (excluding low voltage external power supplies), Tier 2

Nameplate output power (Pno)	Minimum average efficiency (expressed as a decimal)
0 to ≤ 1 watt	≥ 0.5 *Pno + 0.169
> 1 to ≤ 49 watts	≥ [0.071* ln (Pno)] - 0.00115*Pno + 0.670
> 49 watts	≥ 0.890

According to the above table, the minimum average efficiency is 80.7%, measured as the average of the efficiencies at 25%, 50%, 75% and 100% of the rated output power at nominal input voltages (V_{IN} = 115 V_{AC} and V_{IN} = 230 V_{AC}).

Another requirement is the efficiency measured at 10% of the rated output power, according to the below table:

Table 6: EC CoC version 5 energy-efficiency criteria for active mode (excluding low voltage external power supplies) at 10% maximum output load, Tier 2

Nameplate output power (Pno)	Minimum average efficiency (expressed as a decimal)
0 to ≤ 1 watt	≥ 0.5 *Pno + 0.060
> 1 to ≤ 49 watts	≥ [0.071 * ln (Pno)] – 0.00115 * Pno + 0.570
> 49 watts	≥ 0.790

For the considered application the minimum efficiency is 70.7%.

Table 7: "Average efficiency at 115 V_{AC}" and *Table 8: "Average efficiency at 230 V_{AC}"* show all the efficiency measurement results.

Table 7: Average efficiency at 115 V_{AC}

% load	I_{OUT} (A)	V_{OUT} (V)	P_{IN} (W)	P_{OUT} (W)	Efficiency (%)
25%	0.163	12.146	2.341	1.974	84.31
50%	0.325	12.146	4.683	3.947	84.29
75%	0.488	12.146	7.066	5.921	83.80
100%	0.650	12.147	9.532	7.896	82.83
Average efficiency					**83.81**

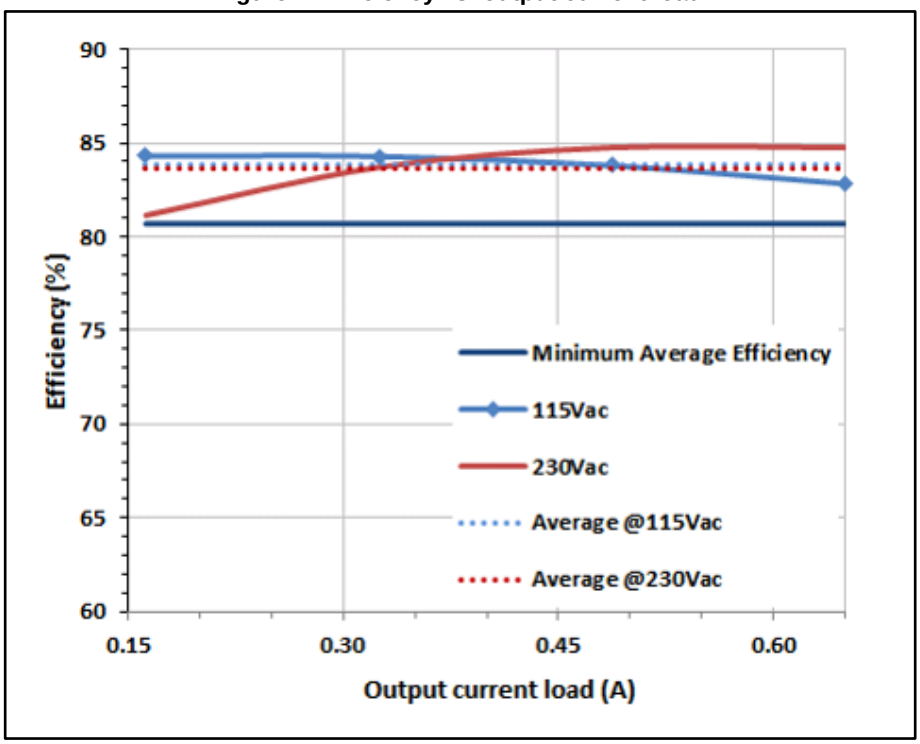
Table 8: Average efficiency at 230 V_{AC}

% load	I_{OUT} (A)	V_{OUT} (V)	P_{IN} (W)	P_{OUT} (W)	Efficiency (%)
25%	0.163	12.145	2.432	1.974	81.15
50%	0.325	12.145	4.715	3.947	83.71
75%	0.488	12.145	6.985	5.921	84.76
100%	0.650	12.145	9.313	7.894	84.77
Average efficiency					**83.60**

Table 9: Average efficiency at 10% of the max. output load

V_{IN} [V_{AC}]	I_{OUT} (A)	V_{OUT} (V)	P_{IN} (W)	P_{OUT} (W)	Efficiency (%)
115	0.065	12.146	0.991	0.789	**79.70**
230	0.065	12.145	1.095	0.789	**72.09**

Figure 7: Efficiency vs. output current load



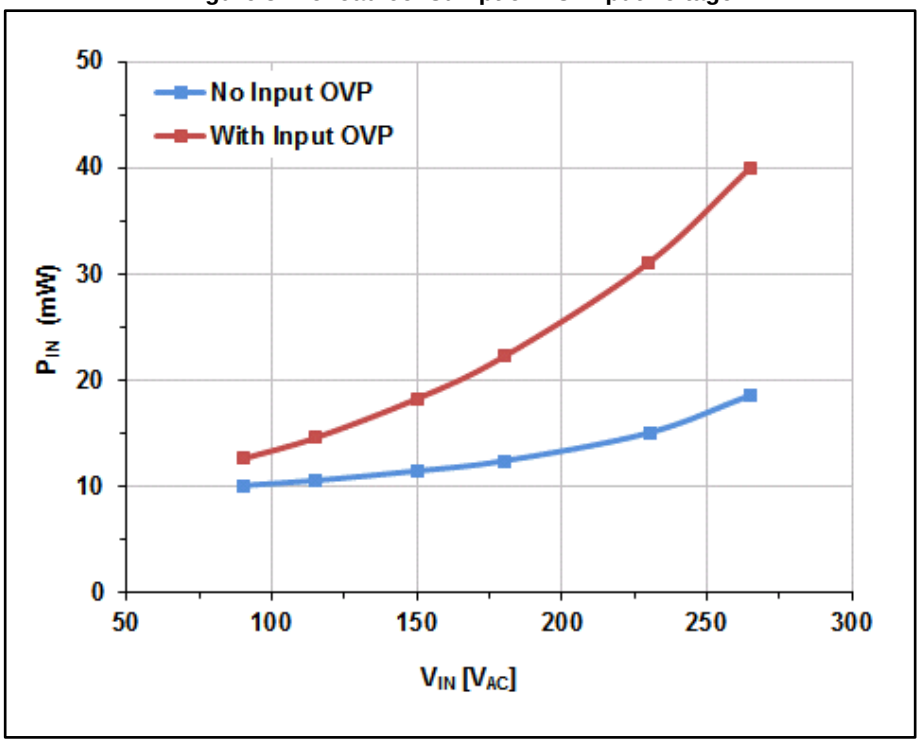
2.3 No load consumption

The converter input power has been measured at no load: in this condition the converter works in burst mode so that the average switching frequency is reduced, thus minimizing the frequency related losses.

Measurements have been performed both with the input OVP protection disabled (DIS pin connected to ground) and with the resistor divider connected to DIS pin (R1=R2=R3=2.2 MΩ, R4=18.7 kΩ and C6=1 nF).

The presence of the input OVP resistor divider, to sense the flyback input voltage when the protection is enabled, does not affect the average switching frequency but does affect the input power due to the power dissipated in the resistor divider itself.

Figure 8: No load consumption vs. input voltage



2.4 Light load consumption

Although the EC CoC has no other requirement regarding the light load performance, we also show the STEVAL-ISA197V1 evaluation board input power at light load to give quite complete information.

In particular, to be compliant with EuP Lot 6, the EPS requires an efficiency higher than 50% when the output load is 250 mW. Such measurements have been performed with the input OVP both enabled and disabled and shows how the evaluation board also meets this requirement.

Figure 9: Light load consumption at different output power - Input OVP disabled

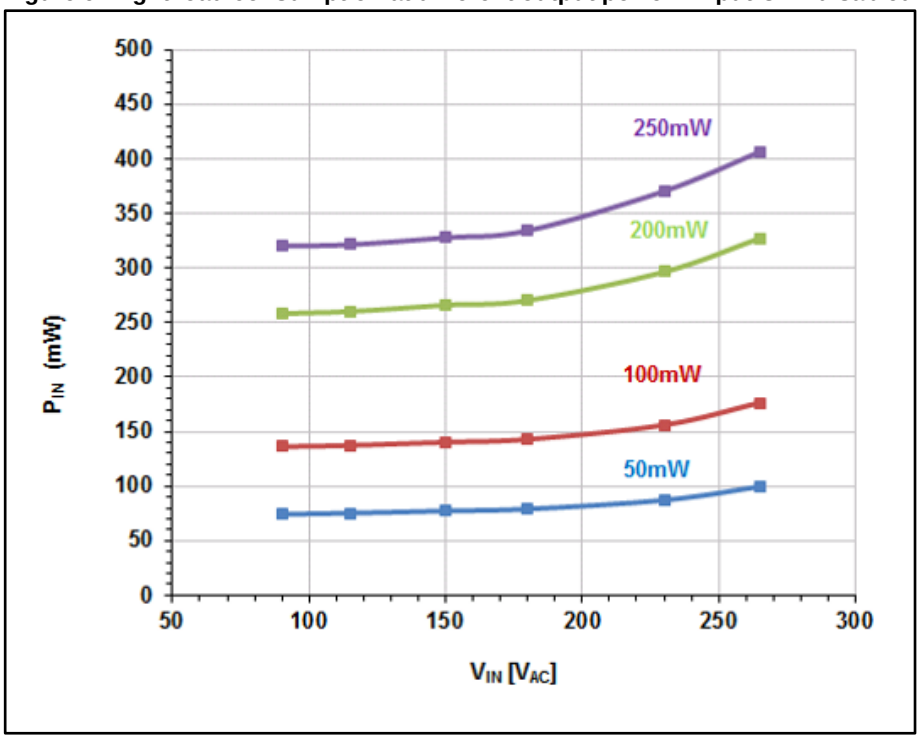
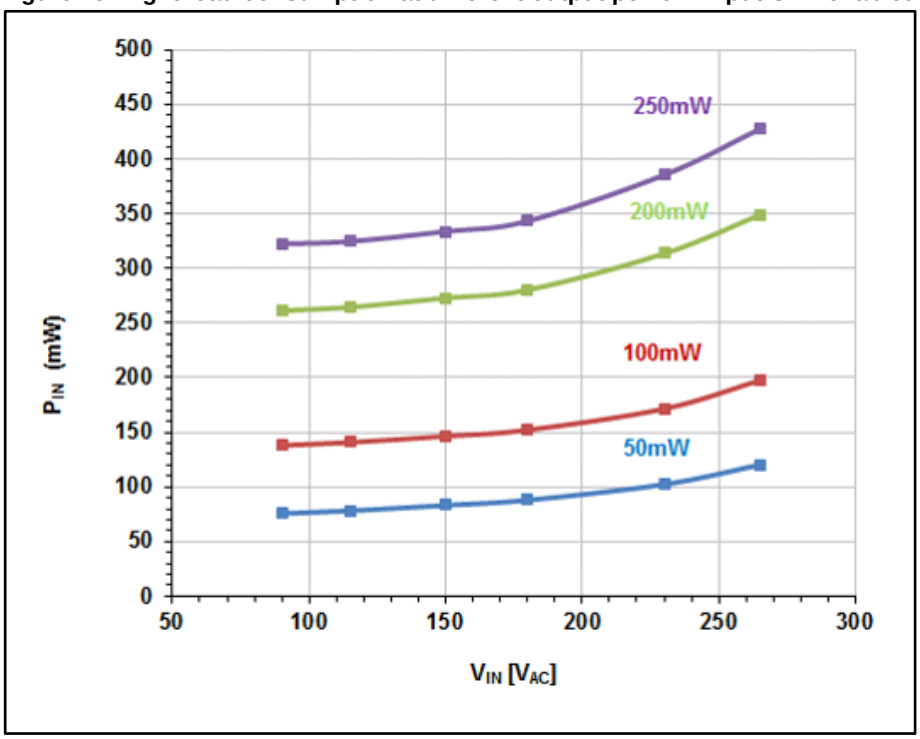


Figure 10: Light load consumption at different output power - Input OVP enabled



3 Typical waveforms

Figure 11: "Drain current and voltage at full load at 90 V_{AC}" and *Figure 12: "Drain current and voltage at full load at 265 V_{AC}"* show the drain voltage and current waveforms at full load condition for the minimum and maximum input voltage, whereas *Figure 13: "Drain current and voltage at full load at 115 V_{AC}"* and *Figure 14: "Drain current and voltage at full load at 230 V_{AC}"* show the two nominal input voltages.

Figure 11: Drain current and voltage at full load at 90 V_{AC}

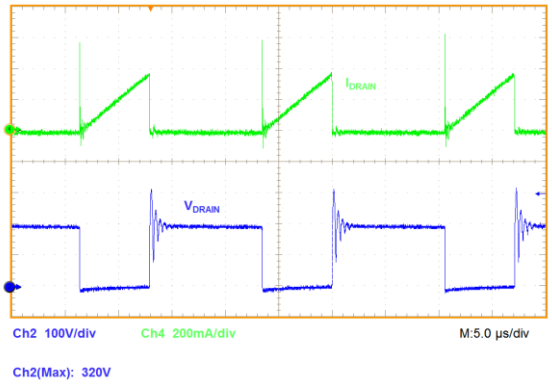


Figure 12: Drain current and voltage at full load at 265 V_{AC}

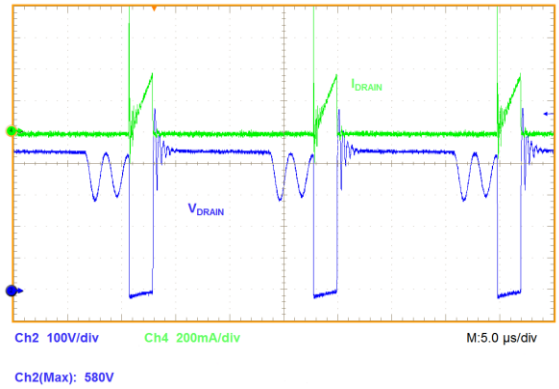


Figure 13: Drain current and voltage at full load at 115 V_{AC}

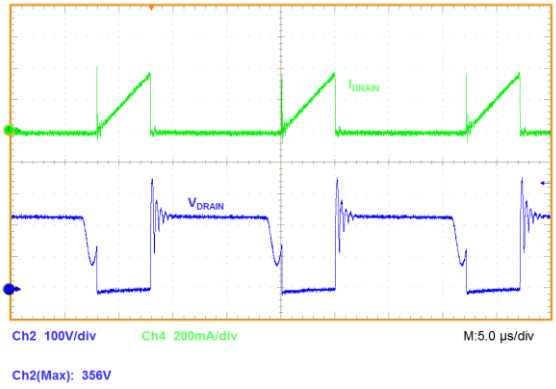
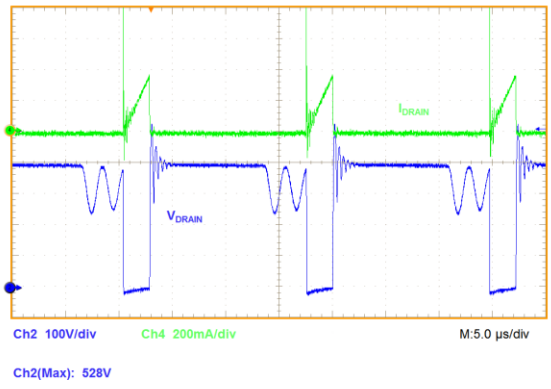


Figure 14: Drain current and voltage at full load at 230 V_{AC}



The output ripple at the switching frequency was also measured.

The board is equipped with an LC filter to further reduce the ripple without reducing the overall output ESR capacitor.

Furthermore, the voltage ripple across the output connector (V_{OUT}) and before the LC filter (V_{OUT_PRE}) was measured to verify the effectiveness of the LC filter, as shown in the following pictures.

Figure 15: Output voltage ripple at full load at 115 V_{AC}

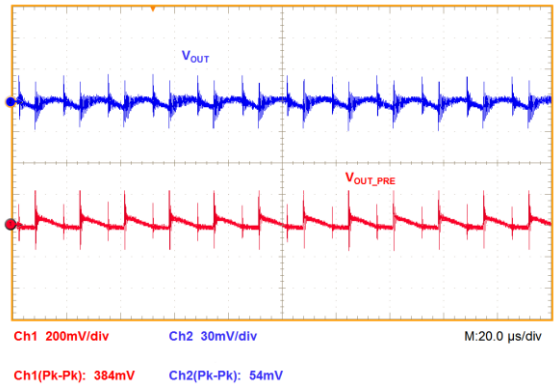
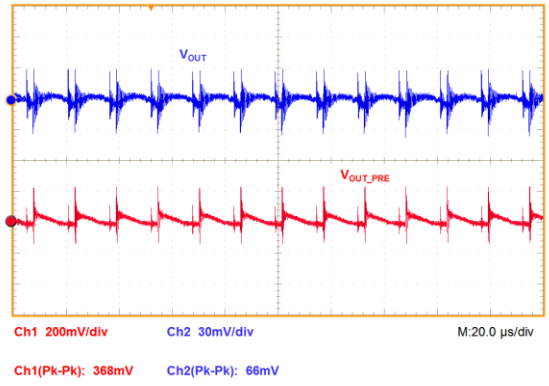


Figure 16: Output voltage ripple at full load at 230 V_{AC}



3.1 Dynamic step load regulation

In any power supply, it is important to measure the output voltage when the converter is submitted to dynamic load variations to ensure good stability and no overvoltage or undervoltage occurs.

The test has been performed by varying the output load from 0 to 0.65 A (100% of the nominal value) for both nominal input voltages.

In any tested condition, no abnormal oscillations were noticed on the output and over/under shoot were well within acceptable values.

Figure 17: Dynamic step load (I_{OUT} from 0 to 0.65 A) at 115 V_{AC}

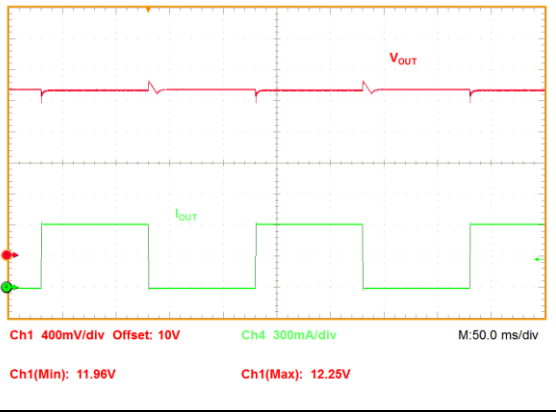
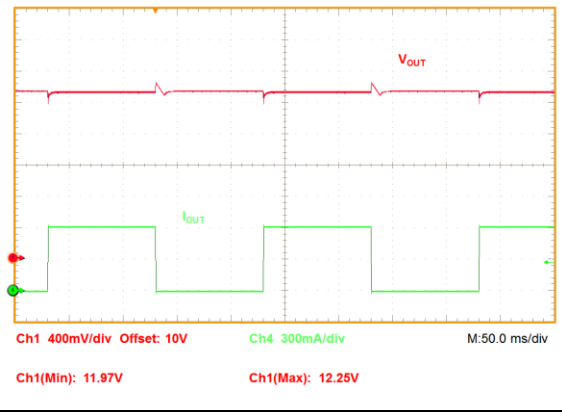


Figure 18: Dynamic step load (I_{OUT} from 0 to 0.65 A) at 230 V_{AC}



4 Soft-start

When the converter starts, the output capacitor is discharged and needs some time to reach the steady state condition. During this time, the power demand from the control loop is the maximum, while the reflected voltage is low; these two conditions could lead to the converter deep continuous operating mode.

In addition, when the MOSFET is switched on, it cannot immediately be switched off as the minimum on-time (T_{ON_MIN}) has to be elapsed.

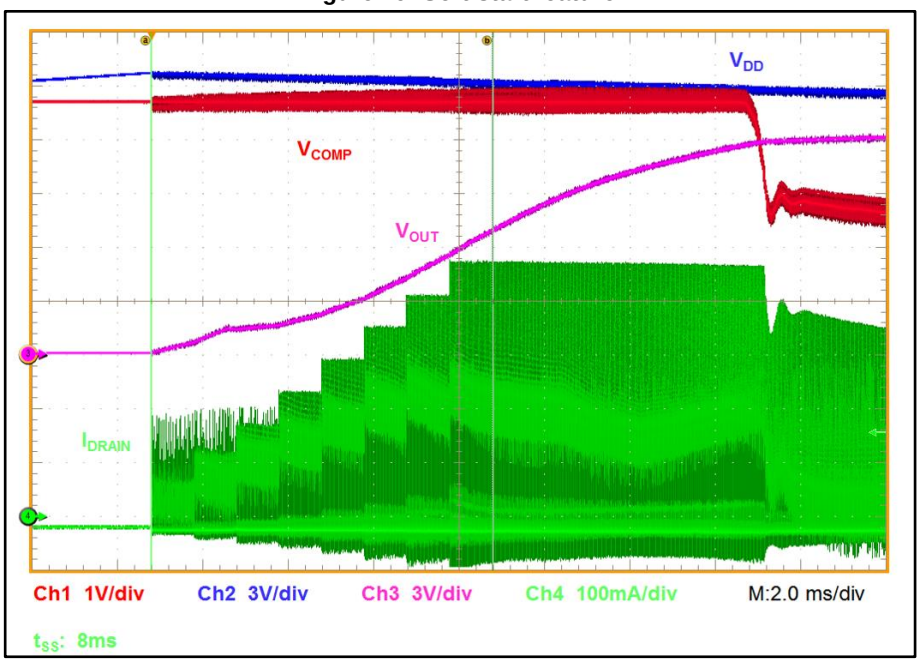
Because of the converter deep continuous working mode, during this T_{ON_MIN}, an excess of drain current can overstress the converter component as well as the device itself, the output diode and the transformer. Transformer saturation is also possible under these conditions.

To avoid all this, the VIPer11 implements an internal soft-start feature. As the device starts to work, regardless of the control loop request, the drain current is allowed to gradually increase from zero to the maximum value.

The drain current limit is increased by steps and the values range from 0 to the drain current limitation value (I_{DLIM}) in eight steps. The soft-start time, t_{SS}, is internally set at 8 ms.

The figure below shows the converter soft-start phase when operating at the minimum line voltage and maximum load.

Figure 19: Soft-start feature



5 Protection features

To increase end-product safety and reliability, VIPer11 has some protection features: overload protection, pulse skip mode, max. duty cycle counter protection and input/output overvoltage protection.

In the following sections, these protections are tested and the results shown.

5.1 Overload and short-circuit protection

When the load power demand increases, the feedback loop reacts by increasing the voltage on pin: the PWM current set point increases and the power delivered to the output rises. This process ends when the delivered power equals the load power request.

In case of overload or output short-circuit (see *Figure 20: "Overload event- OLP triggering"*), the drain current value reaches the I_{DLIM}.

In every cycle this condition is met, an internal OCP counter is incremented; if this overload condition is continuously maintained for the time t_{OVL} (50 ms typical), the protection is tripped (see *Figure 20: "Overload event- OLP triggering"*), the power section is turned off and the converter is disabled for a $t_{RESTART}$ time (1 s typical).

After this elapses, the IC resumes switching and, if the fault condition is still present, the protection occurs indefinitely in the same way (*Figure 21: "Overload event- continuous overload"*). This ensures the converter to restart attempts with low repetition rate to make it work safely with extremely low power throughput and avoiding the IC overheating in case of repeated overload events.

Furthermore, at startup, after any protection tripping, the internal soft-start function is invoked (*Figure 22: "Overload event- t_{SS} and t_{OVL}"*) to reduce the stress on the secondary diode.

After the fault removal, the IC resumes working normally. If the fault is removed during t_{SS} or t_{OVL}, before the protection tripping, the counter is decremented on a cycle-by-cycle basis down to zero and the protection is not tripped.

If the short-circuit is removed during $t_{RESTART}$, the IC has to wait for the $t_{RESTART}$ to elapse before resuming to switch (*Figure 23: "Overload event- fault removed and autorestart"*).

Figure 20: Overload event- OLP triggering

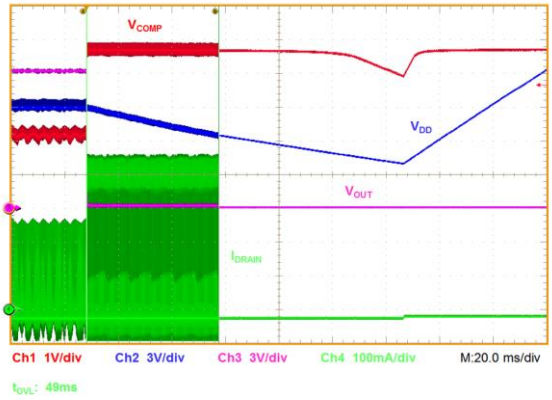


Figure 21: Overload event- continuous overload

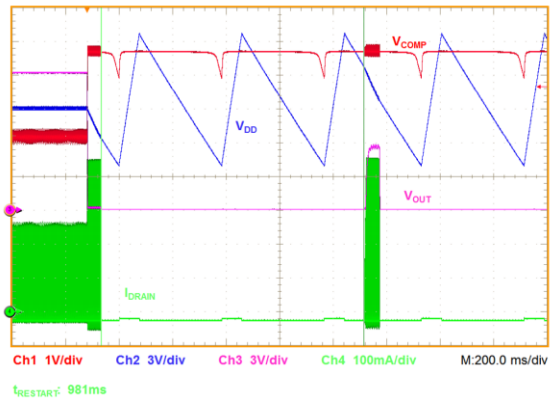


Figure 22: Overload event- t_{SS} and t_{OVL}

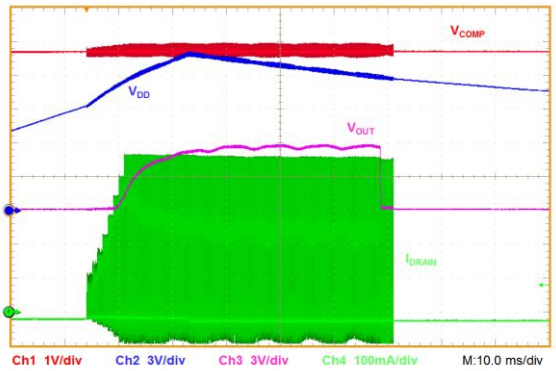
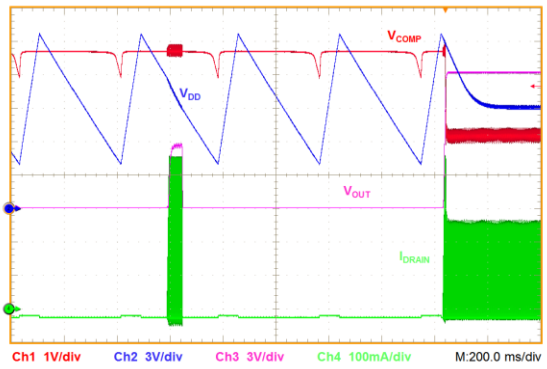


Figure 23: Overload event- fault removed and autorestart



5.2 Pulse skip mode

Any time the drain peak current (I_{DRAIN}) exceeds I_{DLIM} within the minimum on-time (T_{ON_MIN}), a switching cycle is skipped.

The check is made on a cycle-by-cycle basis and the cycles can be skipped until the minimum switching frequency F_{OSC_MIN} (15 kHz, typical) is reached.

If the above condition is indefinitely met, as the internal OCP counter reaches its end-of-count, the IC is stopped for $t_{RESTART}$ (1s, typical) and activated again via the soft-start phase.

Any time I_{DRAIN} does not exceed I_{DLIM} within T_{ON_MIN}, a switching cycle is restored. The check is made on a cycle-by-cycle basis and the cycles can be restored until the nominal switching frequency F_{OSC} is reached.

Providing, when needed, an inductor discharge time longer than the one allowed at the nominal switching frequency, the protection helps to limit the “flux runaway” effect, often present at converter startup: the primary MOSFET, charged during the minimum on-time through the input voltage, cannot discharge the same amount during the off-time, due to the fact that the output voltage is very low.

The result is a definite increase of average inductor current that can dangerously reach high values until the output capacitor is not charged enough to ensure the inductor discharge rate needed for the volt second balance.

At startup at 265 V_{AC} (input voltage), during the first switching cycle, the drain current reaches its limitation during the T_{ON_MIN} then the switching frequency is halved until reaching the minimum switching frequency (15 kHz). Any time the drain current is below the current limitation (within the minimum on-time), the switching frequency increases until the nominal value F_{OSC} is reached (see figures below).

Figure 24: Startup at 265 V_{AC}- full load

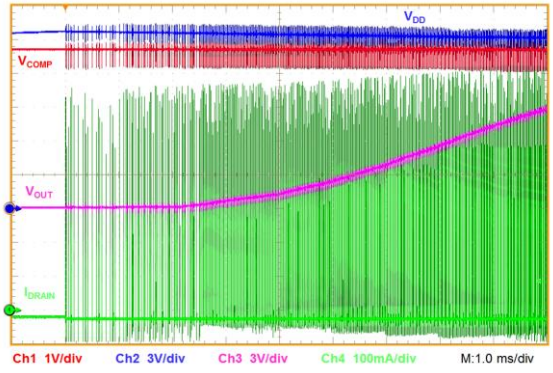
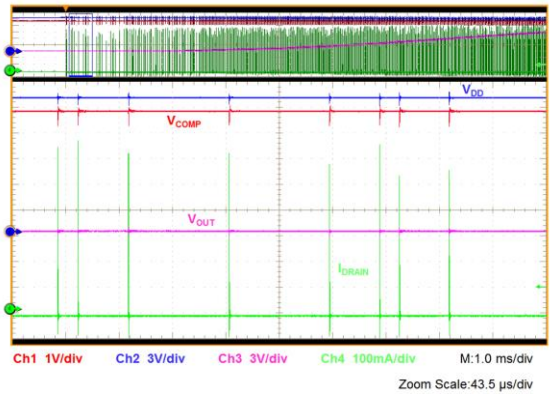


Figure 25: Startup at 265 V_{AC}- full load magnification



5.3 Max. duty cycle counter protection

The IC embeds a max. duty cycle counter which disables the PWM if the MOSFET is turned off by the max. duty cycle (70% min, 80% max) for ten consecutive switching cycles.

After the protection tripping, the PWM is disabled for $t_{RESTART}$ and then reactivated via the soft-start phase until the fault condition is removed.

In some cases (i.e., breaking of the loop at low input voltage) even if V_{COMP} is saturated high, the OLP cannot be triggered because at every switching cycle the PWM is turned off by the maximum duty cycle before the drain peak current reaches I_{DLIM}.

As a result, the output voltage V_{OUT} could increase out of control and be maintained indefinitely at a much higher value than the nominal one with a risk for the output capacitor, the output diode and the IC itself.

The max. duty cycle counter protection prevents this kind of failures.

To test this protection, heavy load and low input voltage have been selected. The IC is protected in auto-restart mode for $t_{RESTART}$ (1 s typical), then tries to start up via the soft-start phase until the fault condition is removed (*Figure 26: "Shutdown by max. duty cycle counter - first tripping and restart"* and *Figure 27: "Shutdown by max. duty cycle counter - steady state"*).

Figure 28: "Shutdown by max. duty cycle counter - ten consecutive switching cycles" highlights the ten cycles causing the protection intervention.

Figure 26: Shutdown by max. duty cycle counter - first tripping and restart

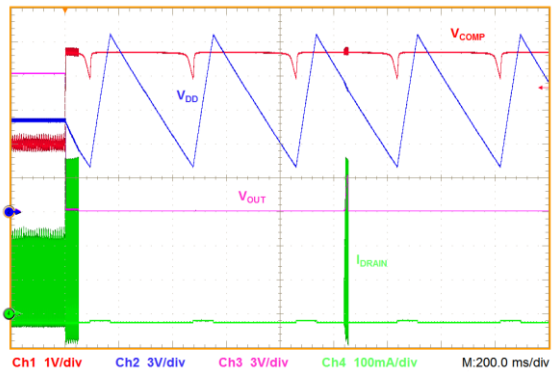


Figure 27: Shutdown by max. duty cycle counter - steady state

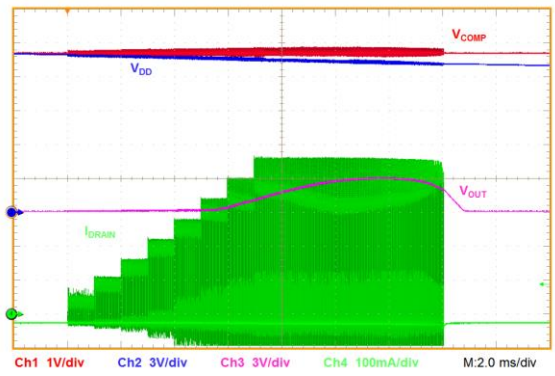
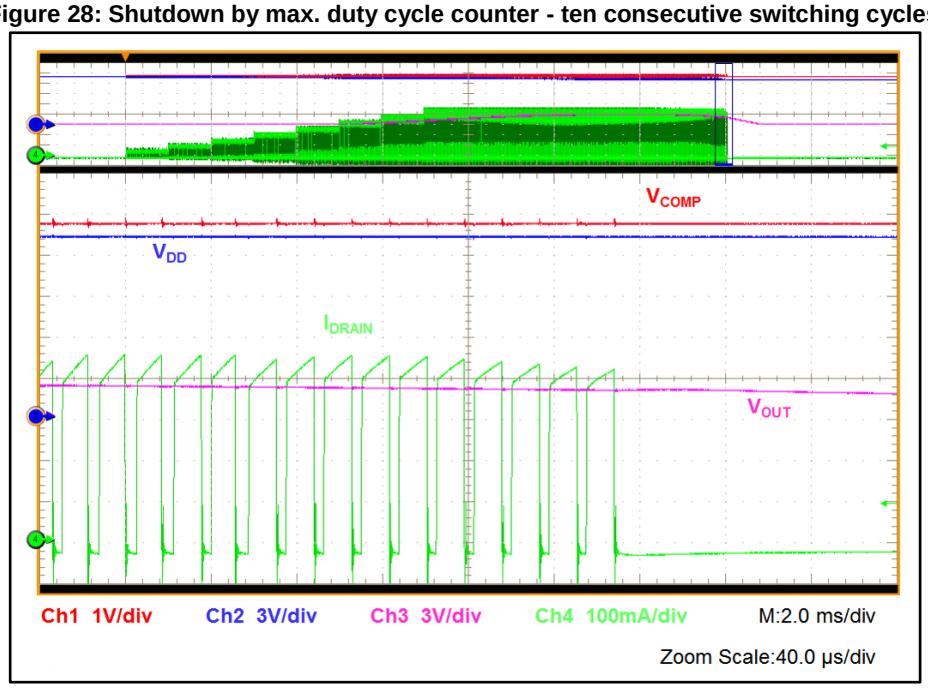


Figure 28: Shutdown by max. duty cycle counter - ten consecutive switching cycles



5.4 Input overvoltage protection

When the voltage across the DIS pin is externally pulled above the internal threshold V_{DIS_th} (1.2 V typical) for more than t_{DEB} (for instance, by means of a voltage divider connected to some higher voltage), the PWM is disabled and enters the auto-restart mode for $t_{DIS\_RESTART}$ (500 ms typical). This allows an input overvoltage protection to be easily realized, just connecting a voltage divider from the rectifier input mains to the DIS pin.

The resistors R1, R2, R3 and R4 (see *Section 1.1: "Schematic diagram"*) can be used for this purpose.

The resistor values are selected according to the following formula:

$$R1 + R2 + R3 = \left(\frac{V_{OVP}}{V_{DIS\_th}} - 1\right) \cdot R4$$

where V_{OVP} is the desired input overvoltage threshold.

The additional steady state power consumption of this network is:

$$P_{DIS}(V_{INdc}) = \frac{(V_{INdc} - V_{DIS})^2}{R1 + R2 + R3} + \frac{{V_{DIS}}^2}{R4}$$

If the Disable function is not required, the DIS pin must be connected to GND (this is the default setting for the STEVAL-ISA197V1 evaluation board, which excludes the function).

For example, if R1=R2=R3=2.2 MΩ and R4=18.7 kΩ (C6=1 nF), the input overvoltage will be set at about 423 V_{DC}. As the input capacitor voltage range is 400 V_{DC} to check the effectiveness of the protection, C1 and C2 have been replaced by others with higher voltage range (450 V_{DC}).

The following figures show some relevant input overvoltage protection waveforms created via the DIS pin.

Figure 29: Input OVP - triggering

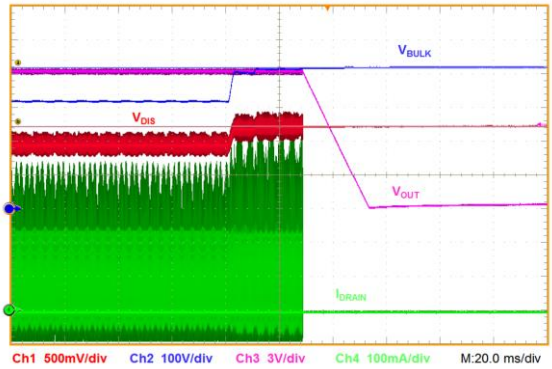


Figure 30: Input OVP - steady state

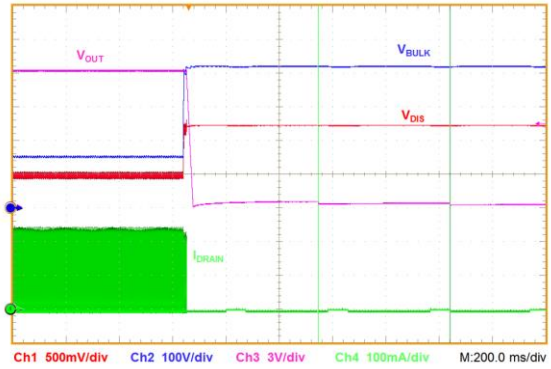


Figure 31: Input OVP - debounce time

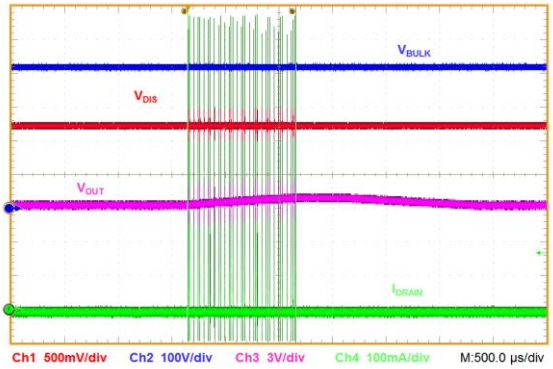
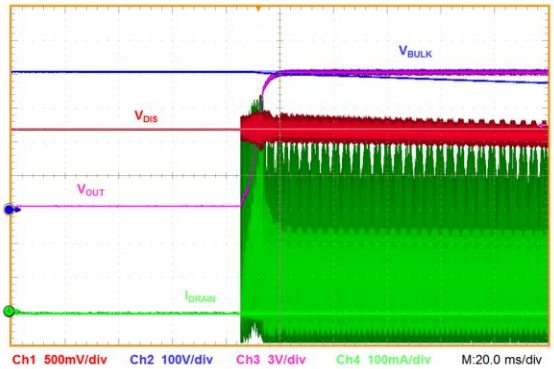


Figure 32: Input OVP - removed



6 Conducted noise measurements

The VIPer114LS frequency jittering feature allows the spectrum to be spread over frequency bands, rather than being concentrated on a single frequency value. Especially when measuring conducted emissions with the average detection method, the level reduction can be several dBµV.

A pre-compliance test for the EN55022 (Class B) European normative was performed and average measurements of the conducted noise emissions at full load and nominal mains voltages are shown in the following figures.

In all test conditions, there is a good margin between the measurements and the corresponding limits.

Figure 33: CE average measurement at 115 V_{AC} full load

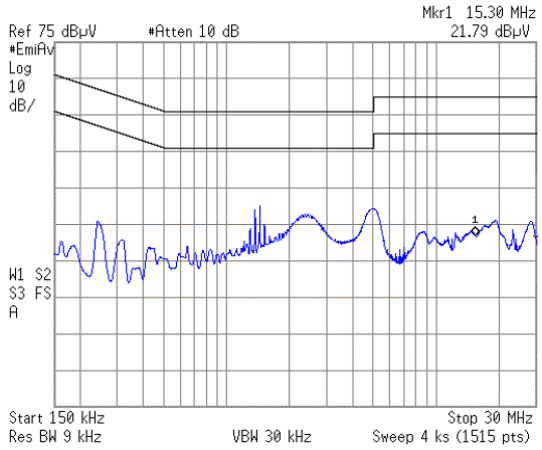
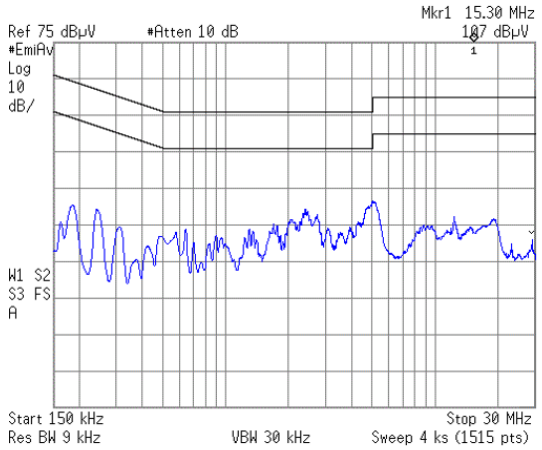


Figure 34: CE average measurement at 230 V_{AC} full load



7 Thermal tests

A thermal analysis of the board was performed using an IR camera, under full load condition, at the two nominal input voltages (115 V_{AC} and 230 V_{AC}).

The results are shown in the following figures and summarized in the table below.

Figure 35: Thermal map at 115 V_{AC} full load (top layer)

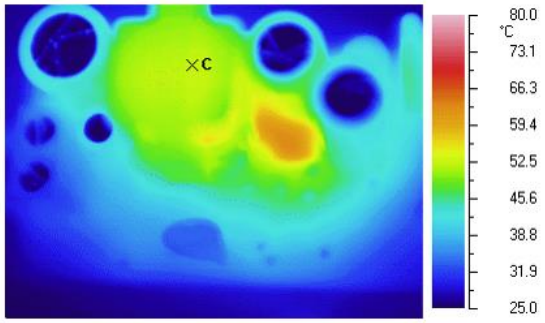


Figure 36: Thermal map at 115 V_{AC} full load (bottom layer)

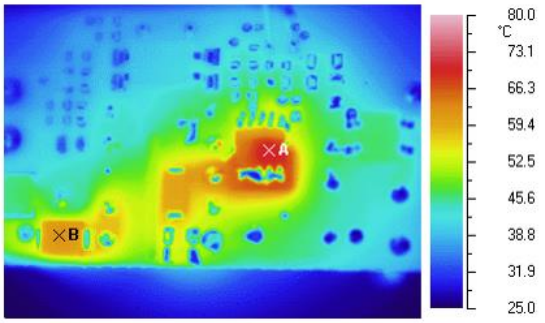


Figure 37: Thermal map at 230 V_{AC} full load (top layer)

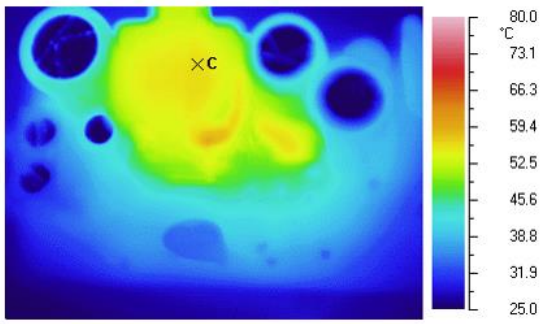


Figure 38: Thermal map at 230 V_{AC} full load (bottom layer)

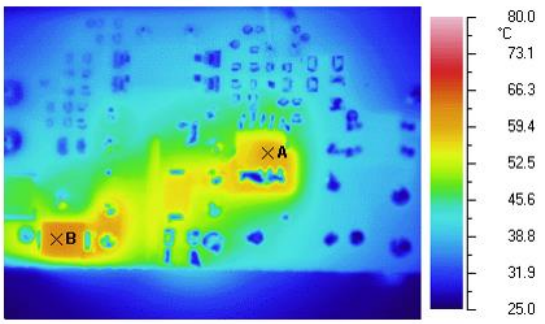


Table 10: Temperature of the key components (T_{AMB} = 25 °C, emissivity = 0.95 for all points)

Point	Temperature (°C)		Reference
	115 V_{AC}	230 V_{AC}	
A	71	60	VIPer114LS
B	62	63	Output diode
C	54	58	Transformer

8 Conclusions

A flyback converter has been described and characterized. Efficiency and low load performance have been highlighted and the bench results were good with very low input power under light load condition.

The efficiency performance has been compared with the requirements of the EC CoC and DoE regulation programs for external AC/DC adapters with highly positive results, where the measured active mode efficiency is always higher than the required minimum. Also, the EMI emissions are quite low, even if a low cost input filter has been used.

9 Evaluation board tools and documentation

The VIPer114LS evaluation board order code is STEVAL-ISA197V1.

Further information about this product is available in the VIPER11 datasheet at www.st.com.

10 Revision history

Table 11: Document revision history

Date	Version	Changes
24-Jul-2017	1	Initial release

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