STEVAL-ISA196V1: VIPer11 5V/1.2A non-isolated flyback

Introduction

The STEVAL-ISA196V1 evaluation board implements a flyback converter (5 V / 1.2 A) wide range mains developed for general purpose applications.

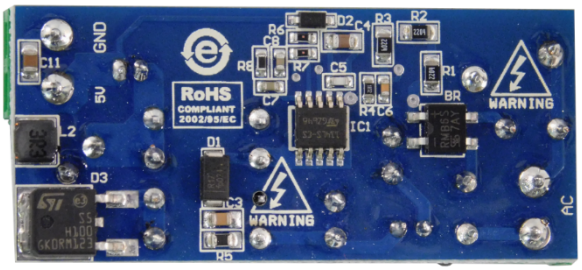
The core of the application is the VIPer11, a new off-line high voltage converter from the VIPerPlus family.

The device is a high-voltage converter that intelligently integrates an 800 V rugged power MOSFET with PWM current-mode control.

The main characteristics of the evaluation board are its single layer, small size and minimal BOM, high efficiency and low standby consumption.

Figure 1. STEVAL-ISA196V1: top view

Figure 2. STEVAL-ISA196V1: bottom view



1 Board and device features

1.1 STEVAL-ISA196V1 features

- Five-star energy efficient rating under no-load operation ($P_{IN\_no\_load}$ < 10 mW @ 230 V_{AC})
- Compliant with the 10% load efficiency prescribed by the European CoC ver. 5
- Active mode efficiency: > 78% (CoC ver. 5 target = 75%)
- Consumes less than 400 mW @ 230 V_{AC} with 250 mW load
- Compliant with IEC55022 Class B conducted EMI, even with reduced EMI filter
- Input overvoltage protection
- RoHS compliant

1.2 STEVAL-ISA196V1 electrical specifications

Table 1. STEVAL-ISA196V1 electrical specifications

Parameter	Symbol	Value
Input voltage range	V_{IN}	85 V_{AC}; 265 V_{AC}
Output voltage 1	V_{OUT}	5 V
Max output current	I_{OUT}	1.2 A
Output power	P_{OUT}	6 W
Precision of output regulation	ΔV_{OUT}	±5 %
High-frequency output 1 voltage ripple	ΔV_{OUT}	50 mV
Max ambient operating temperature	T_{AMB}	60 °C
Switching frequency	F_{OSC}	60 kHz

1.3 VIPer features

- 800 V avalanche-rugged power MOSFET
- Embedded HV startup and sense-FET
- Current mode PWM controller
- Wide supply voltage range: 4.5 V to 30 V
- Pulse frequency modulation (PFM) and ultra-low standby consumption of the internal circuitry under light-load condition
- 60 kHz fixed switching frequency with jittering
- Embedded E/A with 1.2 V reference
- Protections with automatic restart: overload/short-circuit (OLP), line or output OVP, max. duty cycle counter, V_{CC} clamp
- Pulse-skip mode to prevent flux-runaway
- Embedded thermal shutdown
- Built-in soft-start for improved system reliability

2 Circuit description

The power supply is set in non-isolated flyback topology. The input section includes resistor R1 for inrush current limitation, diode D1 and filter (L1, L2, C1, C2) for EMC suppression.

The FB pin is the inverting input of an error amplifier and an accurate 1.2 V voltage reference with respect to GND. This allows the setting and tight regulation of the output voltage through a voltage divider connected directly to the output terminal, according to the following formula:

$$V_{OUT} = 1.2V \cdot \left(1 + \frac{R6}{R7}\right) \quad (1)$$

The C-R-C network from COMP (the output of the error amplifier) to the GND pin provides frequency compensation to the feedback loop that regulates the output voltage.

During power-up, as V_{DRAIN} exceeds $V_{HVSTART}$, the internal HV current source charges the C4 V_{CC} capacitor to V_{CCon}; then the Power MOSFET starts switching, the HV current source is turned off and the IC is powered by C4.

Resistors R1, R2, R3 and R4 form a voltage divider from the rectified input mains to the DIS pin, which can be used to perform input overvoltage protection. By default, R1, R2 and R3 are not mounted and R4 = 0 Ω in order to minimize the input power consumption during no load and light load. If input UVP is required, R1, R2, R3 and R4 should be selected as indicated in Section 5.6 Input overvoltage protection.

The IC can be supplied by connecting the small signal diode D3 between the output terminal and the VCC pin. In fact, considering that V_{OUT} = 5 V and the maximum value of V_{CSon} is 4.5 V (from the VIPer11 datasheet), the HV current source is never activated. The low consumption of the IC internal blocks allows very low input power consumption in no-load condition (less than 10 mW @ 230 V_{AC}) even without the auxiliary winding of the transformer.

2.1 Bill of materials

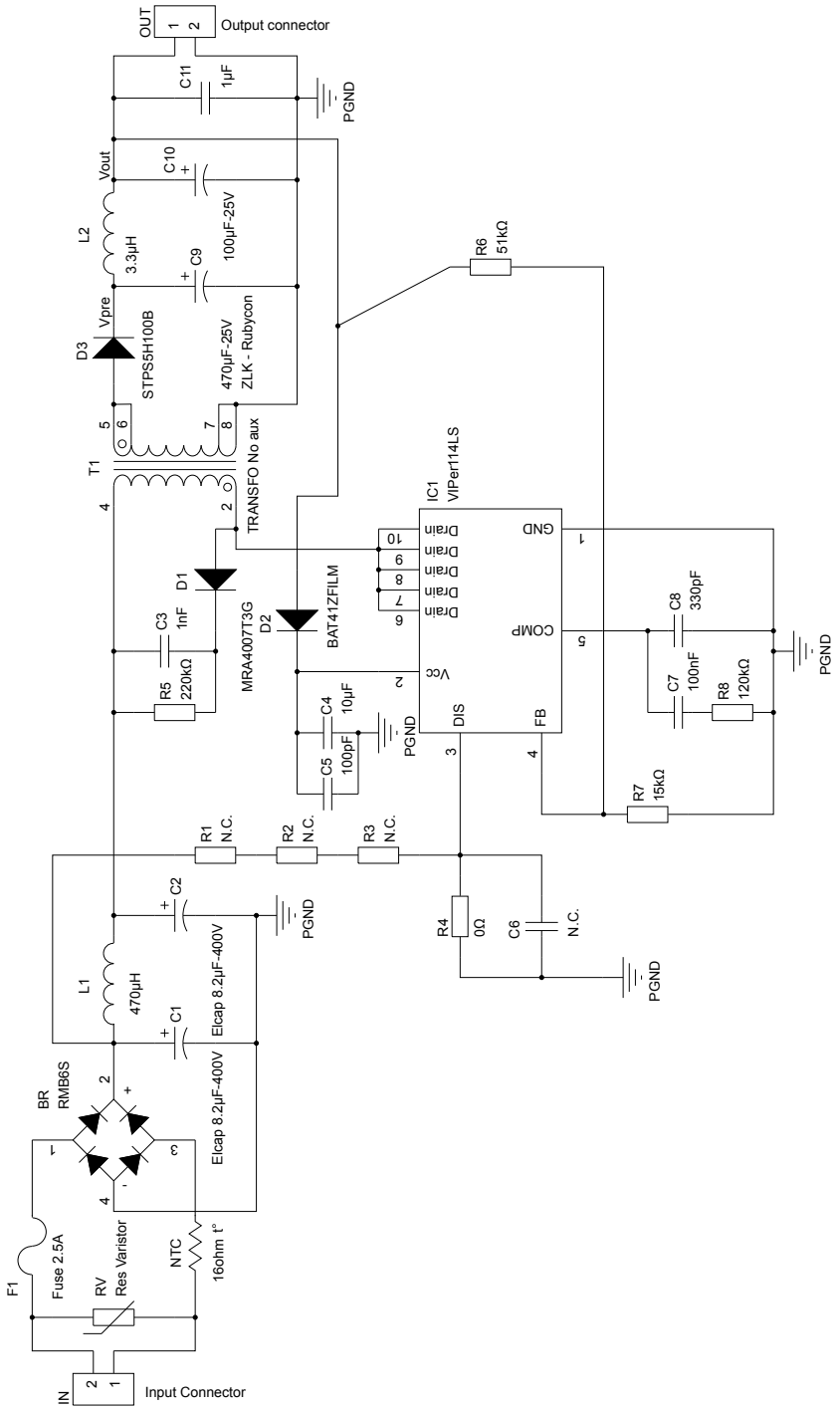
Table 2. STEVAL-ISA196V1 bill of materials

Item	Q.ty	Ref.	Part/value	Description	Manufacturer	Order code
1	1	IN		Input connector	TE Connectivity	282837-2
2	1	OUT		Output connector	TE Connectivity	282837-2
3	1	RV		MOV	EPCOS	B72210S0321K101
4	1	BR	MBS	Bridge rectifier	Taiwan Semiconductor	RMB6S
5	1	F1	2.5 A	Fuse	Eaton	SS-5H-2.5A-BK
6	1	NTC	16 Ω		EPCOS	B57236S160M
7	0	R1	0805	not mounted		
8	0	R2	0805	not mounted		
9	0	R3	0805	not mounted		
10	1	R4	0 Ω 0603	Resistor		
11	1	R5	220 kΩ±1% - 0.5 W 0805	Resistor	Panasonic	ERJP6WF2203V
12	1	R6	51 kΩ±1% - 0.1 W 0603	Resistor	Panasonic	ERJU03F5102V
13	1	R7	15 kΩ±1% - 0.1 W 0603	Resistor	Panasonic	ERJU03F1502V

Item	Q.ty	Ref.	Part/value	Description	Manufacturer	Order code
14	1	R8	120 kΩ±1% - 0.1 W 0603	Resistor	Vishay	CRCW0603120KFKEA
15	2	C1, C2	8.2 µF-400 V, Ø8 mm - p3.5 mm - h 16 mm	Elocrtolytic capacitors	Rubycon	400AX8R2MEFC8X16
16	1	C3	1 nF-1000 V 0805	MLCC capacitor	Kemet	C0805X102KDRACTU
17	1	C4	10 µF-35 V 0805	MLCC capacitor	TDK	C2012X5R1V106K085AC
18	1	C5	100 pF-50 V 0603	MLCC capacitor	Wurth Elektronik	885012206077
19	0	C6	0603	not mounted		
20	1	C7	100 nF - 50 V 0603	MLCC capacitor	Yageo	CC0603KRX7R9BB104
21	1	C8	330 pF - 50 V 0603	MLCC capacitor	Murata	GCM1885C1H331JA16D
22	1	C9	470 µF-25 V Ø8 mm - p3.5 mm - h20 mm	Elocrtolytic capacitor	Rubycon	25ZLK470M8X20
23	1	C10	100 µF-25 V Ø5 mm - p2 mm - h 11 mm	Elocrtolytic capacitor	Rubycon	25YXJ100M5X11
24	1	C11	1 µF-25 V 0805	MLCC capacitor	Murata	GRM21BR71E105KA99L
25	1	D1	1 A-1000 V SMA	General purpose diode	ON Semiconductor	MRA4007T3G
26	1	D2	0.2 A-100 V SOD-123	Signal Schottky	STMicroelectronics	BAT41ZFILM
27	1	D3	5 A-100 V DPAK	Power Schottky	STMicroelectronics	STPS5H100B
28	1	L1	470 µH XS Ø6 mm - h8.5 mm		Wurth Elektronik	7447462471
29	1	L2	3.3 µH (4x4) mm		Wurth Elektronik	74404042033
30	1	IC1	SSO10	Offline HV converter	STMicroelectronics	VIPer114LS
31	1	T1	EE13/7/6	Flyback transformer	Wurth Elektronik	750810014 (rev00)

2.2 Schematic diagram

Figure 3. **STEVAL-ISA196V1 circuit schematic**



3 Transformer

Table 3. Transformer electrical characteristics

Parameter	Value	Test Conditions
Manufacturer	WURTH	
Part Number	750810014	
Primary D.C. resistance	4.420 Ω	2-4, T_A = 20 °C
Secondary D.C. resistance	0.026 Ω	Tie (5+6, 7+8), T_A = 20 °C
Primary inductance (pins 3 - 4)	2.0 mH ±10%	10 kHz, T_A = 20 °C
Leakage inductance	26 µH typ, 34 µH max	Tie (5+6, 7+8), T_A = 20 °C
Turns ratio	12.36:1	(2 - 4)/(5 - 8), tie (5+6,7+8)
Saturation current	0.53 A max	20% rolloff from initial
Dielectric	1875 V_{AC}, 1s	4-5, tie (5+6), T_A = 20 °C

Figure 4. Transformer electrical diagram

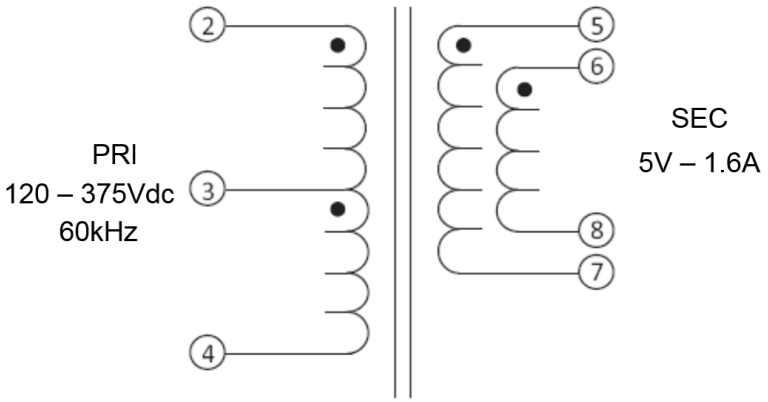


Figure 5. Transformer side view

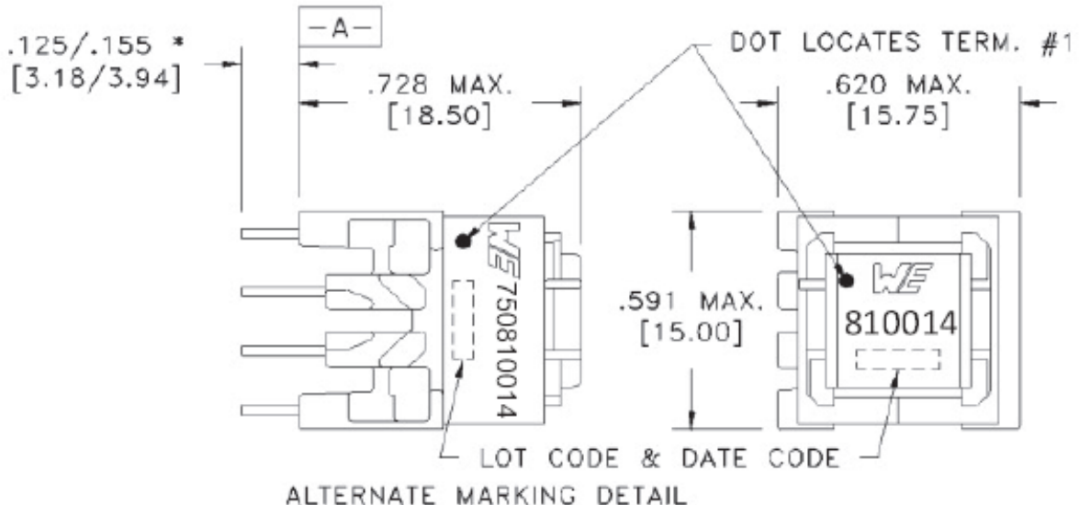


Figure 6. transformer pin distances (bottom view)

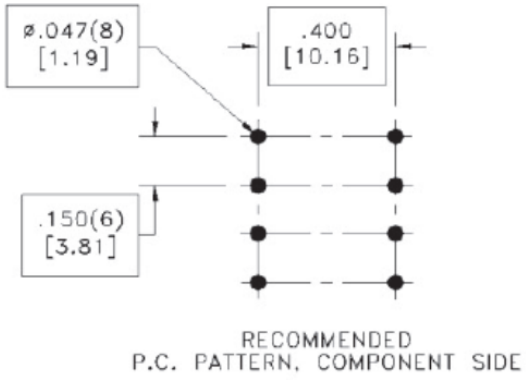
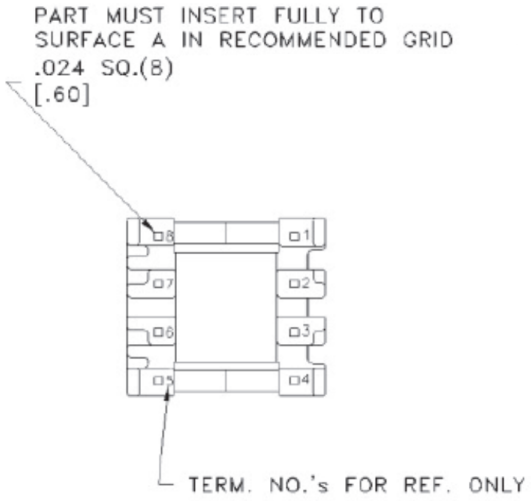


Figure 7. transformer bottom view



3.1 Drain voltage and current waveforms

Figure 8. Waveforms at 115 V_{AC}, full load

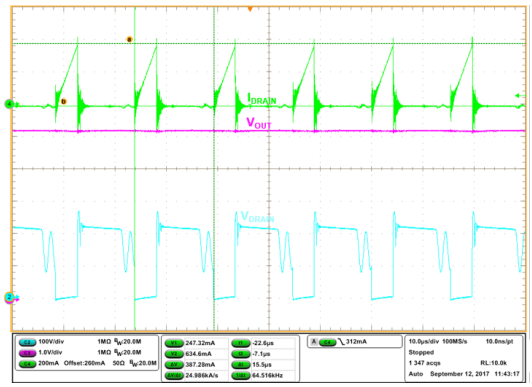


Figure 9. Waveforms at 230 V_{AC}, full load

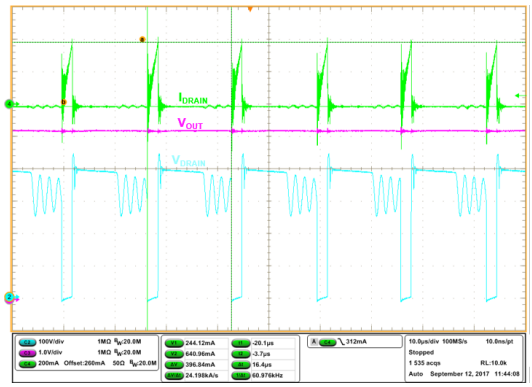


Figure 10. Waveforms at 90 V_{AC}, full load

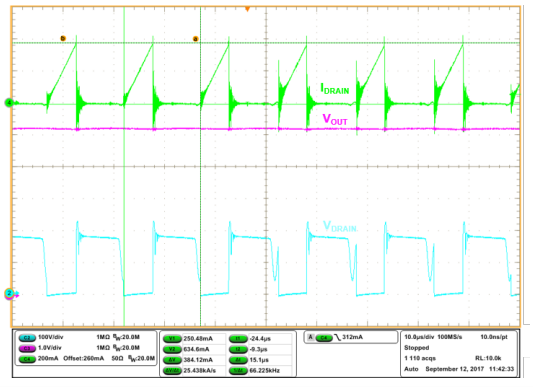
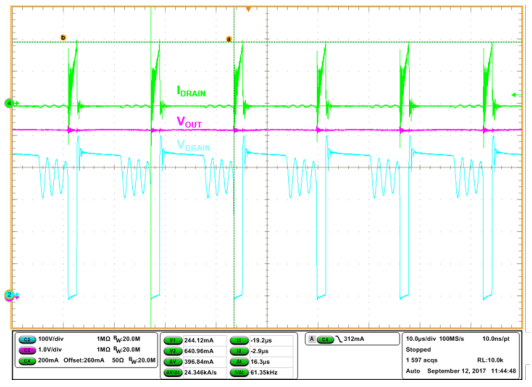


Figure 11. Waveforms at 265 V_{AC}, full load



4 Testing the board

4.1 Efficiency

All the measurements listed in this section were taken without the DIS network, with R1, R2, R3, C6 not mounted and R4 = 0 Ω (default setting of the BOM).

Active mode efficiency is defined as the average of the efficiencies measured at 25%, 50%, 75% and 100% of maximum load, at nominal input voltages (V_{IN} = 115 V_{AC} and V_{IN} = 230 V_{AC}).

External power supplies (the power supplies which are contained in a separate housing from the end-use devices they are powering) need to comply with the Code of Conduct, version 5 "Active mode efficiency" criterion.

The STEVAL-ISA196V1 is classified under the “Low-voltage external power supply” subclass, for:

- a nameplate output voltage of less than 6 Volts; and
- a nameplate output current greater than or equal to 550 milliAmperes.

For this subclass, the Code of Conduct, version 5 states that an SMPS with power throughput of 6 W should have an active mode efficiency higher than 75.2%.

Another applicable standard is the DOE (Department of Energy) recommendation of 75.0% active mode efficiency for the same power throughput.

Table 4. Active mode efficiency demonstrates the compliance of the STEVAL-ISA196V1 evaluation board with both of the above standards.

Table 4. Active mode efficiency

CoC5 req. (P_{OUT} = 6W)	DOE req. (P_{OUT} = 6W)	STEVAL-ISA196V1 performance
75.2%	75.0%	79.4% (@ V_{IN} =115V_{AC})
		79.0% (@V_{IN} = 230V_{AC})

4.2 Light load performance

In version 5 of the Code of Conduct, there are also efficiency requirements when the output load is 10% of the nominal output power. The following table demonstrates compliance of the STEVAL-ISA196V1 device with this requirement.

Table 5. CoC5 requirement and STEVAL-ISA196V1 performance at 10% output load

CoC5 requirement	STEVAL-ISA196V1 performance
66.0	77.3(@115V_{AC})
	71.7(@230V_{AC})

Power consumption when the power supply is not loaded is also addressed in CoC5. The table below demonstrates the conformance of the STEVAL-ISA196V1 with the criteria for EPS converters with nominal output power below 49 W at nominal input voltages.

Table 6. CoC5 Energy consumption criteria for no-load & STEVAL-ISA196V1 performance

Max no load consumption (0.3W<Pno<49W)	STEVAL-ISA196V1 no load consumption
75mW	3.9 mW (@V_{IN} = 115V_{AC})
	7.9 mW (@V_{IN} = 230 V_{AC})

Depending on the equipment supplied, there are several criteria to measure the performance of a converter. In particular, one requirement for light-load performance (EuP lot 6) is that the input power should be less than 500 mW when the converter is loaded with 250 mW. The following table shows how the STEVAL-ISA196V1 board satisfies this requirement, along with efficiency figures for P_{OUT} = 25 mW and P_{OUT} = 50 mW light-load conditions.

Table 7. Light load performance

V_{IN} [V_{AC}]	eff [%]		
	@ P_{OUT} = 25mW	@ P_{OUT} = 50mW	@ P_{OUT} = 250mW
115	58	62	71.9
230	49	55	65.3

Another criterion is output power (or efficiency) when the input power is equal to one watt.

Table 8. Efficiency @ P_{IN} = 1W

V_{IN} [V_{AC}]	eff @ P_{IN} = 1W [%]
115	76.7
230	70.6

5 IC features

5.1 Soft-start

The device features an internal soft-start function, which progressively increases the cycle-by-cycle current limitation set point from zero up to I_{DLIM} in eight 50 mA steps. This limits the drain current during the output voltage increase and therefore reduces the stress on the secondary diode. The soft-start time t_{SS} (the time needed for the current limitation set-point to reach its final value) is internally fixed at 8 ms. This function is activated on converter startup and on restart after a fault event.

Figure 12. Soft-start at full load

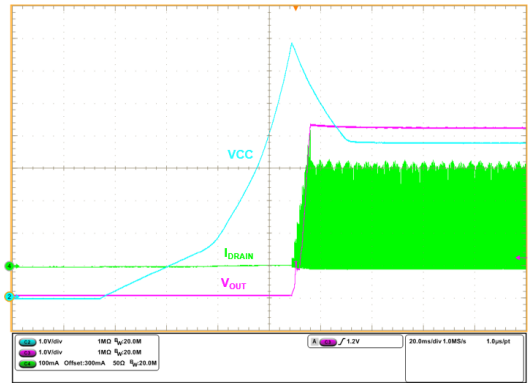
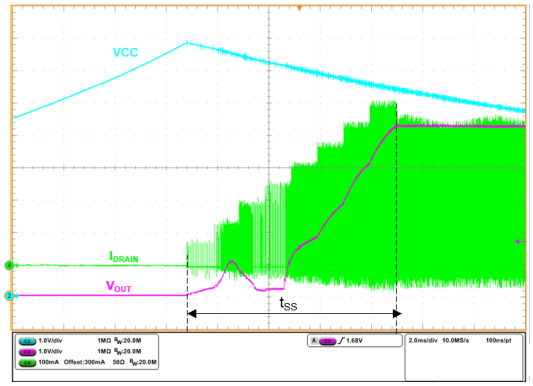


Figure 13. Soft-start at full load, zoom



5.2 Overload protection

During an overload or short-circuit, the drain current reaches I_{DLIM}. For every cycle that this condition is met, an internal OCP counter is incremented and the protection is tripped if the fault is maintained for the duration t_{OVL} (50 ms typ., internally fixed), see Figure 14. OLP (fault applied during steady state operation; t_{OVL}). On protection tripping, the power section is turned off and the converter is disabled for $t_{RESTART}$ (1 s typ.), after which the IC resumes switching and, if the fault persists, continues triggering the protection in the same way (see Figure 15. OLP (fault applied during steady state operation; $t_{RESTART}$)). This lowers the restart attempt rate to ensure safe operation with extremely low power throughput and avoids IC overheating.

Figure 14. OLP (fault applied during steady state operation; t_{OVL})

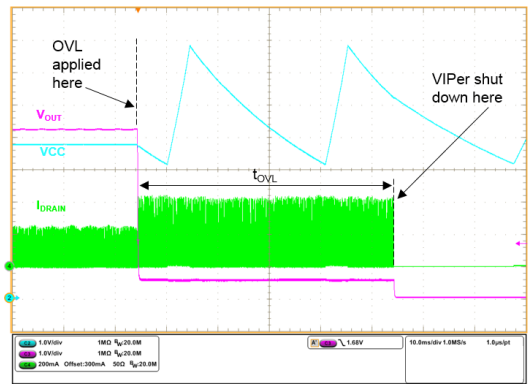
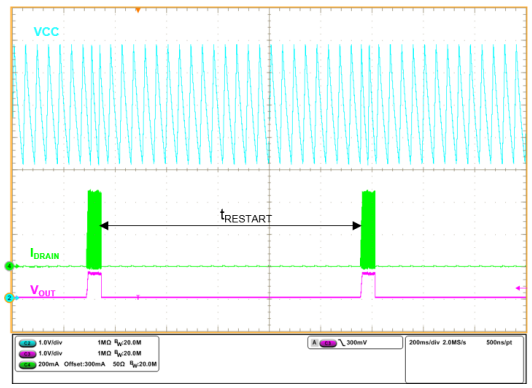


Figure 15. OLP (fault applied during steady state operation; $t_{RESTART}$)



Furthermore, every time the protection is tripped, the internal soft-start function is invoked (see Figure 16. OLP (fault maintained; t_{SS} and t_{OVL})) at restart to reduce the stress on the secondary diode.

Following fault removal, the IC resumes normal operation working normally. If the fault is removed during t_{SS} or t_{OVL} (before protection tripping), the counter counts down each cycle to zero and the protection is not tripped. If the short circuit is removed during $t_{RESTART}$, the IC waits for the $t_{RESTART}$ period to elapse before resuming switching (Figure 17. OLP (fault removed and autorestart)).

Figure 16. OLP (fault maintained; t_{SS} and t_{OVL})

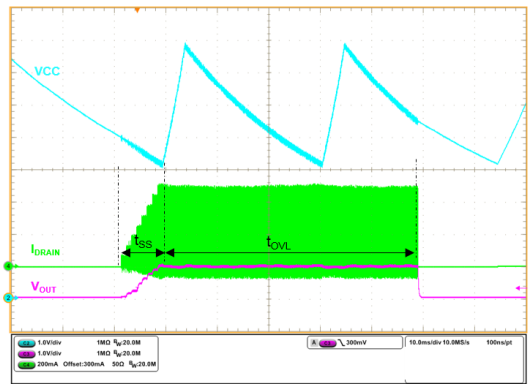
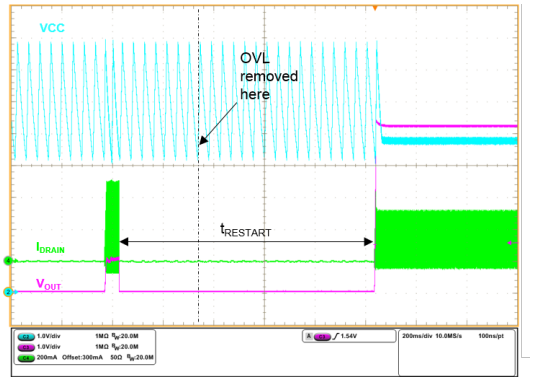


Figure 17. OLP (fault removed and autorestart)



5.3 Pulse-skip mode

Any time the drain peak current, I_{DRAIN}, exceeds I_{DLIM} within the minimum on-time t_{ON_MIN}, one switching cycle is skipped. The check is performed on a cycle-by-cycle basis, and the cycles can be skipped until the minimum switching frequency F_{OSC_MIN} (15 kHz, typ) is reached.

If the above condition persists, when the internal OCP counter reaches its end-of-count, the IC is stopped for $t_{RESTART}$ (1 s, typ.) and subsequently reactivated via the soft-start phase.

Whenever I_{DRAIN} does not exceed I_{DLIM} within t_{ON_MIN}, one switching cycle is restored. The check is made on a cycle-by-cycle basis, and the cycles can be restored until the nominal switching frequency F_{OSC} is reached.

The protection helps limit the "flux runaway" effect with an inductor discharge time longer than what would be allowed at nominal switching frequency when required. The "flux runaway" effect is often present at converter startup when the primary MOSFET that is charged during the minimum on-time through the input voltage cannot discharge the same amount during off-time because the output voltage is very low. The result is a net increase in average inductor current, which can reach dangerously high values while the output capacitor is not yet sufficiently charged to ensure the inductor discharge rate needed to maintain the volt-second balance.

To check the protection, the secondary diode D3 is shorted while the converter is operating at 265 V_{AC}. In the following two figures, the first part of the protection sequence is captured. From Figure 19. V_{IN} = 230 V_{AC}, D3 shorted, steady-state, image 2:

1. I_{DLIM} is exceeded at the first cycle, so the next one is skipped, resulting in a 30 kHz switching frequency
2. I_{DLIM} is exceeded again, so the switching frequency is further halved to 15 kHz
3. I_{DLIM} is exceeded again and the switching frequency is kept at 15 kHz indefinitely

Figure 18. V_{IN} = 230 V_{AC}, D3 shorted, steady-state, image 1

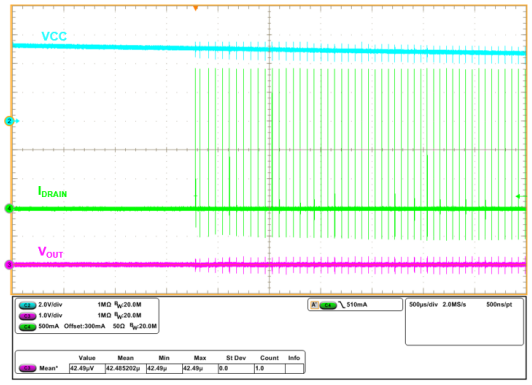


Figure 19. V_{IN} = 230 V_{AC}, D3 shorted, steady-state, image 2

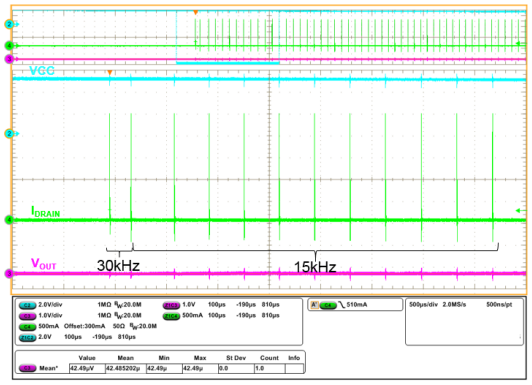


Figure 20. V_{IN} = 230 V_{AC}, D3 shorted, zoom shows the magnification of one of the switching cycles, where the DRAIN current exceeds I_{DLIM} within t_{ON_MIN}. The converter is operated indefinitely at 15 kHz and the OCP internal counter is incremented at every switching cycle. As it is designed to reach its end-of-count (defined by t_{OVL}) after 50 ms at 60 kHz operation, the overload time is incremented to 200 ms, as shown in Figure 21. VIN = 230 V_{AC}, D3 shorted, steady-state, image 3.

Figure 20. V_{IN} = 230 V_{AC}, D3 shorted, zoom

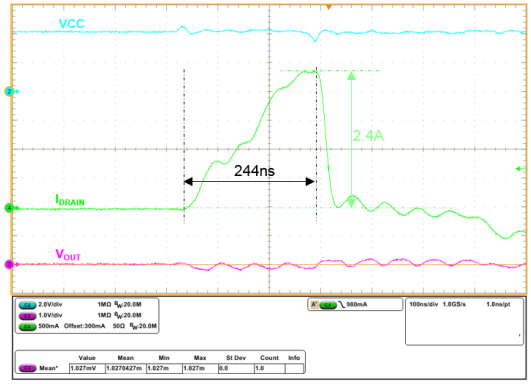
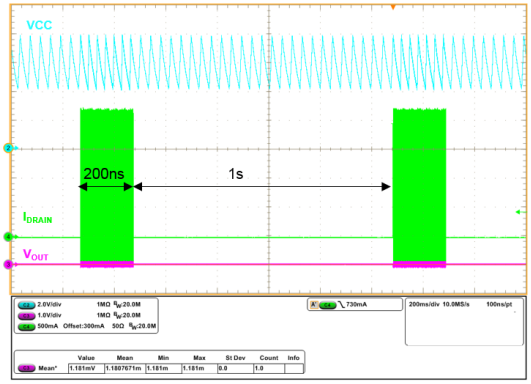


Figure 21. VIN = 230 V_{AC}, D3 shorted, steady-state, image 3



5.4 Max duty-cycle counter protection

The IC embeds a maximum duty-cycle counter which disables the PWM if the MOSFET is turned off by max. duty cycle (70% min., 80% max.) for ten consecutive switching cycles. After protection tripping, the PWM is disabled for $t_{RESTART}$ and subsequently reactivated via the soft-start phase until the fault condition is removed.

In some cases (i.e., breaking of the loop at low input voltage) even if V_{COMP} is saturated high, the OLP cannot be triggered because the PWM is turned off at every switching cycle by maximum duty cycle before the DRAIN peak current can reach I_{DLIM}. This can cause the output voltage V_{OUT} to rise uncontrollably and be maintained well above nominal values indefinitely, placing the output capacitor, the output diode and the IC itself at risk due to the potential breach of the 800 V breakdown threshold.

The max duty-cycle counter protection prevents the above failure, and we shall test this protection using heavy load and low input voltage settings. The IC is protected in autorestart mode for $t_{RESTART}$ (1 s typ.), then continues attempting soft-starts until the fault condition is removed, as shown below.

Figure 22. Shut down due to max duty cycle counter (initial tripping and restart)

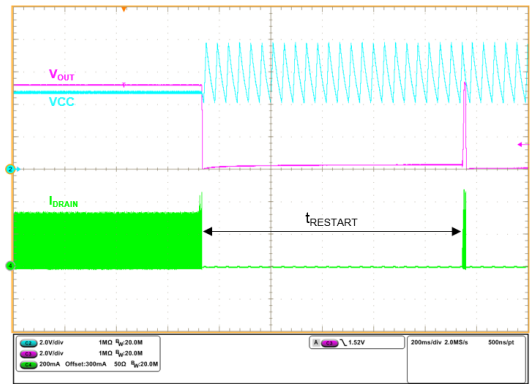


Figure 23. Shut down due to max duty cycle counter (steady state)

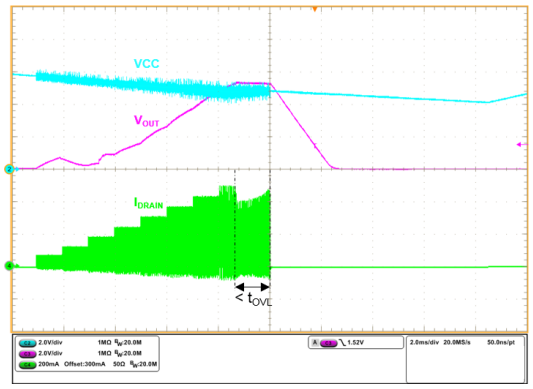


Figure 24. Shut down due to max duty cycle counter (steady state) - zoom shows the ten cycles causing the protection intervention. Figure 25. First of ten consecutive switching cycles at max duty cycle magnifies the first cycle and shows the duty-cycle measurement: 12/(12 + 4) = 75%.

Figure 24. Shut down due to max duty cycle counter (steady state) - zoom

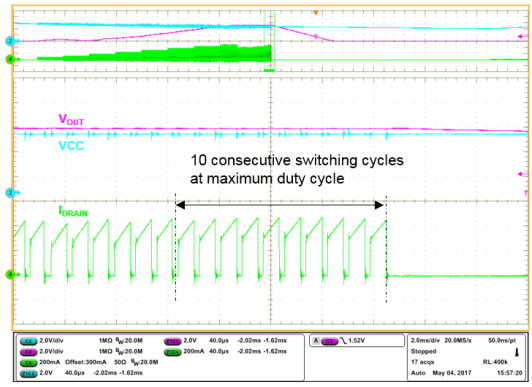
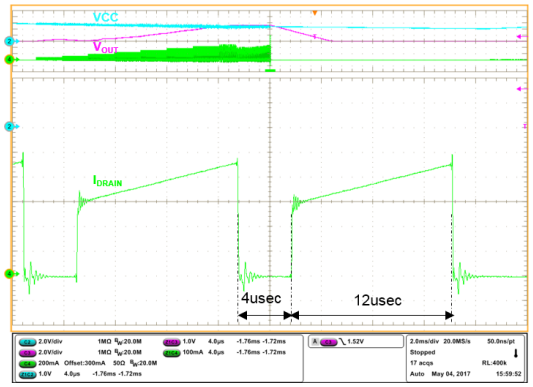


Figure 25. First of ten consecutive switching cycles at max duty cycle



5.5 Overtemperature protection

If the IC junction temperature rises higher than the internal threshold T_{SD} (160 °C, typ.), the PWM is disabled for $t_{RESTART}$. A single switching cycle is then performed, in which the temperature sensor embedded in the Power MOSFET section is checked. If a junction temperature above T_{SD} persists, the PWM remains disabled for time $t_{RESTART}$ (see Figure 26. OTP tripping and steady-state).

The overtemperature protection was tripped by subjecting the STEVAL-ISA196V1 to overheating by airflow from a thermal gun and the IC shut down when the case temperature measured approximately 152 °C (with a thermal camera). The load was then decreased and the converter resumed with a soft-start phase when the case temperature dropped to about 120 °C.

Figure 26. **OTP tripping and steady-state**

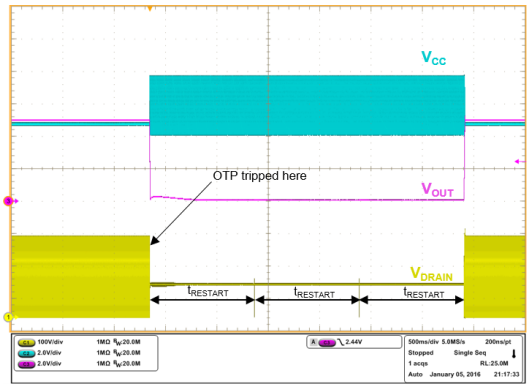
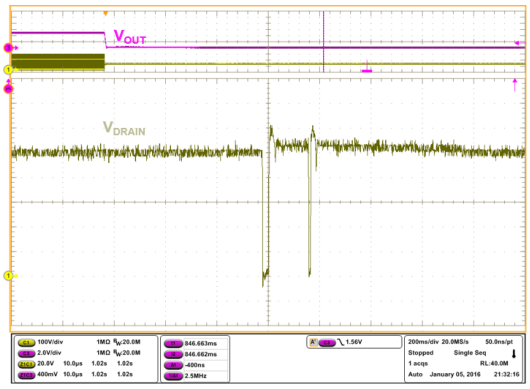


Figure 27. **Thermal check activation during OTP**



5.6 Input overvoltage protection

When the voltage across the DIS pin is externally pulled above the internal threshold V_{DIS_th} (1.2 V typ) for more than t_{DEB} (for instance, by means of a voltage divider connected to a higher voltage), the PWM is disabled in autorestart mode for $t_{DIS\_RESTART}$ (500 ms, typ.). This simplifies the implementation of the input overvoltage protection to merely connecting a voltage divider from the rectified input mains to the DIS pin. Resistors R1, R2, R3 and R4 in Section 2.2 Schematic diagram can be used for this purpose, with values selected according to the following formula:

$$R1 + R2 + R3 = \left(\frac{V_{IN\_OVP}}{V_{DIS\_th}} - 1\right) \cdot R4 \quad (1)$$

where V_{IN_OVP} is the desired input overvoltage threshold.

The additional steady-state power consumption of this network is:

$$P_{DIS}\left(V_{IN\_DC}\right) = \frac{\left(V_{IN\_DC} - V_{DIS}\right)^2}{R1 + R2 + R3} + \frac{V_{DIS}^2}{R4} \quad (2)$$

For example, if R4 = 9.1 kΩ, R1 = R2 = R3 = 1 MΩ, the protection is triggered at V_{IN} = 400 V_{DC}, with additional steady-state power consumption at 230 V_{AC} of about 35 mW.

For filtering purposes, 1 nF/50 V can be selected for C6.

As the STEVAL-ISA196V1 is in non-isolated topology, an output overvoltage protection can be obtained by connecting the voltage divider to the output terminal, with the additional network power consumption being:

$$P_{DIS}\left(V_{OUT}\right) = \frac{\left(V_{OUT} - V_{DIS}\right)^2}{R1 + R2 + R3} + \frac{V_{DIS}^2}{R4} \quad (3)$$

If the Disable function is not required, the DIS pin must be soldered to GND (STEVAL-ISA196V1 default setting) to exclude the function.

The following figures show some relevant waveforms for input overvoltage protection implemented through the DIS pin.

Figure 28. Input OVP triggering

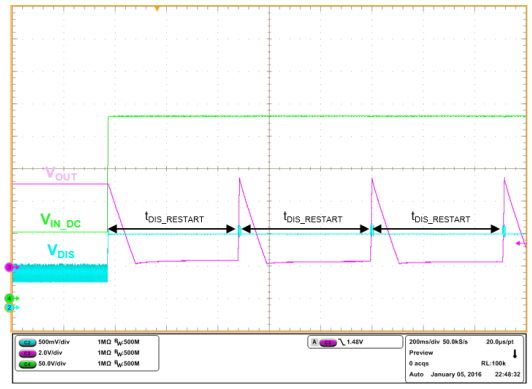


Figure 29. Input OVP triggering (steady state)

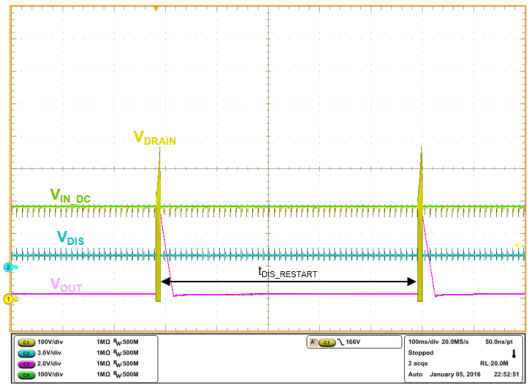


Figure 30. Input OVP triggering (steady state, zoom)

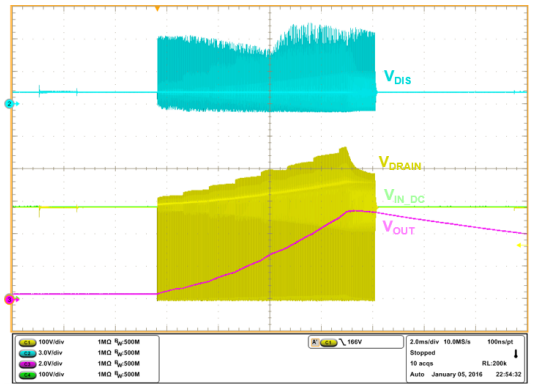
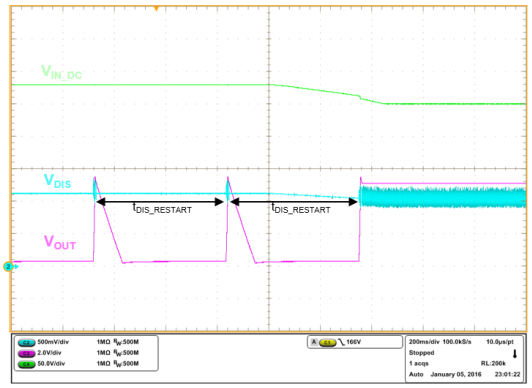


Figure 31. Input OVP removed and IC restart

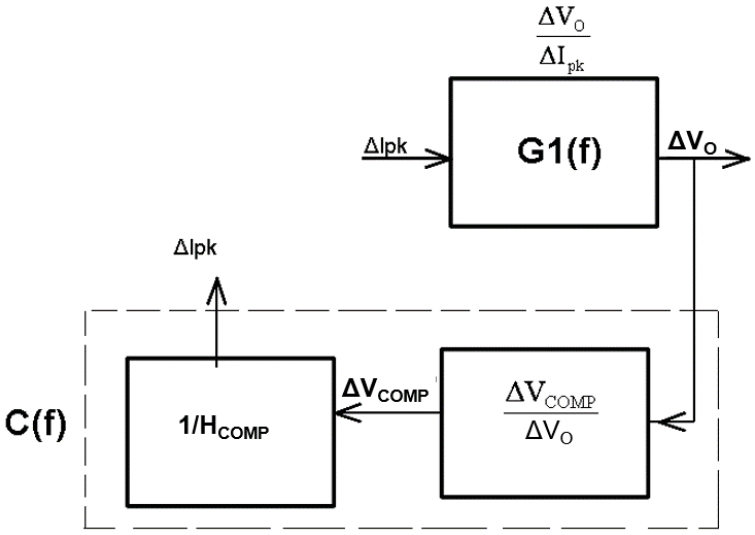


6 Feedback loop calculation guidelines

6.1 Transfer function

The set PWM modulator + power stage is indicated by G1(f), while C(f) is the "controller" that ensures the stability of the system.

Figure 32. Control loop block diagram



The mathematical expression for the power block G1(f) is the following:

$$G1(f) = \frac{\Delta V_O}{\Delta I_{pk}} = \frac{|V_{OUT}| \cdot \left(1 + \frac{j \cdot 2 \cdot \pi \cdot f}{z}\right)}{Ipkp\left(fsw, Vdc\right)\left(1 + \frac{j \cdot 2 \cdot \pi \cdot f}{p}\right)} = \frac{|V_{OUT}| \cdot \left(1 + \frac{j \cdot f}{fz}\right)}{Ipkp\left(fsw, Vdc\right)\left(1 + \frac{j \cdot f}{fp}\right)} \quad (1)$$

fp is the pole due to the output load and fz the zero due to the ESR of the output capacitor:

$$fp = \frac{1}{\pi \cdot C_{OUT}(R_{OUT} + 2 \cdot ESR)} \quad (2)$$

$$fz = \frac{1}{2 \cdot \pi \cdot C_{OUT} \cdot ESR} \quad (3)$$

The mathematical expression of the compensator C(f) is:

$$C1(f) = \frac{\Delta I_{pk}}{\Delta V_O} = \frac{C_0}{H_{COMP}} \cdot \frac{1 + \frac{f \cdot j}{fZc}}{\left(2 \cdot \pi \cdot f \cdot j\right) \cdot \left(1 + \frac{f \cdot j}{fPc}\right)} \quad (4)$$

where:

$$C_0 = \frac{-Gm}{C7 + C8} \cdot \frac{R7}{R6 + R7} \quad (5)$$

$$fZc = \frac{1}{2 \cdot \pi \cdot R8 \cdot C7} \quad (6)$$

$$fPc = \frac{1}{2 \cdot \pi \cdot R8} \cdot \frac{C7 + C8}{C7 \cdot C8} \quad (7)$$

are chosen to censure the stability of the system. Gm = 0.55m A/V (typ.) is the VIPer11 transconductance, H_{COMP} = (V_{COMPH} - V_{COMPL})/(I_{DLIM} - I_{DLIM_PFM}).

6.2 Compensation procedure

The first step is to choose the pole and zero of the compensator and the crossing frequency:

$$fZc = x \cdot fp \quad (1)$$

$$fPc = y \cdot fp \quad (2)$$

$$fcross \leq \frac{fsw}{10} \quad (3)$$

…where x and y are given arbitrary values.

G1(fcross) can be calculated from Eq. (1) and, since by definition $\left| C(fcross)*G1(fcross) \right| = 1$, C_0 is obtained from Eq. (4) as follows:

$$C_0 = \frac{\left|2 \cdot \pi \cdot fcross \cdot j\right| \cdot \left|1 + \frac{fcross \cdot j}{fPc}\right|}{\left|1 + \frac{fcross \cdot j}{fZc}\right|} \cdot \frac{Hcomp}{G1(fcross)} \quad (4)$$

At this point, the Bode diagram for G1(f)*C(f) can be plotted to check the phase margin for stability.

If the margin is not high enough, choose new fZc, fPc and fcross values and repeat the procedure.

When stability is achieved, the next step is to find the values of the schematic components:

- R6 is set to a value in the order of several tens of kOhms
- R7 is calculated from Eq. (1):

$$R7 = \frac{R6}{\frac{V_{OUT}}{V_{REF\_FB}} - 1} \quad (5)$$

- C8 is calculated by combining Eq. (5), Eq. (6) and Eq. (7):

$$C8 = \frac{fZc}{fPc} \cdot \frac{Gm}{|C_0|} \cdot \frac{R6}{R6 + R7} \quad (6)$$

- C7 is calculated from Eq. (6) and Eq. (7):

$$C7 = C8 \cdot \left(\frac{fPc}{fZc} - 1\right) \quad (7)$$

- Finally, R8 is calculated from Eq. (7):

$$R8 = \frac{1}{2 \cdot \pi \cdot fPc} \cdot \frac{C7 + C8}{C7 \cdot C8} \quad (8)$$

After selecting commercial values for R6, R7, R8, C7 and C8, the actual values of C_0, fZc and fPc should be calculated from equations Eq. (5), Eq. (6) and Eq. (7) to obtain C_0_act, fZc_act and fPc_act, respectively. Substitute these values into Eq. (4) to obtain the actual compensator value, C_act(f).

The Bode diagram of G1(f)*C_act(f) can now be plotted to check whether the phase margin for stability is still guaranteed.

7 Thermal measurements

Thermal analysis of the board was performed using an IR camera at 90 V_{AC}, 115 V_{AC}, 230 V_{AC} and265 V_{AC} mains input, 25 °C ambient temperature and full load condition. The results are shown in the following figures.

Figure 33. Thermal measurement at 90 V_{AC}, full load (bottom view)

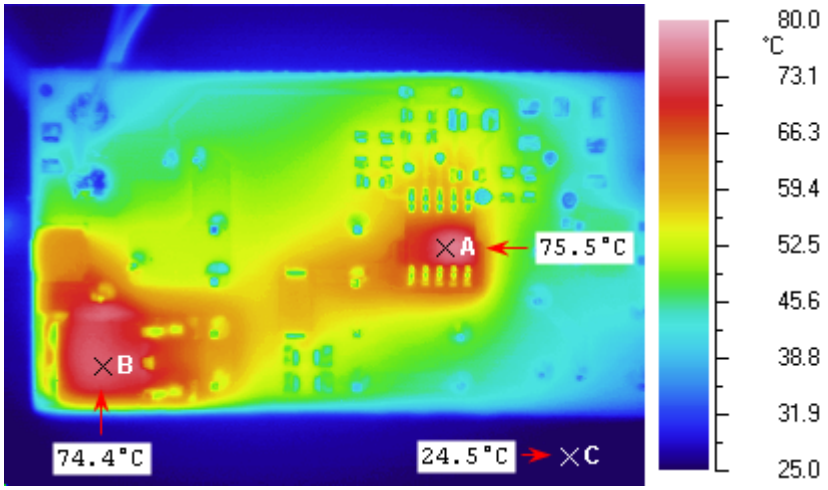


Figure 34. Thermal measurement at 115 V_{AC}, full load (bottom view)

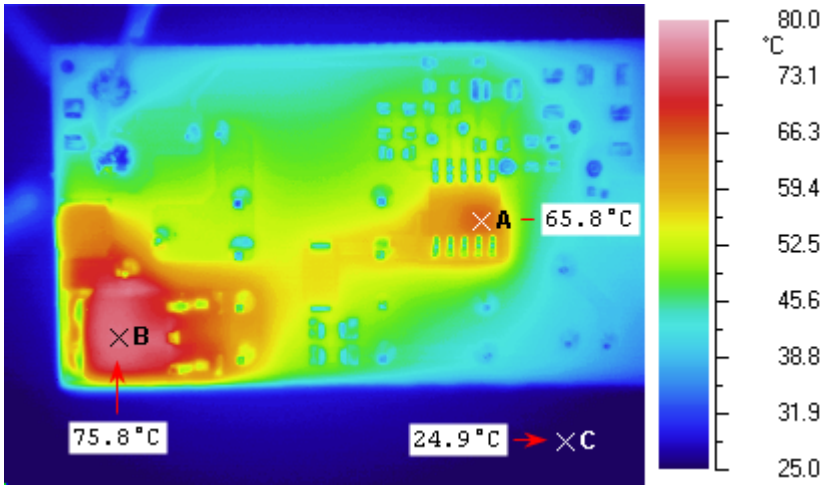


Figure 35. **Thermal measurement at 230 V_{AC}, full load (bottom view)**

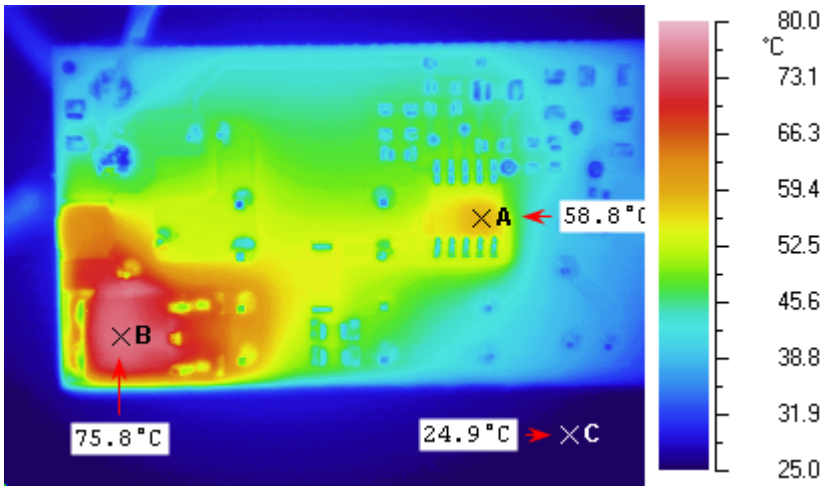
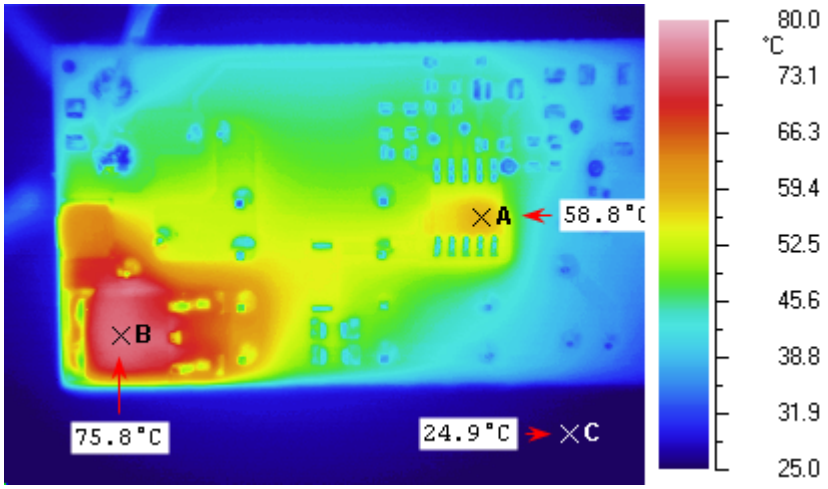


Figure 36. **Thermal measurement at 265 V_{AC}, full load (bottom view)**



8 EMI measurements

A pre-compliance test for European normative EN55022 (Class B) was performed using an EMC analyzer with average detector and a line impedance network stabilization (LISN).

Figure 37. EMI measurements with average detector at 115 V_{AC}, full load, T_{AMB} = 25 °C

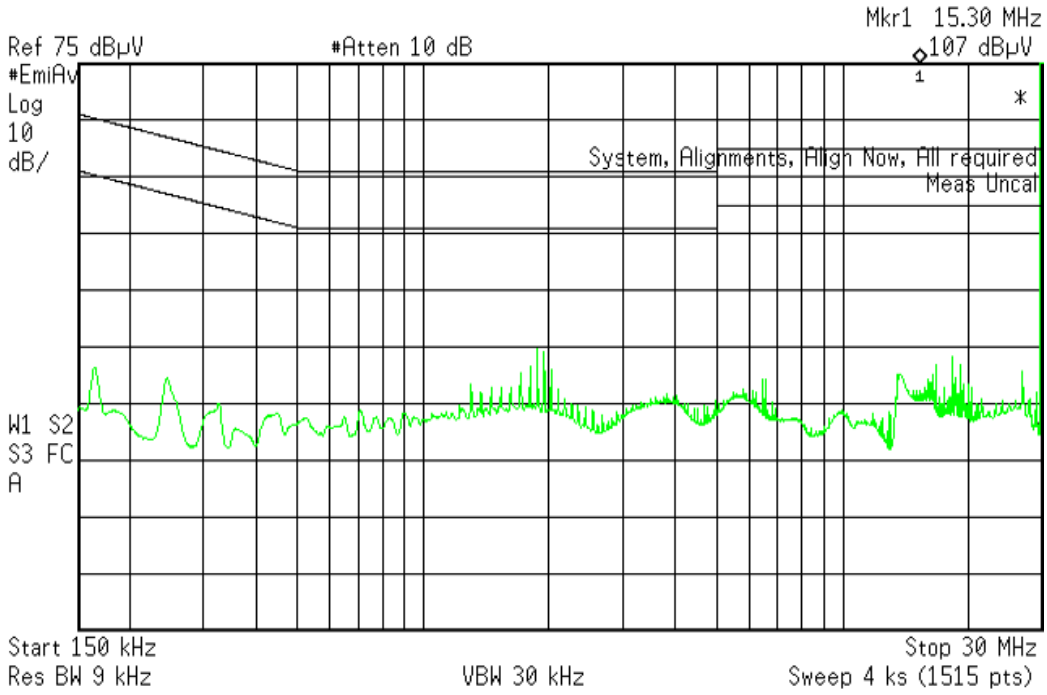
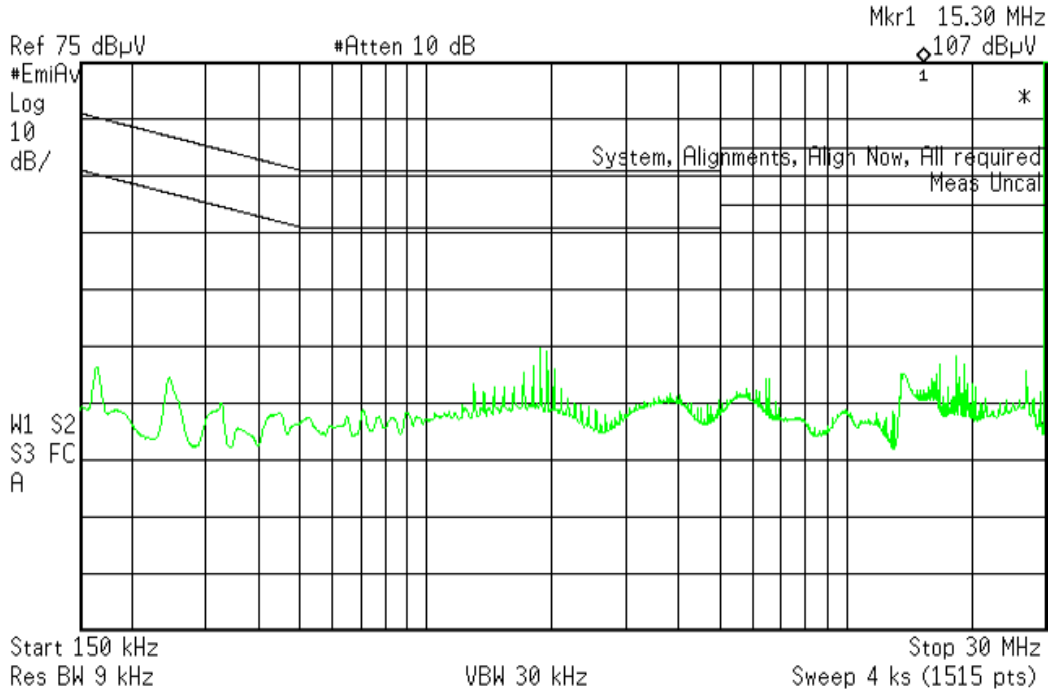


Figure 38. EMI measurements with average detector at 230 V_{AC}, full load, T_{AMB} = 25 °C



9 Board layout

Figure 39. Board layout (complete)

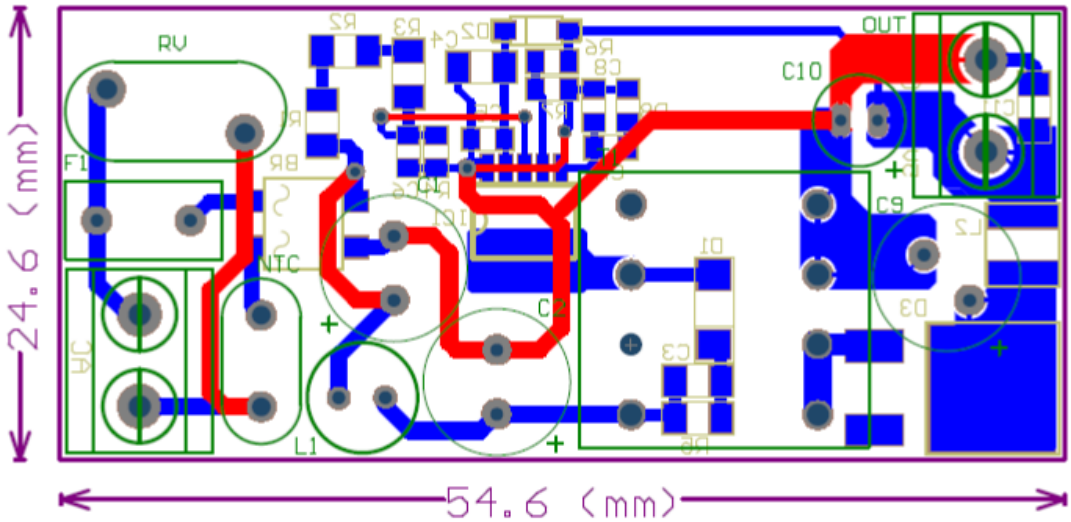


Figure 40. Board layout (top layer + top overlay)

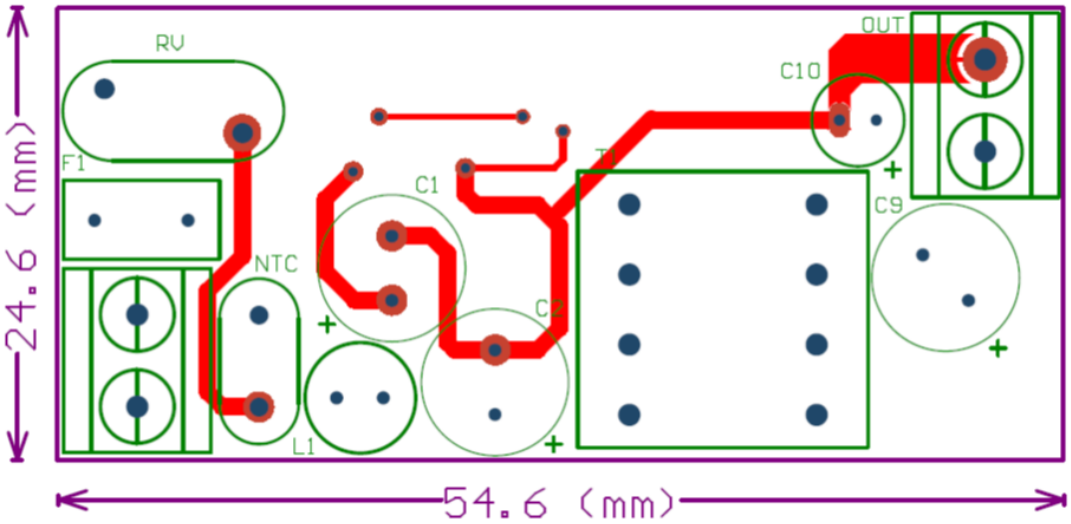
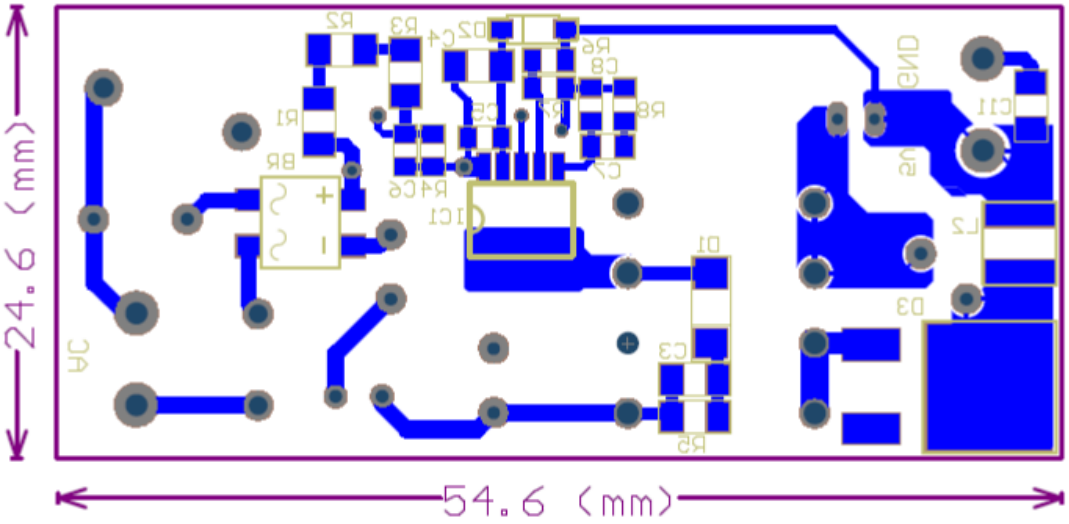


Figure 41. **Board layout (bottom layer + top overlay)**



10 Conclusions

The STEVAL-ISA196V1 demonstrates that the VIPer11 facilitates the design of a non-isolated converter that is compliant with the most stringent energy regulations, and which requires relatively few external components.

The STEVAL-ISA196V1 consumes less than 10 mW at 230 VAC mains under no-load condition and can satisfy both CoC 5 and DOE low-voltage external power supplies requirements for active mode and light-load efficiency.

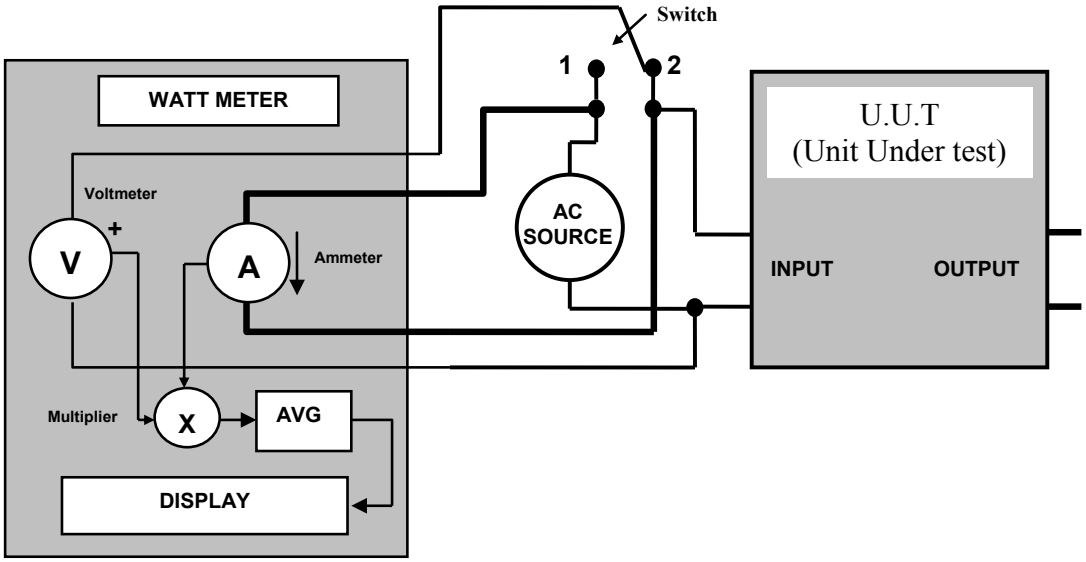
The 800 V avalanche rugged Power MOSFET and the embedded protections add reliability to the power converter, rendering the VIPer11 the ideal choice for applications requiring robustness and energy-efficient performance.

A APPENDIX A - Test equipment and measurement of efficiency and light load performance

The converter input power is measured with a wattmeter, taking simultaneous readings of the converter input current (using its internal ammeter) and voltage (using its internal voltmeter). The wattmeter is a digital instrument, so it samples the current and voltage and converts them into digital forms. The digital samples are then multiplied to give the instantaneous measured power. The sampling frequency is in the range of 20 kHz (or higher, depending on the instrument used). The reading gives the average measured power over a short time interval short period of time (1 s typ.).

The following figure shows the wattmeter connected to the UUT (unit under test) and the AC source, as well as the wattmeter internal block diagram.

Figure 42. Connections of the UUT to the wattmeter for power measurements



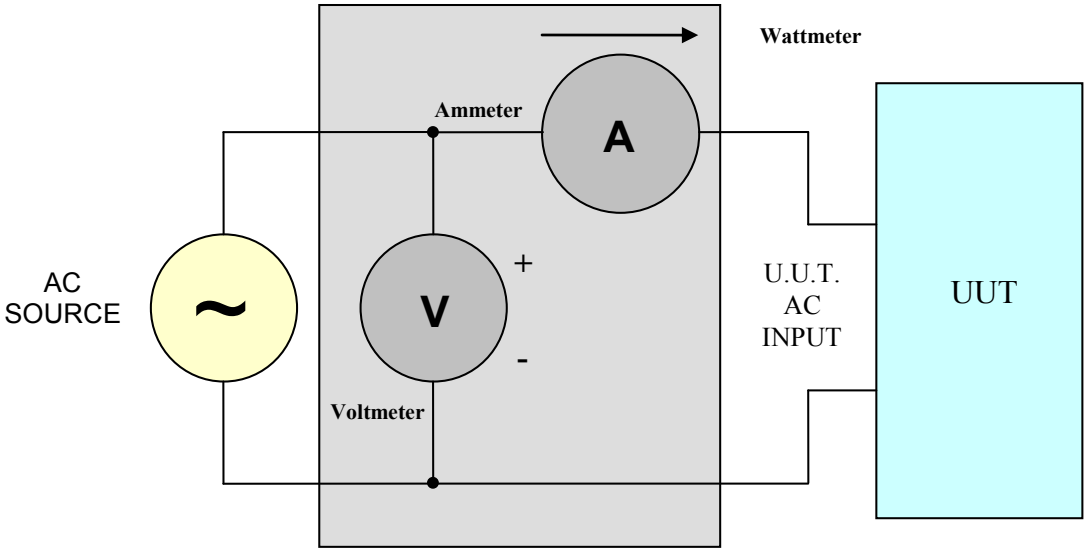
An electronic load is connected to the output of the power converter (UUT), allowing the setting and measurement of the load current of the converter, while the output voltage is measured by a voltmeter. The output power is the product of the load current and output voltage.

The ratio between the output power and the input power measured by the wattmeter is the efficiency of the converter. It is measured under different input and output conditions acting on the AC source and on the electronic load.

With reference to Figure 42. Connections of the UUT to the wattmeter for power measurements, the UUT input current causes a voltage drop across the ammeter internal shunt resistance (the ammeter is not ideal so it has an internal resistance higher than zero) and across the cables connecting the wattmeter to the UUT.

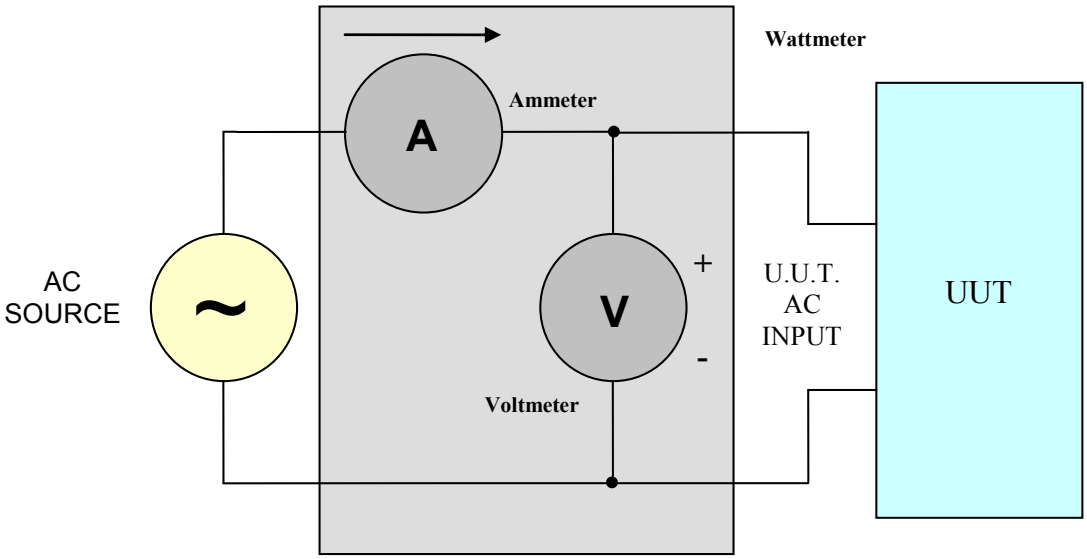
If the switch in Figure 42. Connections of the UUT to the wattmeter for power measurements is in position 1 (see the simplified scheme in Figure 43. Switch in position 1 - setting for standby measurements) this voltage drop causes a measured input voltage higher than the input voltage at the UUT input that obviously affects the measured power. The voltage drop is generally negligible if the UUT input current is low (for example, when we are measuring the input power of a UUT in the light-load condition).

Figure 43. **Switch in position 1 - setting for standby measurements**



For high UUT input currents, the voltage drop can be relevant (compared to the UUT real input voltage), so in this case the switch in Figure 42. Connections of the UUT to the wattmeter for power measurements can be set to position 2 (see simplified scheme in Figure 44. Switch in position 2 - setting for efficiency measurements) where the UUT input voltage is measured directly at the UUT input terminal and the input current does not affect the measured input voltage.

Figure 44. **Switch in position 2 - setting for efficiency measurements**



The voltage across the voltmeter causes a leakage current inside the voltmeter itself (that is not ideal). If the switch in Figure 42. Connections of the UUT to the wattmeter for power measurements is in position 2 (see simplified scheme in Figure 44. Switch in position 2 - setting for efficiency measurements), the voltmeter leakage current is measured by the ammeter together with the UUT input current, causing a measurement error. The error is negligible if the UUT input current is much higher than the voltmeter leakage. If the UUT input current is not much higher than the voltmeter leakage current, it is probably better to set the switch in Figure 42. Connections of the UUT to the wattmeter for power measurements to position 1.

If you are not sure which measurement scheme is more suitable, you can try both and record the lower input power value.

As noted in IEC 62301, instantaneous measurements are appropriate when power readings are stable. The UUT shall be operated at 100% of nameplate output current output for at least 30 minutes (warm-up period) immediately prior to conducting efficiency measurements.

After this warm-up period, the ac input power shall be monitored for a period of 5 minutes to assess the stability of the UUT. If the power level does not drift by more than 5% from the maximum value observed, the UUT can be considered stable and the measurements can be recorded at the end of the 5-minute period.

If ac input power is not stable over a 5-minute period, the average power or accumulated energy shall be measured over time for both ac input and dc output.

Some wattmeter models allow integrating the measured input power over a time interval and then measuring the energy absorbed by the UUT during that time, from which the average input power is calculated.

Revision history

Table 9. **Document revision history**

Date	Version	Changes
17-Jan-2018	1	Initial release.

Contents

List of figures

List of tables