STEVAL-ISA195V1: 5 V/1.8 W 30 kHz buck demo with the VIPer11

The STEVAL-ISA195V1 is a 5 V - 0.36 A power supply set in buck topology using the new VIPER11 off-line high voltage converter by STMicroelectronics, specifically developed for non-isolated SMPS. The device features:

- An 800 V avalanche rugged power section
- Integrated HV-start-up current generator
- Onboard soft-start
- PWM operation at 30 kHz with frequency jittering for lower EMI
- Transconductance error amplifier with 1.2 V ±2% reference voltage
- Self-supply option to avoid auxiliary winding and bias components

Thanks to the advanced light load management and ultra-low consumption of the VIPER11 internal blocks, the demo board input power consumption in no-load conditions can be reduced to less than 20 mW @230 V_{AC}, and the most stringent energy saving regulations in terms of active mode and light load efficiency can be fulfilled. IC protection includes:

- Pulse skip mode to avoid flux-runaway during start-up
- Delayed overload shutdown for safe fault condition management
- Max. duty cycle counter
- Thermal shutdown
- Input overvoltage

All protections (except pulse skip mode) involve auto-restart mode.

Figure 1. STEVAL-ISA195V1 top and bottom view

1 Board electrical specifications and design

The electrical specifications of the demo board are listed in the table below.

Table 1. STEVAL-ISA195V1 electrical specifications

Parameter	Value	Symbol
Input voltage range	[85 V_{AC}; 265 V_{AC}]	V_{IN}
Output voltage	5 V	V_{OUT}
Max. output current	0.36 A	I_{OUT}
Precision of output regulation	±5%	Δ_{VOUT_LF}
High frequency output ripple voltage	50 mV	Δ_{VOUT_HF}
Max. ambient operating temperature	60 °C	T_{AMB}
Switching frequency	30 kHz	F_{OSC}

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Max. ambient operating temperature	60 °C	T_{AMB}
Switching frequency	30 kHz	F_{OSC}

1.2 Circuit description

The FB pin is the inverting input of the VIPer11 internal error amplifier and is an accurate 1.2 V voltage reference with respect to the GND pin. This allows the voltage across the capacitor C8 to be set (which actually is a replica of the output voltage) through the R3 and R4 voltage divider shown in the circuit schematic, according to the following formula:

Equation 1:

$$V_{OUT} = V_{FB\_REF} \cdot \left(1 + \frac{R4}{R3}\right) \quad (1)$$

where resistor R4 is split into R4a and R4b to improve tuning of the output voltage value.

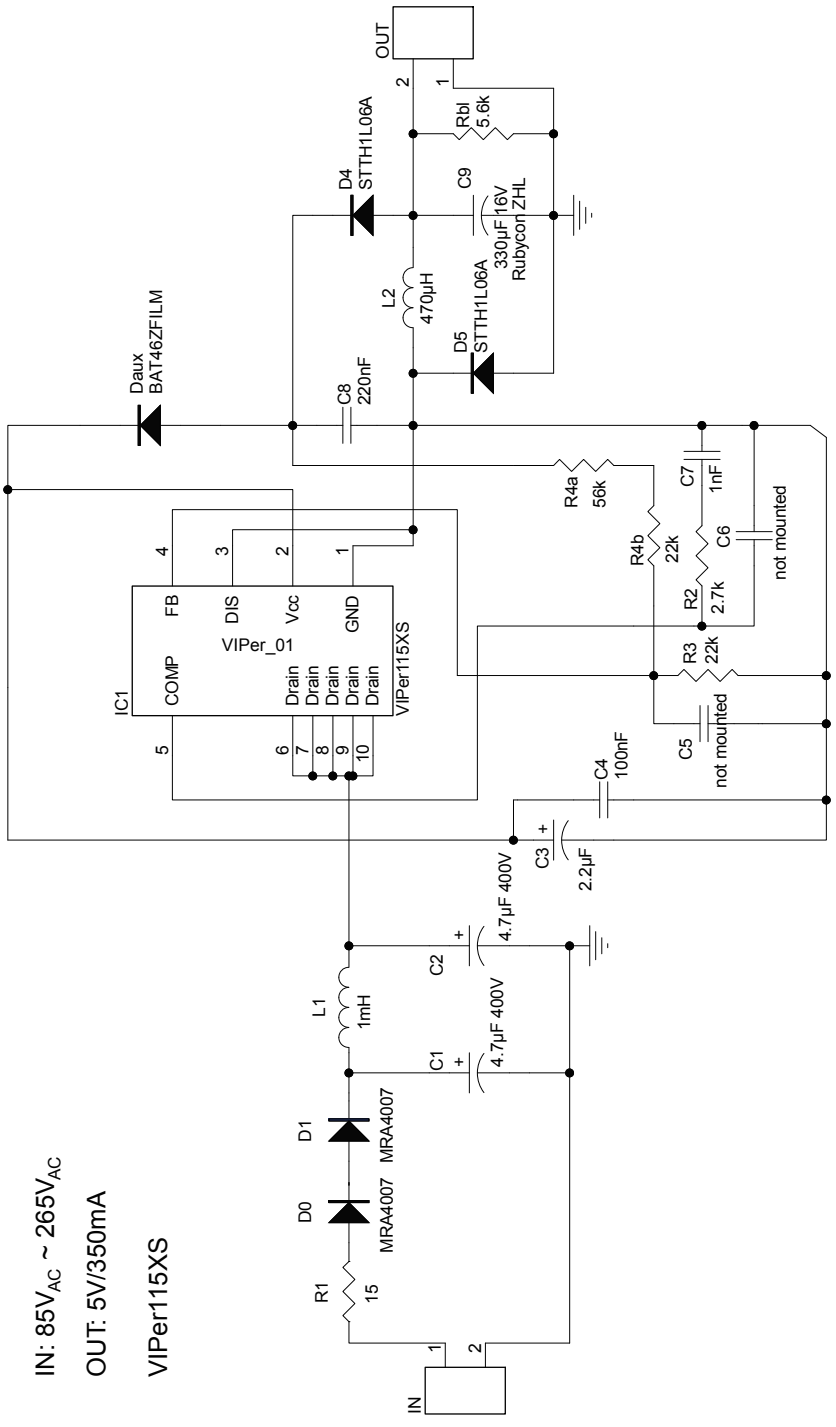
The compensation network is connected between the COMP pin (which is the output of the error amplifier) and the GND pin.

The bleeder resistor Rbl provides a 1 mA approximate minimum load to avoid overvoltage when the output load is disconnected. It is a trade-off between overvoltage containment and increase of power consumption under no-load. At power-up, as V_{DRAIN} exceeds $V_{HVSTART}$, the internal HV current generator charges the VCC capacitor, C3, to V_{CCon}, the power MOSFET starts switching, the current generator is turned off and the IC is powered by C3.

When V_{OUT} reaches its steady-state value, the IC is biased from the output through the diode D_{AUX}. This is referred to as "external biasing" and can be applied because the 5 V output voltage is high enough to keep the C3 voltage above the V_{CSon} threshold, whose maximum value $V_{CSon\_max.}$ is 4.5 V. With this setting, the VCC voltage shape during steady-state operation is constant, following the output voltage, the HV current generator is never activated and very low input power consumption under light or no-load conditions is possible (less than 20 mW at 230 V_{AC} under no-load with an appropriate design), thanks to the low consumption of the internal blocks of the IC.

1.3 Schematic diagram

Figure 2. STEVAL-ISA195V1 circuit schematic



1.3.1 Bill of materials

Table 2. **STEVAL-ISA195V1 bill of materials**

Item	Q.ty	Ref.	Part/value	Description	Manufacturer	Order code
1	2	D0, D1	1 A-1000 V	power rectifier diode	ON SEMICONDUCTOR	MRA4007T3G
2	1	Daux	0.15 A-100 V	signal Schottky diode	ST	BAT46ZFILM
3	2	D4, D5	600 V 1 A	Diode ultra fast	ST	STTH1L06A
4	1	L1	1 mH	axial inductor	Epcos	B82144A2105J
5	1	L2	0.47 mH ± 10%	radial inductor	COILCRAFT	DR0810-474L
6	2	C1, C2	4.7 µF, 400 V	electrical cap	Rubycon	400PX4R7MEFC8X115
7	1	C3	2.2 µF, 50 V	ceramic multilayer cap	Murata	GRM21BR61H225KA73L
8	1	C4	100 nF, 50 V	ceramic multilayer cap	Yageo	CC0603KRX7R9BB104
9	2	C5, C6	Not mounted	ceramic multilayer cap		
10	1	C7	1 nF, 50 V	ceramic multilayer cap	TDK	C1608C0G1H102J080AA
11	1	C8	220 nF, 50V	ceramic multilayer cap	Murata	GRM188F51H224ZA01D
12	1	C9	330 µF 16 V	Elcap ultra-low ESR	Rubycon, ZL series	16ZL330MEFC8X11.5
13	1	R1	15 Ω 1 W	flameproof	TE Connectivity	ROX1SJ15R
14	1	R2	2.7 kΩ±1% - 0.1 W		Vishay	CRCW06032K70FKEA
15	1	R3	22 kΩ±1% - 0.1 W		Vishay	CRCW060322K0FKEA
16	1	R4a	56 kΩ±1% - 0.1 W		Vishay	CRCW060356K0FKEA
17	1	R4b	22 kΩ±1% - 0.1 W		Vishay	CRCW060322K0FKEA
18	1	IC		Offline HV converter	ST	VIPer115XS

1.4 Board layout

Figure 3. Layout complete

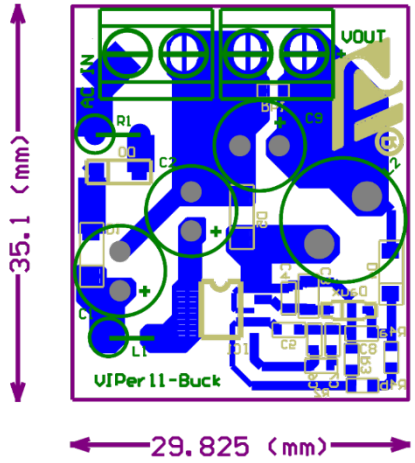


Figure 4. Layout top layer

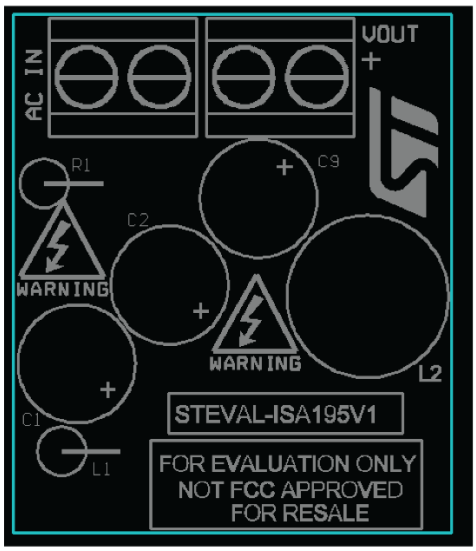
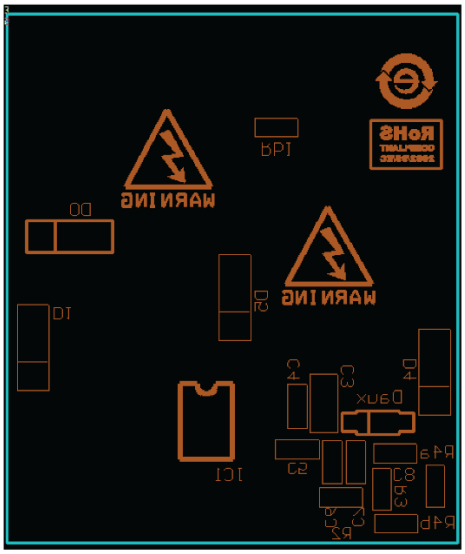


Figure 5. Layout bottom layer



1.5 Testing the boards

1.5.1 Typical waveforms

Voltage and current waveforms at nominal V_{IN} in full load conditions are reported in figures below.

Figure 6. Waveforms @ 115 V_{AC}, full load

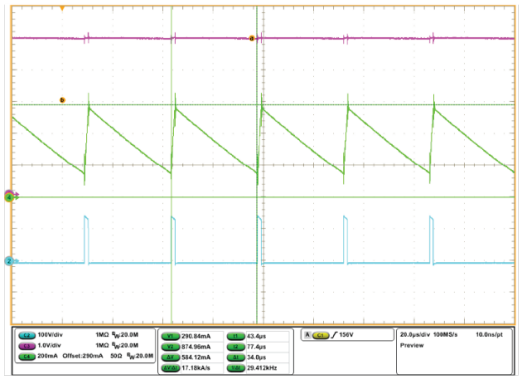


Figure 7. Waveforms @ 115 V_{AC}, full load, zoom

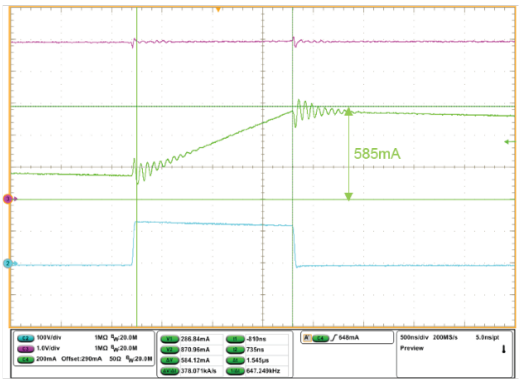


Figure 8. Waveforms @ 230 V_{AC}, full load

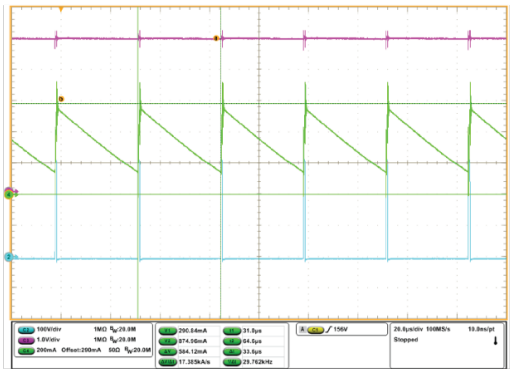
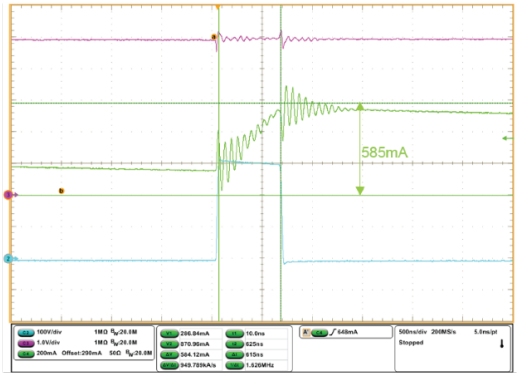


Figure 9. Waveforms @ 230 V_{AC}, full load, zoom



1.5.2 Line load regulation

The output voltage has been measured in different line and load conditions. The results are shown in the following figures.

Figure 10. Line regulation

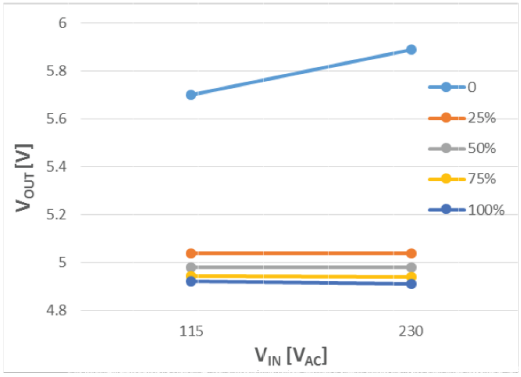
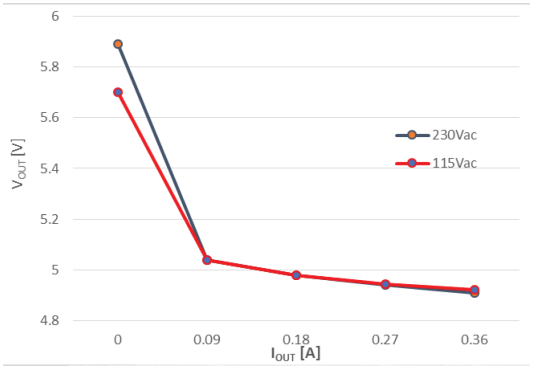


Figure 11. Load regulation



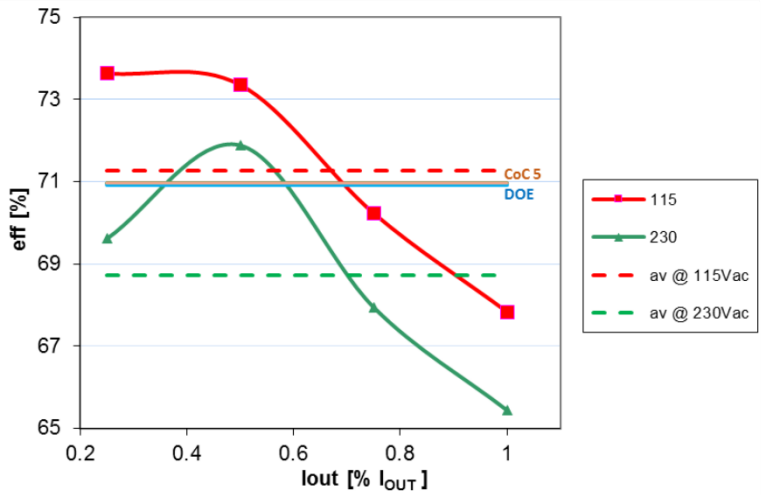
1.5.3 Efficiency measurements

The active mode efficiency is defined as the average of the efficiency measured at 25%, 50%, 75% and 100% of maximum load, at nominal input voltages (V_{IN} = 115 V_{AC} and V_{IN} = 230 V_{AC}). External power supplies (the power supplies contained in a separate housing from the end-use devices they are powering) need to comply with the

Code of Conduct, version 5 "Active mode efficiency" criterion, which, for a power throughput of 1.8 W, states the active mode efficiency must be above 70.96%.

DOE (department of energy) recommendation is another standard, whose active mode efficiency requirement for the same power throughput is 70.92%. In figure below, the DOE and CoC5 limits are indicated in solid lines; average efficiency at 115 V_{AC} and 230 V_{AC} (71.26% and 68.72% respectively) in dotted lines; markers on the curves represent efficiency at 25%, 50%, 75% and 100% of maximum load. At 115 V_{AC}, STEVAL-ISA195V1 is compliant with both standards.

Figure 12. Active mode efficiency vs VIN and comparison with CoC5 and DOE



1.5.4 Light load performance

In version 5 of the Code of Conduct, the power consumption of the power supply when it is not loaded is also considered.

Table 3. Energy consumption criteria for no-load

Nameplate output power (Pno)	Maximum power in no-load for AC-DC EPS
0.3 W < Pno ≤ 49 W	75 mW
50 W < Pno < 250 W	150 mW

The STEVAL-ISA195V1 no-load performance, measured at nominal input voltages (115 V_{AC} and 230 V_{AC}), are well above the requirement, as reported in Table below.

Table 4. Demonstration board input power consumption under no-load

V_{IN} [V_{AC}]	No-load	
	VOUT [V]	P_{IN} [mW]
115	5.70	11.97
230	5.89	16.47

CoC5 also includes requirements on the efficiency when the output load is 10% of the nominal output power. The STEVAL-ISA195V1 is compliant with this requirement, as shown in the following table.

Table 5. CoC5 requirement and performance at 10% output load

Minimum efficiency requirement at 10% of full load		
V_{IN}	STEVAL-ISA195V1 performance	CoC5 req. (P_{OUT} = 1.8 W)
115	70.0%	61.0%
230	65.3%	

Depending on the equipment supplied, there are several criteria to measure the performance of a converter. In particular one requirement for light load performance (EuP lot 6) is that the input power should be less than 500 mW when the converter is loaded with 250 mW. The following table shows how the STEVAL-ISA195V1 board satisfies this requirement, along with efficiency figures for P_{OUT} = 25 mW and P_{OUT} = 50 mW light load conditions.

Table 6. Light load performance

V_{IN} [V_{AC}]	Efficiency%		
	@ P_{OUT} = 25 mW	@ P_{OUT} = 50 mW	@ P_{OUT} = 250 mW
115	54.3%	61.4%	70.4%
230	48.7%	56.7%	65.7%

The following table provides data for another output power (or the efficiency) criterion, when the input power is one watt.

Table 7. Efficiency @ P_{IN} = 1 W

V_{IN} [V_{AC}]	Eff. @ P_{IN} = 1 W [%]
115	71.5
230	69.6

1.6 Functional check

1.6.1 Start-up

The start-up phase at maximum load and 115 V_{AC} and 230 V_{AC} nominal input voltages are shown in Figure 13. Start-up at V_{IN} = 115 V_{AC}, full load and Figure 15. Start-up at V_{IN} = 230 V_{AC}, full load. An internal soft-start function progressively increases the cycle-by-cycle current limitation set point from zero up to I_{DLIM} in 8 steps. This limits drain current during the output voltage rise, thus reducing the stress on the secondary diode. The t_{SS} soft-start time needed for the current limitation to reach its final value is internally set at 8 ms. This function is activated for any converter start-up attempt or after a fault event. The IC has a “pulse skipping” feature, which skips a switching cycle whenever the OCP comparator is triggered within the minimum on-time. The switching frequency is thus halved, down to the minimum allowed value of F_{OSC_MIN} (15 kHz, typ.). By allowing a longer inductor discharge time, this feature helps prevent current runaway: the possible uncontrolled increase in drain current during the very first cycles of converter start-up, due to the initial inability of the system to maintain the volt-second balance when there is a large input-to-output voltage differential. Whenever the OCP comparator is not triggered inside the minimum on-time, a switching cycle is restored, thus doubling the switching frequency up to the nominal frequency F_{OSC}. Pulse skipping and F_{OSC} restoration are evident in and Figure 14. Start-up at V_{IN} = 115 V_{AC}, full load, zoom and Figure 16. Start-up at VIN = 230 V_{AC}, full load, zoom.

Figure 13. Start-up at V_{IN} = 115 V_{AC}, full load

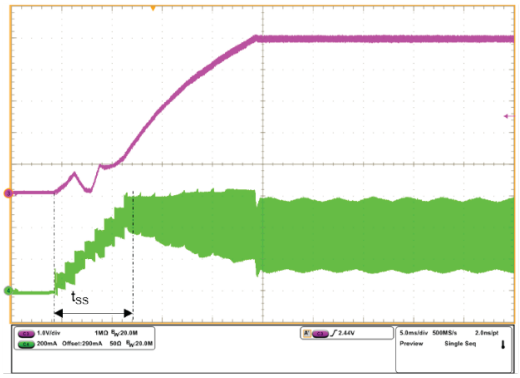


Figure 14. Start-up at V_{IN} = 115 V_{AC}, full load, zoom

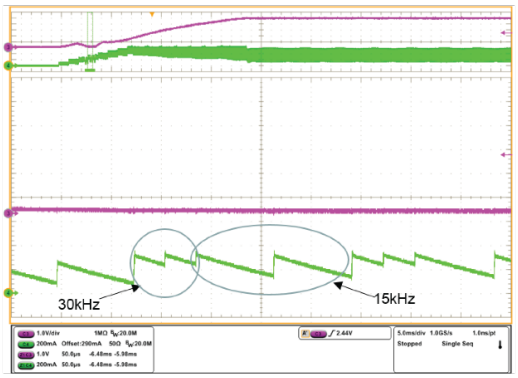


Figure 15. Start-up at V_{IN} = 230 V_{AC}, full load

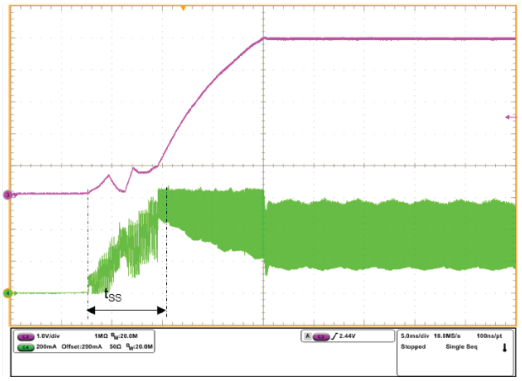
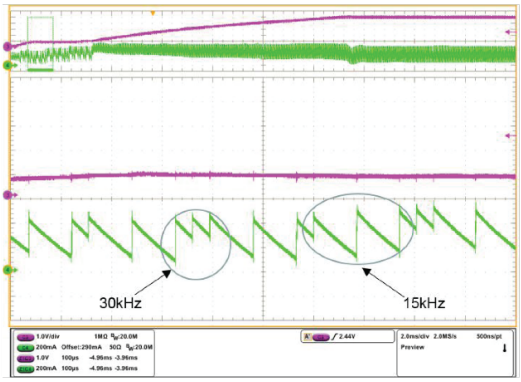


Figure 16. Start-up at VIN = 230 V_{AC}, full load, zoom



The effect of pulse skipping feature is shown in Figure 17. Max. peak current at V_{IN} = 115 V_{AC}, start-up in full load conditions and Figure 18. Max. peak current at V_{IN} = 230 V_{AC}, start-up in full load conditions : the maximum value reached by the peak current at start-up is quite low, both at 115 V_{AC} and at 230 V_{AC}.

Figure 17. Max. peak current at V_{IN} = 115 V_{AC}, start-up in full load conditions

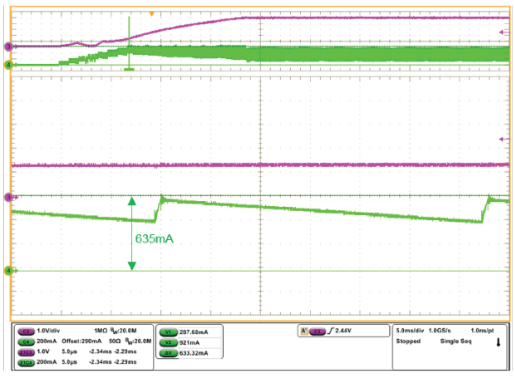
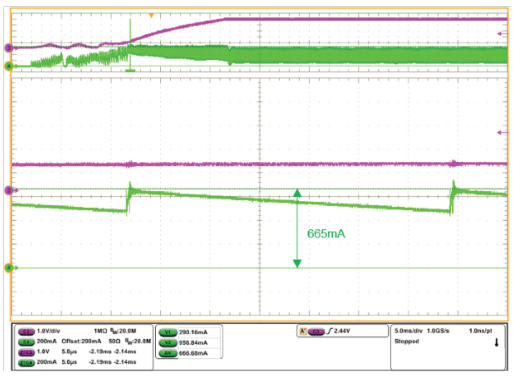


Figure 18. Max. peak current at V_{IN} = 230 V_{AC}, start-up in full load conditions



1.6.2 Overload protection

During an overload or short-circuit, the drain current reaches I_{DLIM} (see Figure 19. Output overload applied: OLP tripping) . For every cycle that this condition is met, an internal OCP counter is incremented and the protection is tripped if the fault is maintained for time t_{OVL} (50 ms typical, set internally): the power section is turned off and the

converter is disabled for time $t_{RESTART}$ (1 s typical). After this time, the IC resumes switching and, if the fault is still present, the protection occurs indefinitely in the same way (see Figure 20. Output overload maintained:OLP steady-state. This ensures a low rate of converter restart attempts for safe operation and extremely low power throughput while avoiding IC overheating in case of repeated fault events. Moreover, every time the protection is tripped, the internal soft start-up function is invoked at restart (Figure 21. Output overload maintained: t_{SS} and t_{OVL}). The IC resumes normal operation when the short is removed. If the short is removed during t_{SS} or t_{OVL}, before the protection is tripped, the counter decrements each cycle down to zero and the protection is not tripped. If the short-circuit is removed during $t_{RESTART}$, the IC waits for the $t_{RESTART}$ period to elapse before resuming switching (Figure 22. OLP: short-circuit removed and auto-restart).

Figure 19. Output overload applied: OLP tripping

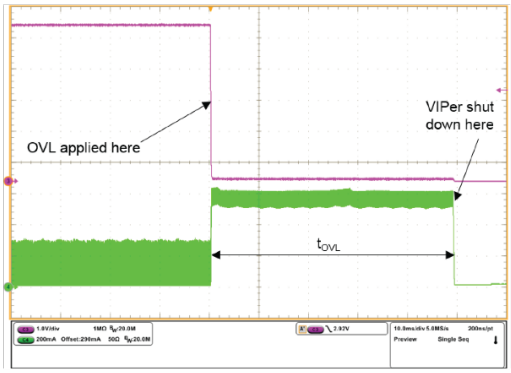


Figure 20. Output overload maintained:OLP steady-state

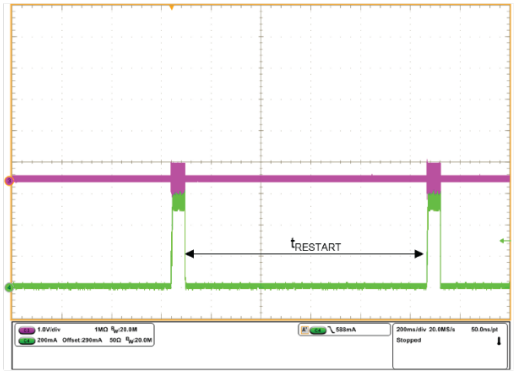


Figure 21. Output overload maintained: t_{SS} and t_{OVL}

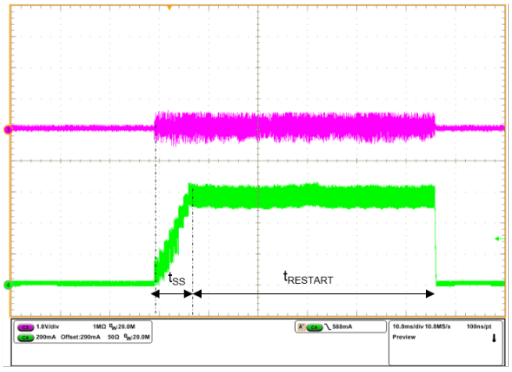
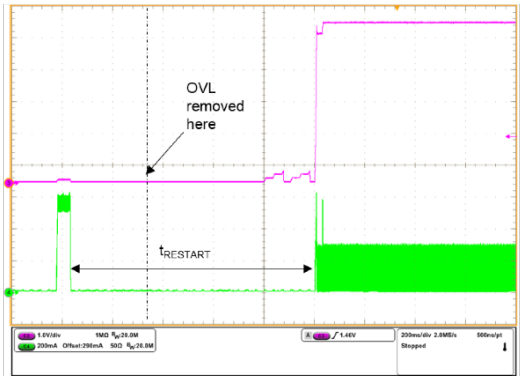


Figure 22. OLP: short-circuit removed and auto-restart



During overload at high V_{IN}, when the ton gets smaller, the I_{DLIM} may be exceeded within the minimum on time, causing the switching frequency to be reduced by pulse skipping function, and the time needed for the OCP counter to reach its end of count increased accordingly. In case of F_{OSC} = 30 kHz, t_{OVL} could range between 50 ms (when pulse skipping is never invoked) and 100 ms (when pulse skipping is always invoked, and the actual switching frequency is always half F_{OSC}). In Figure 23. Output overload @ 230V_{AC}: t_{OVL} increase t_{OVL} is increased to 100 ms. The magnified Figure 24. Output overload @ 230V_{AC}: pulse skipping shows the frequency reduction due to pulse skipping during overload. When the fault is removed, the device waits for $t_{RESTART}$ to elapse before resuming switching via soft-start.

Figure 23. **Output overload @ 230V_{AC}: t_{OVL} increase**

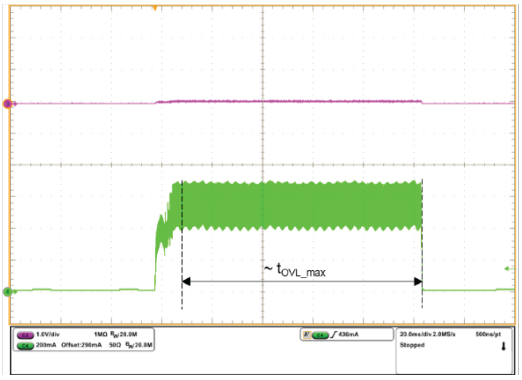
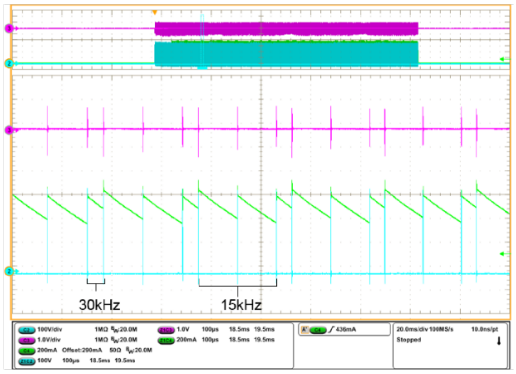


Figure 24. **Output overload @ 230V_{AC}: pulse skipping**



1.7 Thermal measurements

Thermal analysis of the board was performed using an IR camera at 115 V_{AC} and 230 V_{AC} mains input, full load condition. The results are shown in the following figures, where “A” indicates the highest temperature point and “B” the ambient temperature.

Figure 25. **Thermal measurements @ V_{IN} = 115 V_{AC} full load (bottom view)**

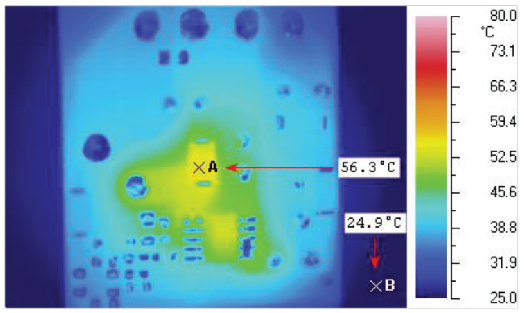


Figure 26. **Thermal measurements @ V_{IN} = 115 V_{AC} full load (top view)**

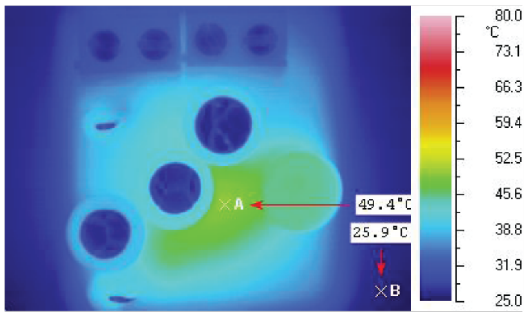


Figure 27. **Thermal measurements @ V_{IN} = 230 V_{AC} full load (bottom view)**

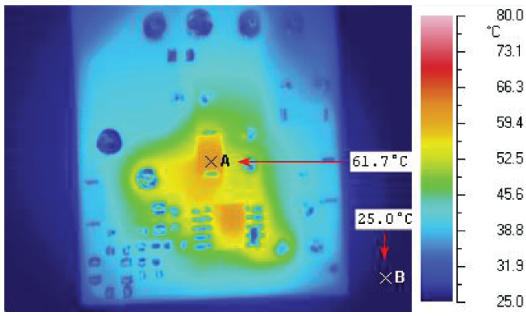
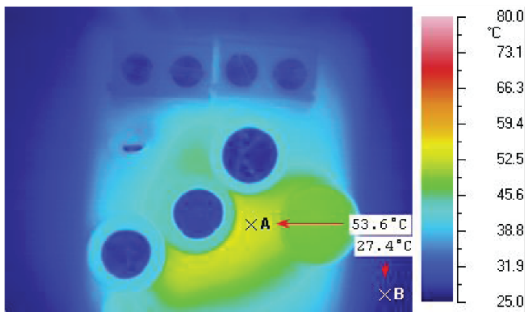


Figure 28. **Thermal measurements @ V_{IN} = 230 V_{AC} full load (top view)**



1.8 EMI measurements

A pre-compliance test for European normative EN55022 (Class B) was performed using an EMC analyzer with average detector and a line impedance stabilization network (LISN).

Figure 29. **EMI measurements with average detector @ 115 VAC, full load, T_{AMB} = 25 °C**

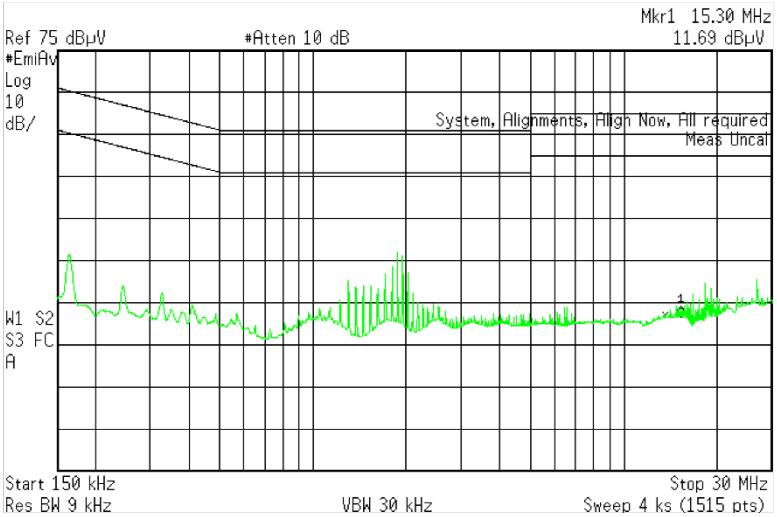
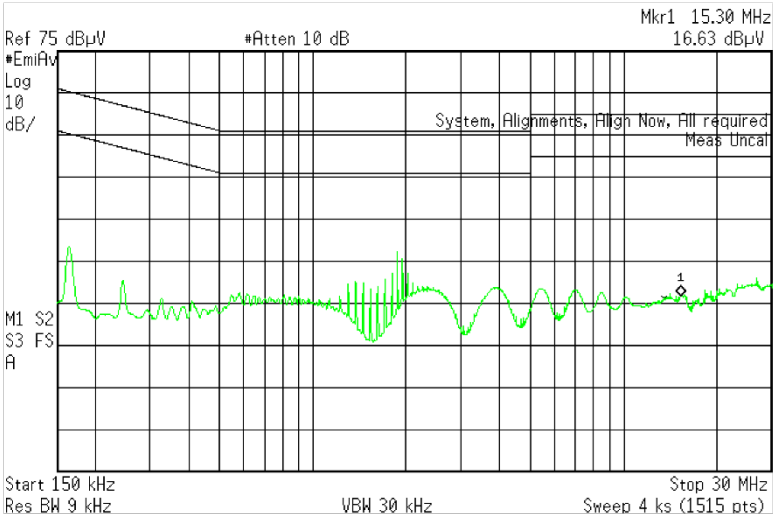


Figure 30. **EMI measurements with average detector @ 230 VAC, full load, T_{AMB} = 25 °C**



1.9 Conclusions

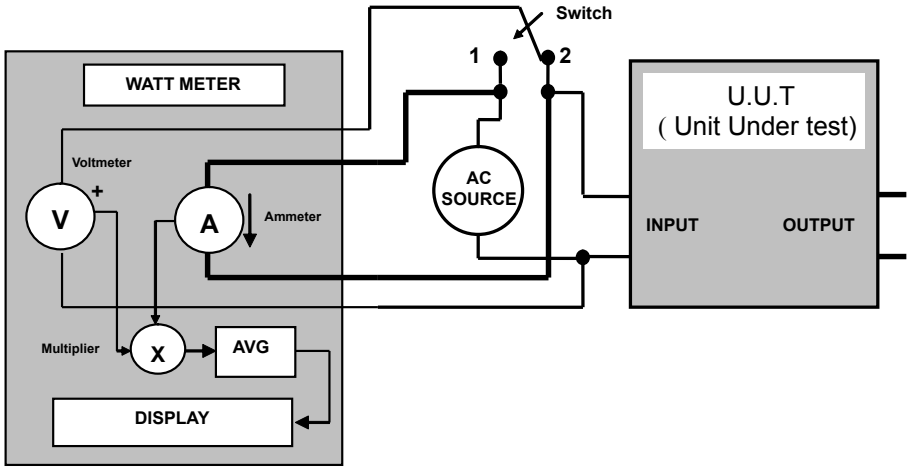
The VIPER11 allows a non-isolated converter to be designed in a simple way and with poor amount of external components. In this document a buck has been described and characterized. Special attention has been dedicated to the light load performance. The efficiency performance has been compared with the most popular requirements for external AC/DC adapter with very good results.

A Appendix (test equipment and measurement of efficiency and low load performance)

The converter input power has been measured using a wattmeter. The wattmeter measures simultaneously the converter input current (using its internal ammeter) and voltage (using its internal voltmeter). The wattmeter is a digital instrument so it samples the current and voltage and converts them in digital forms. The digital samples are then multiplied giving the instantaneous measured power. The sampling frequency is in the range of 20 kHz (or higher depending on the instrument used). The display provides the average measured power, averaging the instantaneous measured power in a short period of time (1 s typ.).

The figure below shows how the wattmeter is connected to the UUT (unit under test) and to the AC source and the wattmeter internal block diagram.

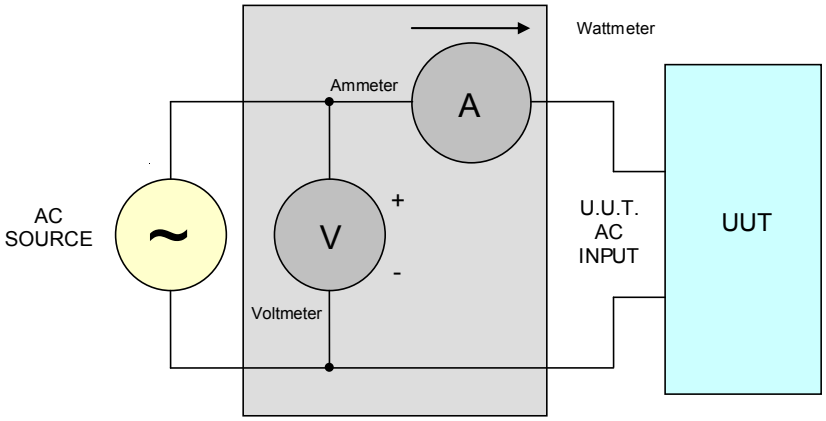
Figure 31. Connections of the UUT to the wattmeter for power measurements



An electronic load has been connected to the output of the power converter (UUT), allowing the converter load current to be set and measured, while the output voltage has been measured by a voltmeter. The output power is the product between load current and output voltage. The ratio between the output power, calculated as previously stated, and the input power, measured by the wattmeter, is the converter efficiency, which has been measured in different input/output conditions.

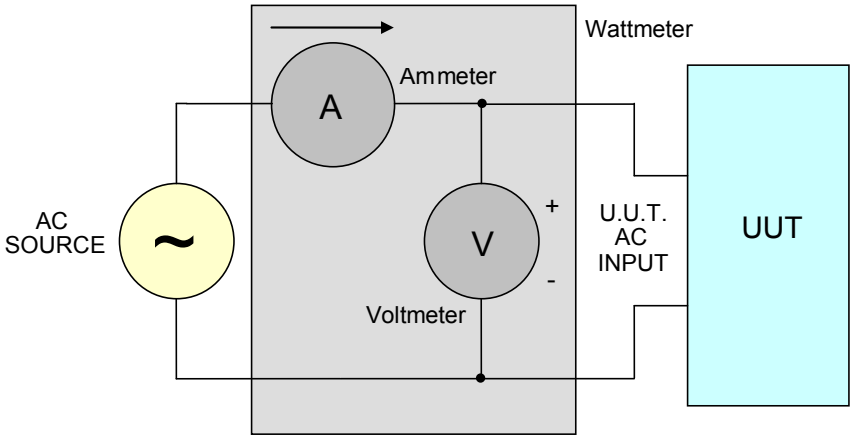
Measuring input power notes With reference to the figure above, the UUT input current causes a voltage drop across the ammeter internal shunt resistance (the ammeter is not ideal so it has an internal resistance higher than zero) and across the cables connecting the wattmeter to the UUT. If the switch of the figure above is in position 1 (see also the simplified scheme of the next figure) this voltage drop causes an input measured voltage higher than the input voltage at the UUT input that, of course, affects the measured power. The voltage drop is generally negligible if the UUT input current is low (for example when we measure the input power of UUT in light load conditions).

Figure 32. Switch in position 1 - setting for standby measurements



In case of high UUT input current (for measurements in heavy load conditions), the voltage drop can be relevant (compared to the UUT real input voltage). If this is the case, the switch in Figure 31. Connections of the UUT to the wattmeter for power measurements should be changed in position 2 (see simplified scheme of figure below) where the UUT input voltage is measured directly to the UUT input terminal and the input current does not affect the measured input voltage.

Figure 33. Switch in position 2 - setting for efficiency measurements



On the other hand, the position of the last figure may introduce a relevant error during light load measurements, when the UUT input current is low and the leakage current inside the voltmeter itself (which is not an ideal instrument and does not have infinite input resistance) is not negligible. This is the reason why it is better to use the setting of Figure 32. Switch in position 1 - setting for standby measurements for light load measurements and Figure 33. Switch in position 2 - setting for efficiency measurements for heavy load measurements.

If it is not clear which measurement scheme has the lesser effect on the result, try with both and register the lower input power value.

As noted in IEC 62301, instantaneous measurements are appropriate when power readings are stable. The UUT is operated at 100% of nameplate output current output for at least 30 minutes (warm-up period) immediately prior to conducting efficiency measurements.

After this warm-up period, the AC input power is monitored for a period of 5 minutes to assess the stability of the UUT. If the power level does not drift by more than 5% from the maximum value observed, the UUT can be considered stable and the measurements can be recorded at the end of the 5 minute period. If AC input power is not stable over a 5 minute period, the average power or accumulated energy is measured over time for both AC input and DC output.

Some wattmeter models allow integrating the measured input power in a time range and then measuring the energy absorbed by the UUT during the integration time. Dividing by the integration time itself the average input power is calculated.

Revision history

Table 8. **Document revision history**

Date	Version	Changes
24-Apr-2018	1	Initial release
10-Jan-2019	2	Minor text changes

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