AN4941
Application note

7 W dual output (-5 V/+7 V) non-isolated flyback converter with capacitive touch sensing using VIPer0P and STM32L052

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Introduction

The STEVAL-ISA192V1 evaluation board is a 7 W double output power supply (-5 V/+7 V) based on non-isolated flyback topology using VIPer0P (zero power off-line high voltage converter) and STM32L052 (ultra-low power ARM® Cortex®-M0 plus microcontroller).

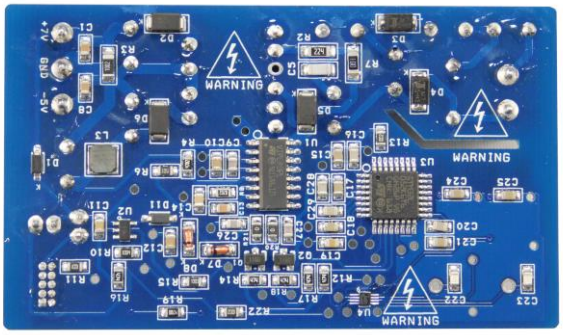
This SMPS is mainly used in electronic appliances that need to be switched on and off during their working cycle through a capacitive touch user interface or push button.

The evaluation board features:

- Smart standby architecture using the zero power mode (ZPM) for capacitive touch sensing in consumer electronics applications
- Enhanced system reliability thanks to VIPer0P 800 V avalanche rugged technology and its embedded protection
- Minimized system input power consumption: less than 30 mW at 230 V_{AC} in ZPM
- IEC55022 Class B conducted EMI compliant, even with reduced EMI filter, thanks to the frequency jittering feature
- IEC61000-4-2 (ESD), IEC61000-4-4 (EFT) and IEC61000-4-5 (Surge) compliant
- RoHS compliant

Figure 1: STEVAL-ISA192V1 evaluation board (top view)

Figure 2: STEVAL-ISA192V1 evaluation board (bottom view)



Contents

List of tables

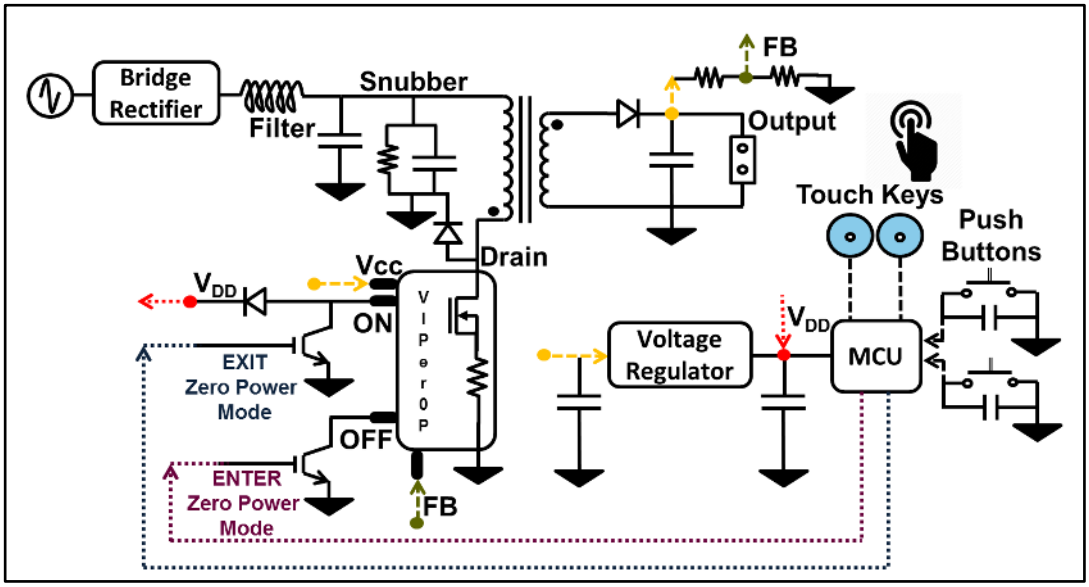
List of figures

1 Electrical specifications and block diagram

Table 1: STEVAL-ISA192V1 electrical specifications

Parameter	Value/Range
Input voltage range	85 V–265 V_{AC}
Output voltage (V_{OUT}) – I	-5 V DC
Output voltage (V_{OUT}) – II	+7 V DC
Maximum output current – I	800 mA
Maximum output current – II	420 mA
Total output power (P_{OUT1}+P_{OUT2})	7 W
Precision of output I regulation	±5%
Max. ambient operating temperature	60 °C
Switching frequency	60 kHz

Figure 3: STEVAL-ISA192V1 block diagram



2 Circuit description

The power supply is based on non-isolated flyback topology. The input section includes a resistor (R1) for inrush current limiting, a diode (D3) and a Pi filter for EMC suppression.

The FB pin is the inverting input of an error amplifier and is an accurate 1.2 V voltage reference with respect to EAGND. This pin is a separate ground which can float down to -20 V with respect to the ground of the device (SGND). This allows the negative output voltage (V_{OUT}-I) to be set and tightly regulated by simply connecting EAGND to the negative rail and to a voltage divider among FB, EAGND and SGND, according to:

Equation 1

$$|V_{OUT1}| = 1.2V \cdot \left(1 + \frac{R6}{R4}\right)$$

The secondary output (V_{OUT}-II) is semi-regulated to +7 V by magnetic coupling through the two output windings turn ratio. The CRC network from COMP (the error amplifier output) to SGND pin provides frequency compensation to the feedback loop that regulates the main output voltage. PGND (the power section ground reference) is connected to SGND with the shortest track and with the lowest impedance, to avoid mismatches between the IC signal ground references and the IC power.

In normal operation, the system behaves as a standard flyback converter.

The key feature of VIPer0P is its zero power mode (ZPM), an idle state where all the internal blocks are switched off and there is no switching activity (so no voltage nor power available at the output). VIPer0P enters ZPM if the OFF pin is pulled to SGND for more than 10 ms and exits ZPM (resuming normal switching) if the ON pin is pulled to SGND for more than 20 µs.

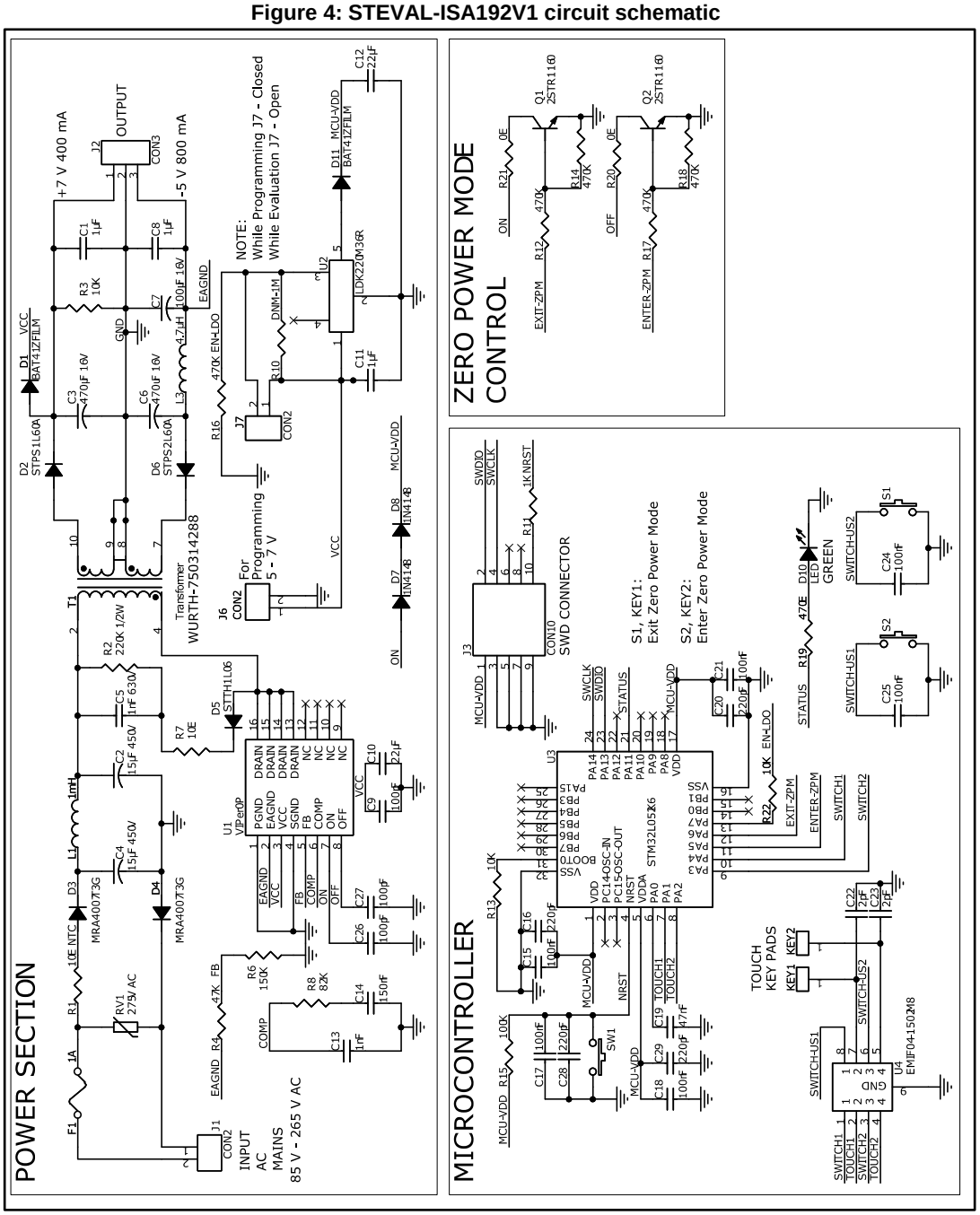
The system enters ZPM upon a specific user command decoded by the microcontroller which actually supervises the operation of the appliance (see *Table 7: "ZPM: switching modes"*).

In ZPM, the V_{CC} pin is charged to an internal clamp and supplies ON and OFF pins through 50 kΩ pull-up resistors, which makes it possible to source a few micro amperes at about 4 V from both pins.

In the case of STEVAL-ISA192V1, the ON pin is used to keep the MCU (featuring ultra-low voltage and ultra-low standby consumption) alive during ZPM, as shown in *Figure 3: "STEVAL-ISA192V1 block diagram"*.

3 Schematic diagram

Figure 4: STEVAL-ISA192V1 circuit schematic



4 Bill of materials

Table 2: STEVAL-ISA192V1 bill of materials

Item	Q.ty	Ref.	Part / Value	Description	Manufacturer	Order code
1	1	U1	VIPer0P SO16N	AC-DC converter	ST	VIPER0PLD
2	1	U2	LDK220M36R SOT23-5L	DC-DC converter	ST	LDK220M36R
3	1	U3	STM32L052K6 LQFP32	32-bit MCU	ST	STM32L052K6T6
4	1	U4	EMIF04-1502M8 Micro QFN 1.7 mm x 1.5 mm	EMI filter and ESD protection	ST	EMIF04-1502M8
5	1	D2	STPS1L60A SMA	Power Schottky rectifier	ST	STPS1L60A
6	1	D6	STPS2L60A SMA	Power Schottky rectifier	ST	STPS2L60A
7	3	D5	STTH1L06 SMA	Ultrafast diode	ST	STTH1L06A
8	2	D1, D11	BAT54 SOD-123	Schottky diode	ST	BAT54ZFILM
9	2	Q1, Q2	2STR1160 SOT-23	NPN transistor	ST	2STR1160
10	2	D3, D4	IN4007 1000 V/1 A SMA	Rectifier diode	ONSemiconductors	MRA4007T3G
11	2	D7, D8	1N4148 SOD-80	Signal diode	Fairchild Semiconductor	LL4148
12	1	D10	SMD 1206	Green LED	ANY	ANY
13	3	C1, C8, C11	10 µF, 16 V, ±10%, SMD, 0805	Ceramic capacitors	ANY	ANY
14	2	C2, C4	15 µF, 450 V, ±20%, 10 mm	Electrolytic capacitors	Nichicon	UVC2G150MPD
15	2	C3, C6	470 µF, 16 V, ±20%, 10 mm	Electrolytic capacitors	ANY	ANY
16	1	C5	1 nF, 630 V, ±5%, SMD 1206	Ceramic capacitor	TDK	C3216C0G2J102JT
17	1	C7	100 µF, 16 V, ±20%, 10 mm	Electrolytic capacitor	ANY	ANY

Item	Q.ty	Ref.	Part / Value	Description	Manufacturer	Order code
18	3	C9, C26, C27	100 pF, 16 V, ±10%, SMD, 0805	Ceramic capacitors	ANY	ANY
19	2	C10, C12	22 µF, 16 V, ±10%, SMD, 0805	Ceramic capacitors	ANY	ANY
20	4	C16, C20, C28, C29	220 pF, ±10%, SMD, 0805	Ceramic capacitors	ANY	ANY
21	1	C13	1 nF, 16 V, ±10%, SMD, 0805	Ceramic capacitor	ANY	ANY
22	1	C14	150 nF, 16 V, ±10%, SMD, 0805	Ceramic capacitor	ANY	ANY
23	6	C15, C17, C18, C21, C24, C25	100 nF, 16 V, ±10%, SMD, 0805	Ceramic capacitors	ANY	ANY
24	1	C19	47 nF, 16 V, ±10%, SMD, 0805	Ceramic capacitor	ANY	ANY
25	2	C22, C23	2 pF, 16 V, ±10%, SMD, 0805	Ceramic capacitors	ANY	ANY
26	1	R1	10E NTC, ±20%	Inrush current limiter	EPCOS	B57153S100M
27	1	R7	10E, 1/4 W, ±5%, SMD, 1206		ANY	ANY
28	1	R2	220 K, 1/4 W, ±10%, SMD, 1206		ANY	ANY
29	1	R3	10 K, 1/4 W, ±10%, SMD, 1206		ANY	ANY
30	2	R13, R22	10 K, 1/8 W, ±10%, SMD, 0805		ANY	ANY
31	1	R4	47 K, 1/8 W, ±1%, SMD, 0805		ANY	ANY

Item	Q.ty	Ref.	Part / Value	Description	Manufacturer	Order code
32	2	R20, R21	0E, 1/8 W, ±10%, SMD, 0805		ANY	ANY
33	1	R6	150 K, 1/8 W, ±1%, SMD, 0805		ANY	ANY
34	1	R8	82 K, 1/8 W, ±10%, SMD, 0805		ANY	ANY
35	1	R15	100 K, 1/8 W, ±10%, SMD, 0805		ANY	ANY
36	1	R11	1 K, 1/8 W, ±10%, SMD, 0805		ANY	ANY
37	5	R12, R14, R16, R17, R18	470 K, 1/8 W, ±10%, SMD, 0805		ANY	ANY
38	1	R19	470E, 1/8 W, ±10%, SMD, 0805		ANY	ANY
39	1	R10	1M-DNM, 1/8 W, ±10%, SMD 0805		ANY	ANY
40	1	L1	1 mH, 200 mA, ±5%	Inductor	EPCOS	B82144A2105J
41	1	L3	4.7 µH, 1 A, ±20%, SMD	Inductor	Taiyo Yuden	NR4012T4R7M
42	1	T1	2.5 mH, ±10%	Transformer	Wurth Elektronik	750314288
43	1	J1	CON2, 5 mm	I/P terminal block	ANY	ANY
44	1	J2	CON3, 5 mm	O/P terminal block	ANY	ANY
45	2	J6, J7	2.54 mm		ANY	ANY
46	1	J3	CON10	SWD connector	CNC Tech	3220-10-0100-00
47	1	SW1	SPST, 0.05 A, SMD 2-PIN	Push button	Multicomp	9471898
48	2	S1, S2	Switch Tactile - SPST 0.05A SMD 4-PIN	Push button	TE Connectivity	FSM4JSMATR

Item	Q.ty	Ref.	Part / Value	Description	Manufacturer	Order code
49	1	RV1	MOV 275 Vac 7.5mm	Varistor	Wurth Elektronik	820 412 711
50	1	F1	1 A, 5 mm	Fuse	LittleFuse	39211000000

5 Transformer

Table 3: Transformer characteristics

Parameter	Value	Test conditions
Manufacturer	Wurth	
Order code	750314288 Rev0	
Primary inductance (pins 3 - 4)	2.5 mH ±10%	Measured at 10 kHz, 0.1 V_{AC}
Leakage inductance	42 to 84 µH	Measured at 10 kHz, 0.1 V_{AC}
Primary to secondary 1 turn ratio (4 - 2)/(8 - 7)	(14.23):(1.00), ±1%	
Primary to secondary 2 turn ratio (4 - 2)/(10 - 9)	(10.27):(1.00), ±1%	

Figure 5: Transformer electrical and pin pattern diagram

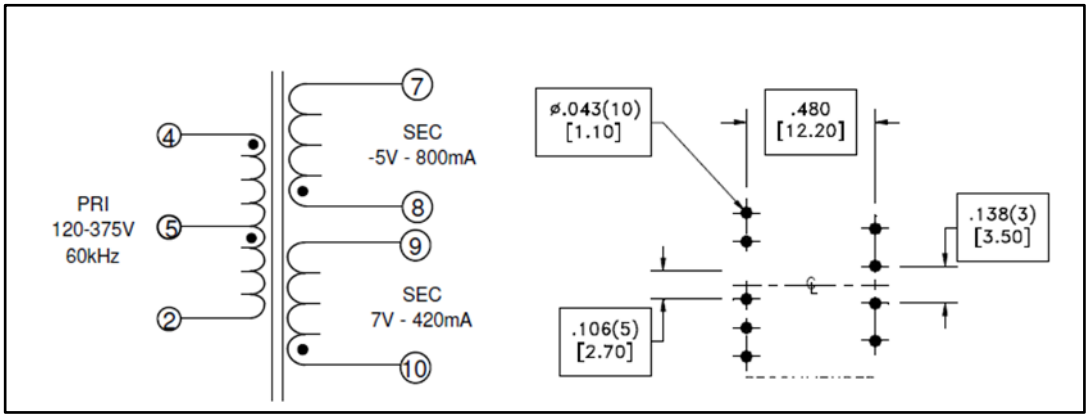
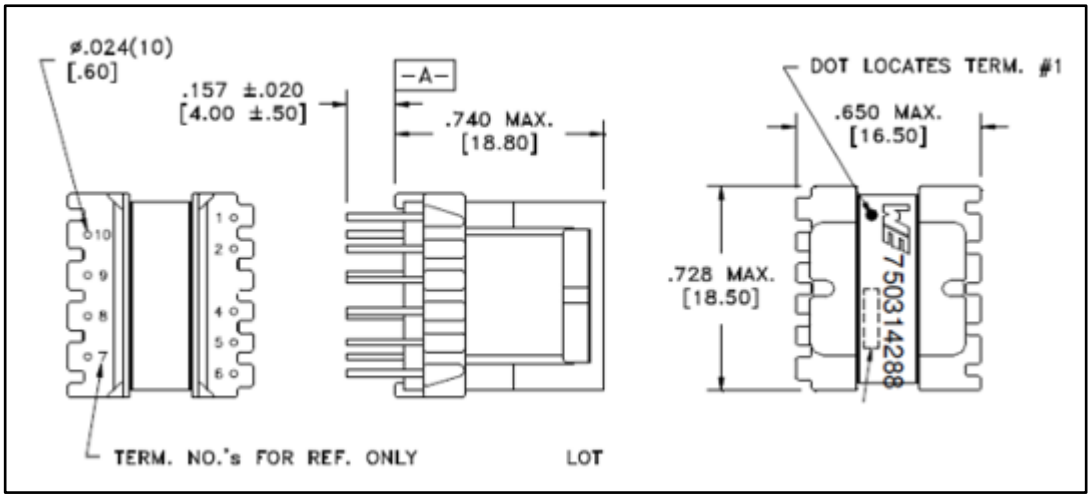


Figure 6: Transformer size and dot location



6 Testing the board

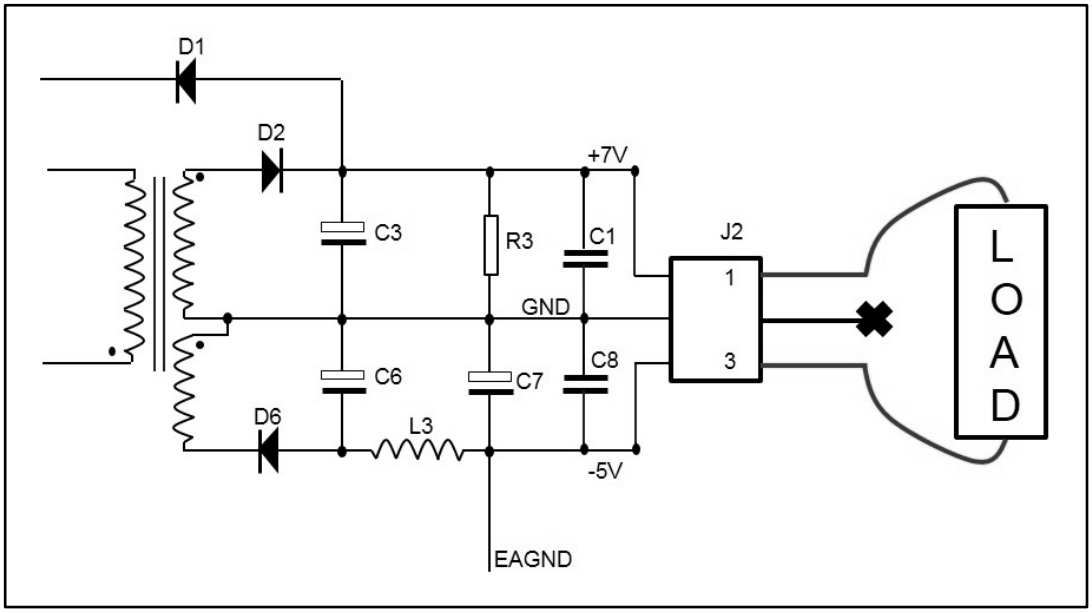
At board power on, LED D10 blinks five times to indicate that the evaluation board has been powered via input mains voltage.

6.1 Efficiency

The active mode efficiency is defined as the average of the efficiencies measured at 25%, 50%, 75% and 100% of the maximum load, at nominal input voltages (115 V_{AC} and 230 V_{AC}). External power supplies need to comply with the Code of Conduct, version 5 "Active mode efficiency" criterion, which, for a power throughput of 7 W, states an active mode efficiency higher than 80% (CoC5). Another standard to be applied is the DOE (department of energy) recommendation, whose active mode efficiency requirement for the same power throughput is 79.8%.

The above mentioned requirements only refer to single output converters, which is not the case of the STEVAL-ISA192V1, which has two outputs and a microcontroller powered up for capacitive touch sensing. However, just to give an indication of its performance, the measurements were conducted by connecting the load across the V_{OUT})-I and V_{OUT}-II lines, as shown in the following figure.

Figure 7: STEVAL-ISA192V1 output load connection

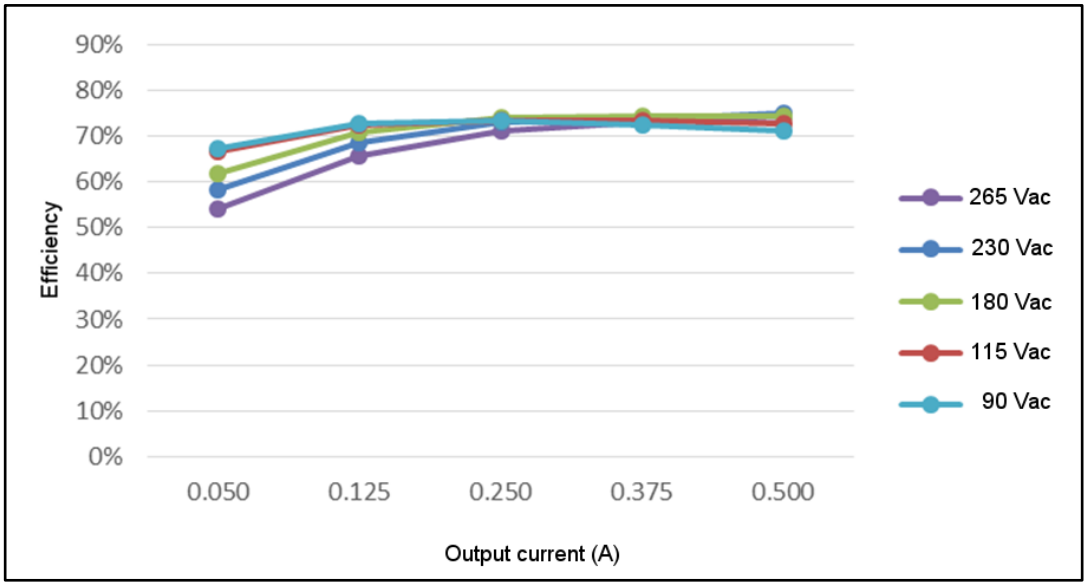


The efficiency of the power supply is being adversely affected by the double voltage drop across D2 and D6, and also by the current consumed in powering the microcontroller on. In an SMPS with a single secondary rectifier, it is reasonable to expect 4-5% higher efficiency values.

Table 4: Active mode efficiency

V_{IN}	STEVAL-ISA192V1 performance	CoC5 requirements for P_{OUT} = 7 W	DOE requirement for P_{OUT} = 7 W
115 V_{AC}	72.1%	80%	79.8%
230 V_{AC}	70.3%		

Figure 8: Efficiency vs. output current load



The maximum output load considered in the figure above is 0.5 A (P_{OUT}=12*0.5=6 W).

Figure 9: Efficiency vs. input voltage at different output current load

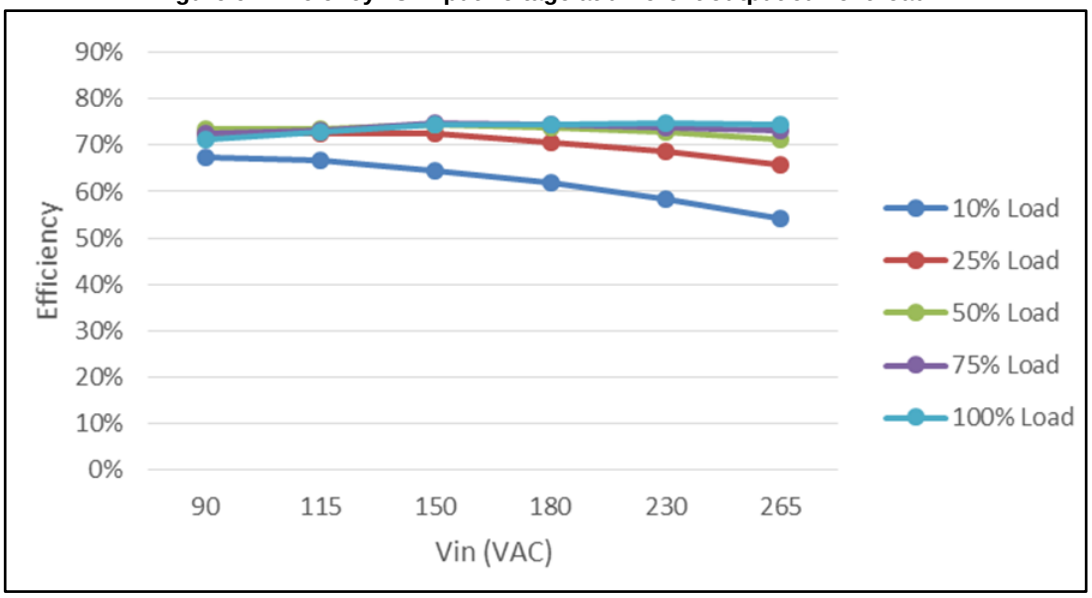


Figure 10: Output voltage load regulation

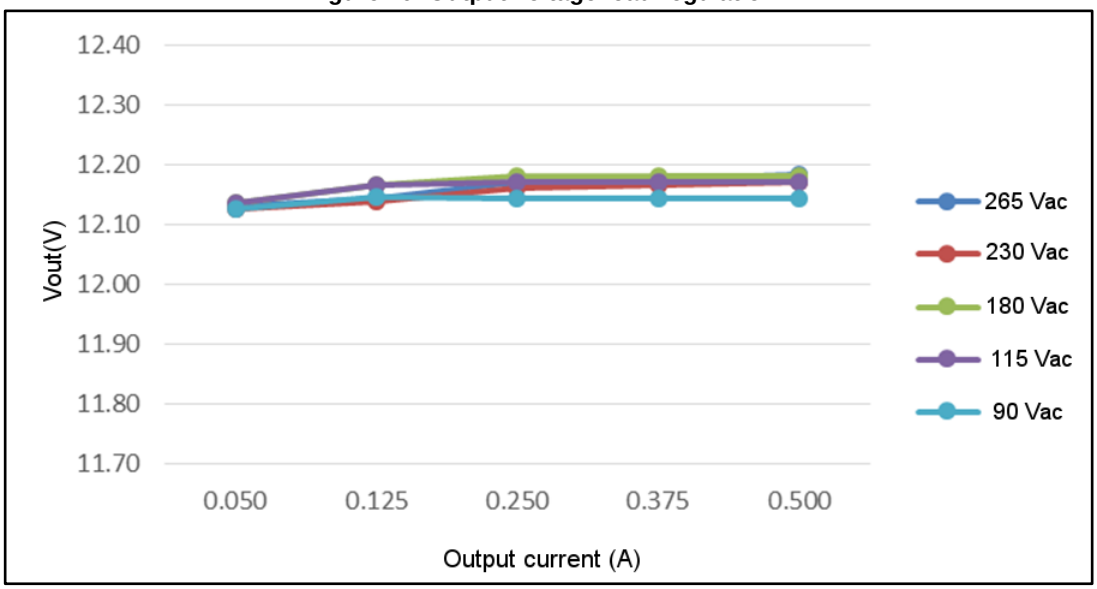
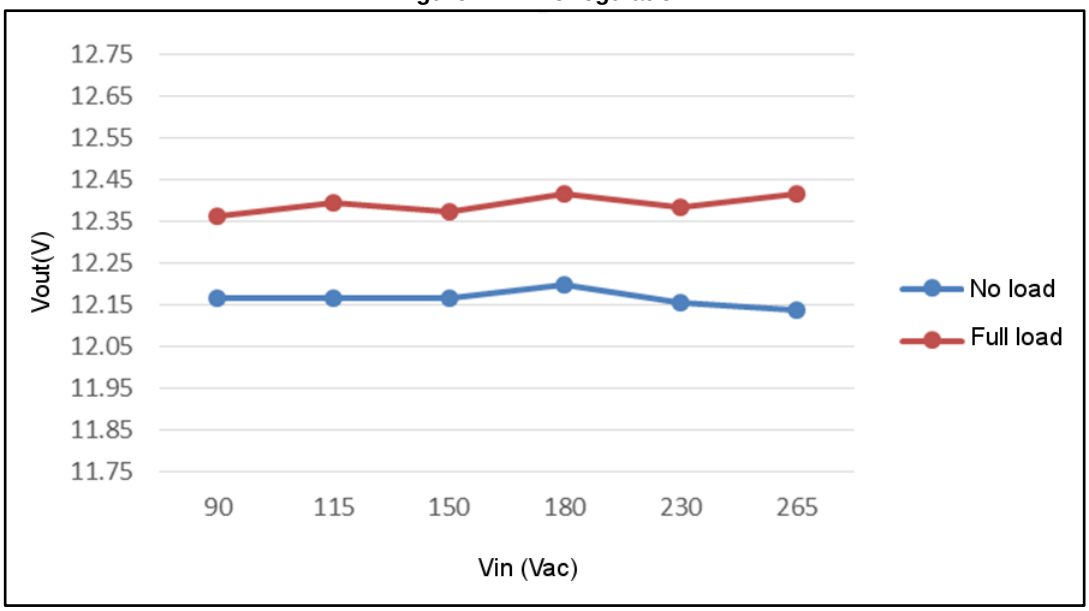


Figure 11: Line regulation



In version 5 of the Code of Conduct, the power supply power consumption is also considered when it is not loaded.

The table below shows the compliance criteria for EPS converters with nominal output power below 49 W and the evaluation board no-load input power consumption measurements. Performance is well above the requirements.

In the same table, the ZPM consumption of the evaluation board is also reported. In ZPM, the power consumption from the mains at 230 V_{AC} can go below 5 mW; the STEVAL-ISA192V1 consumption is 30 mW due to the MCU polling strategy implemented at firmware level.

Table 5: CoC5 energy consumption criteria for no load and STEVAL-ISA192V1 evaluation board performance

Max P_{IN} req. in no load (0.3 W < $P_{no\ load}$ < 49 W)	STEVAL-ISA192V1 P_{IN} consumption		
CoC5	V_{IN} = 230 V_{AC}	No load	ZPM
75mW		30mW	29mW

6.2 Typical waveforms

ViPer0P drain voltage and output voltage waveforms under full load conditions for the different input voltages are reported in the following figures.

Figure 12: VIPer0P drain voltage and output voltages at 85 V_{AC}

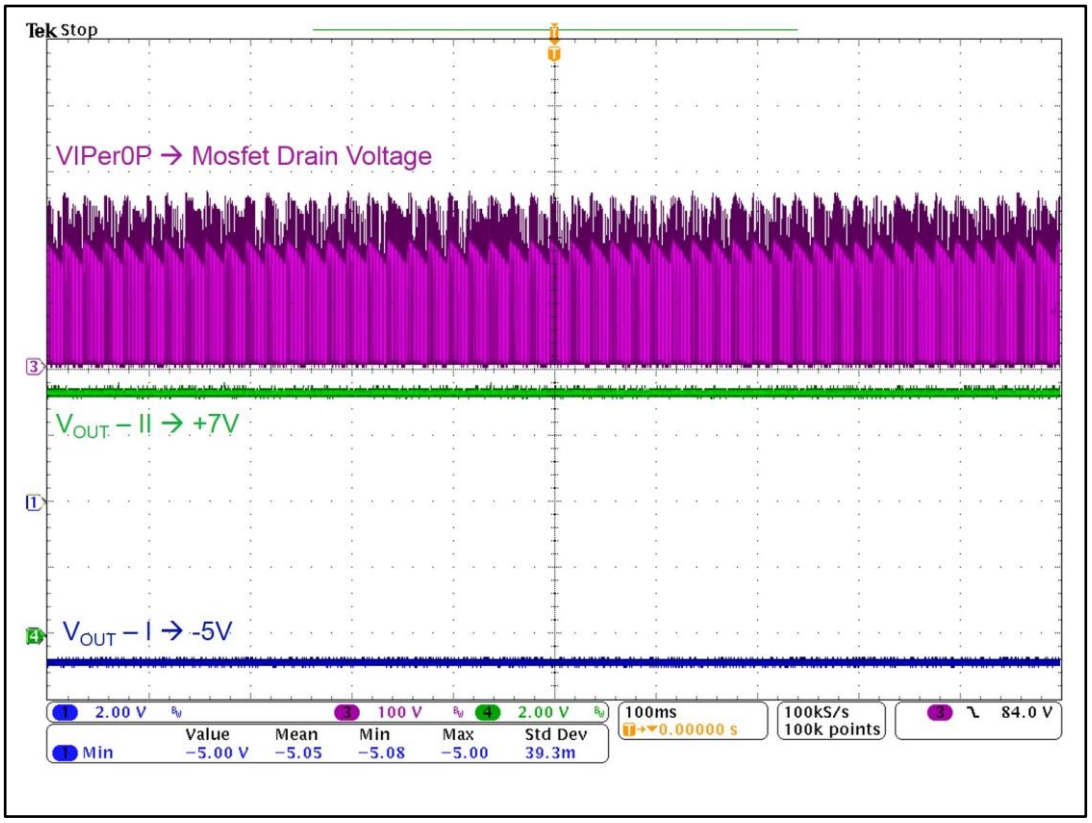


Figure 13: VIPer0P drain voltage and output voltages at 85 V_{AC}: zoom

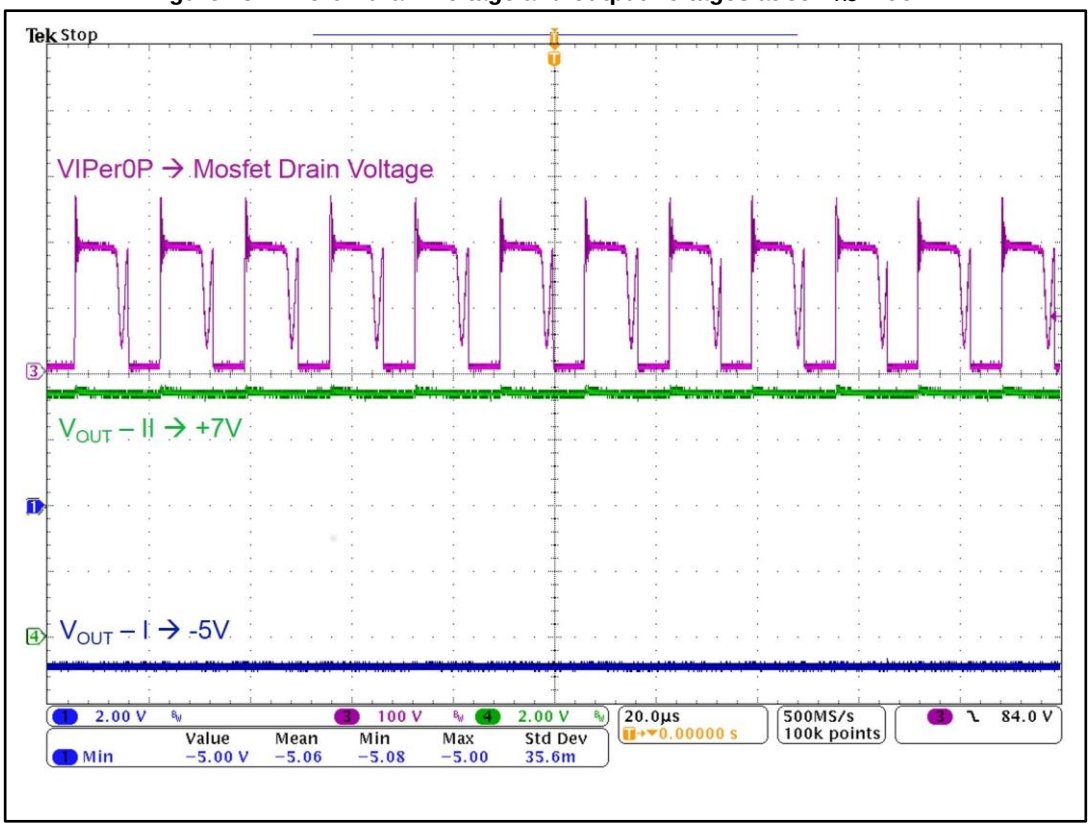


Figure 14: VIPer0P drain voltage and output voltages at 110 V_{AC}

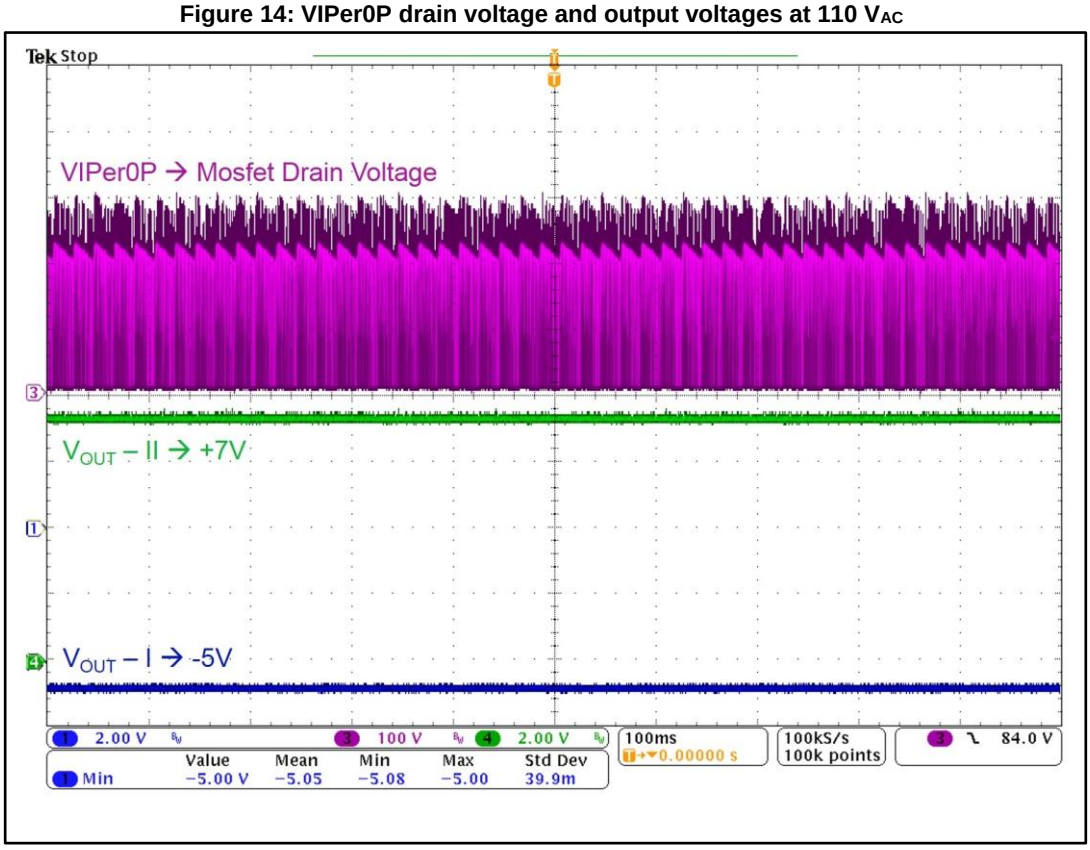


Figure 15: VIPer0P drain voltage and output voltages at 110 V_{AC}: zoom

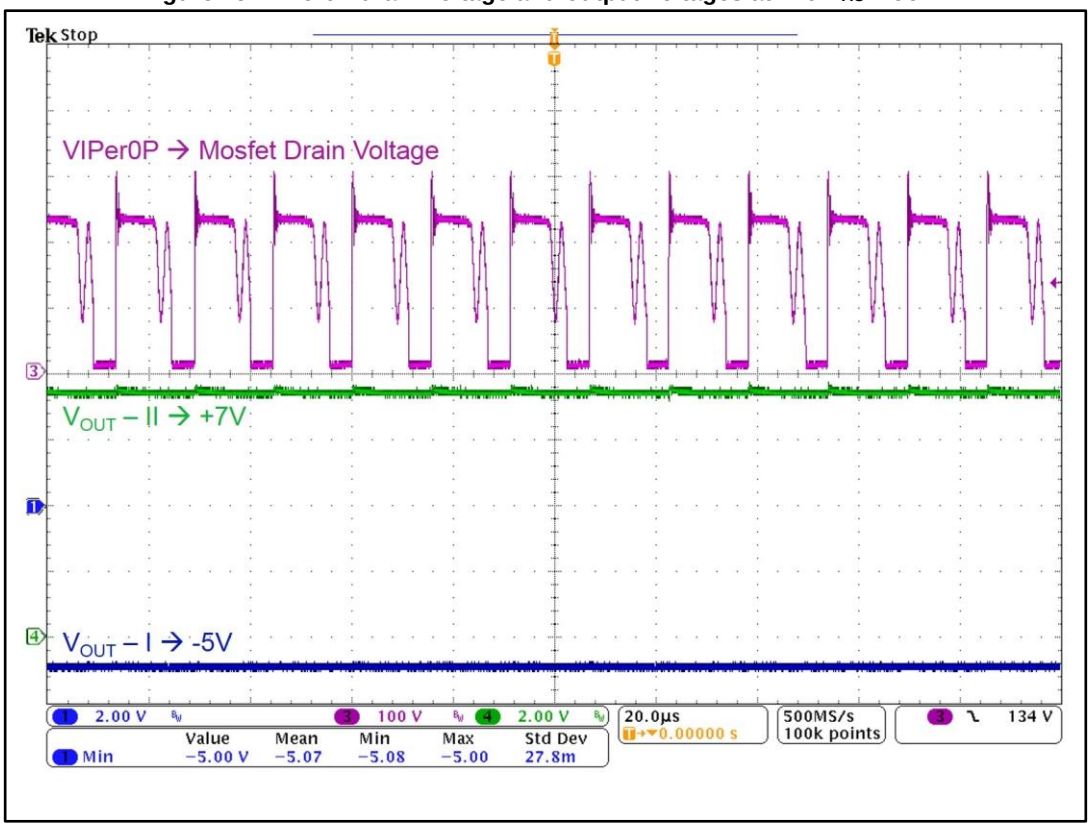


Figure 16: VIPer0P drain voltage and output voltages at 230 V_{AC}

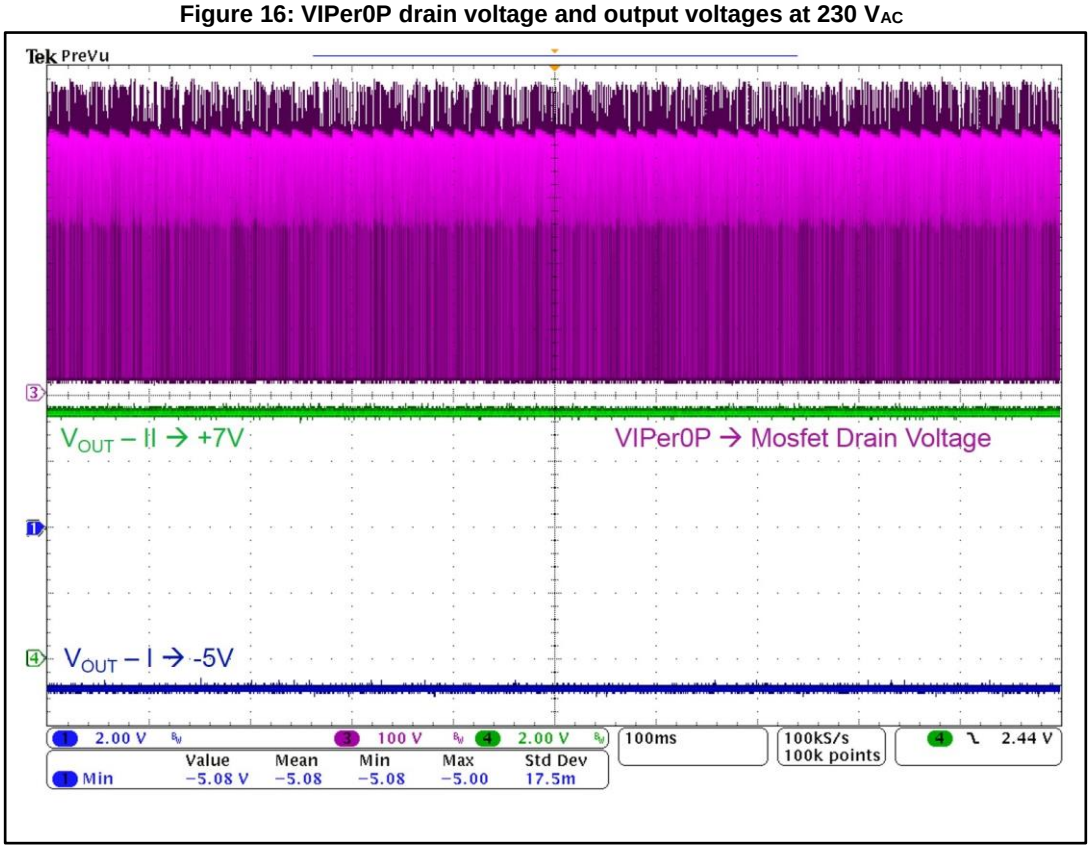


Figure 17: VIPer0P drain voltage and output voltages at 230 V_{AC}: zoom

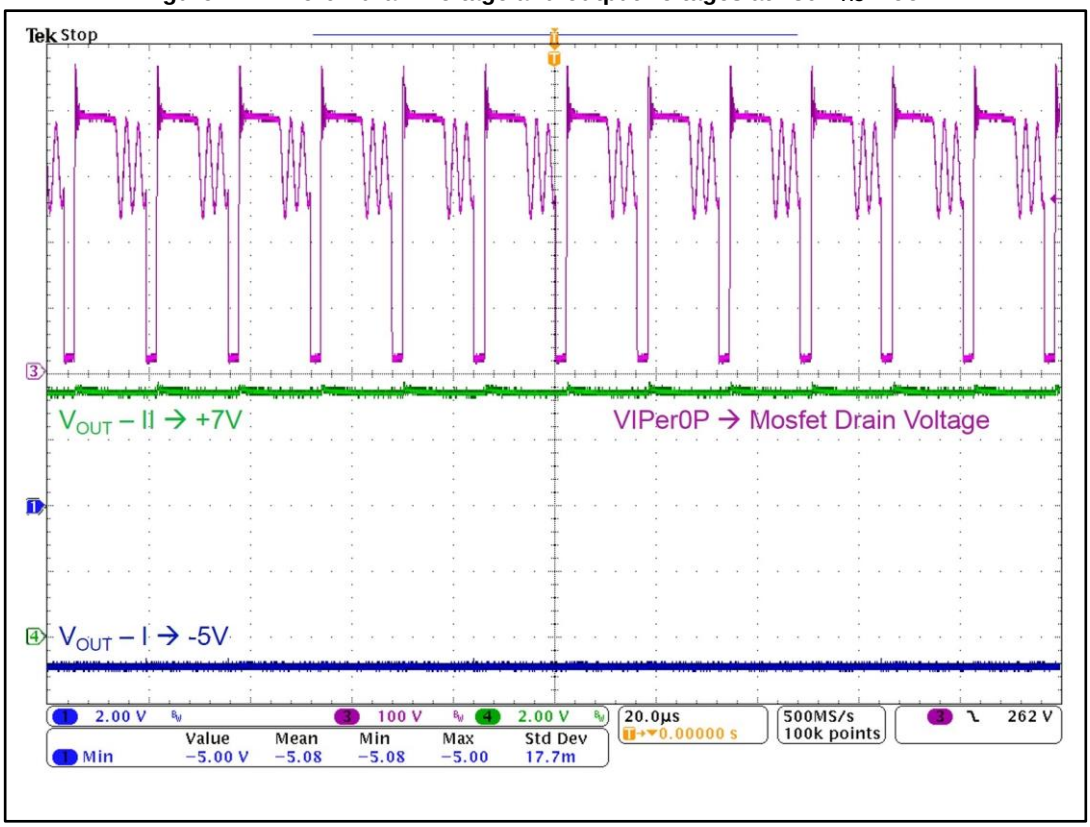


Figure 18: VIPer0P drain voltage and output voltages at 265 V_{AC}

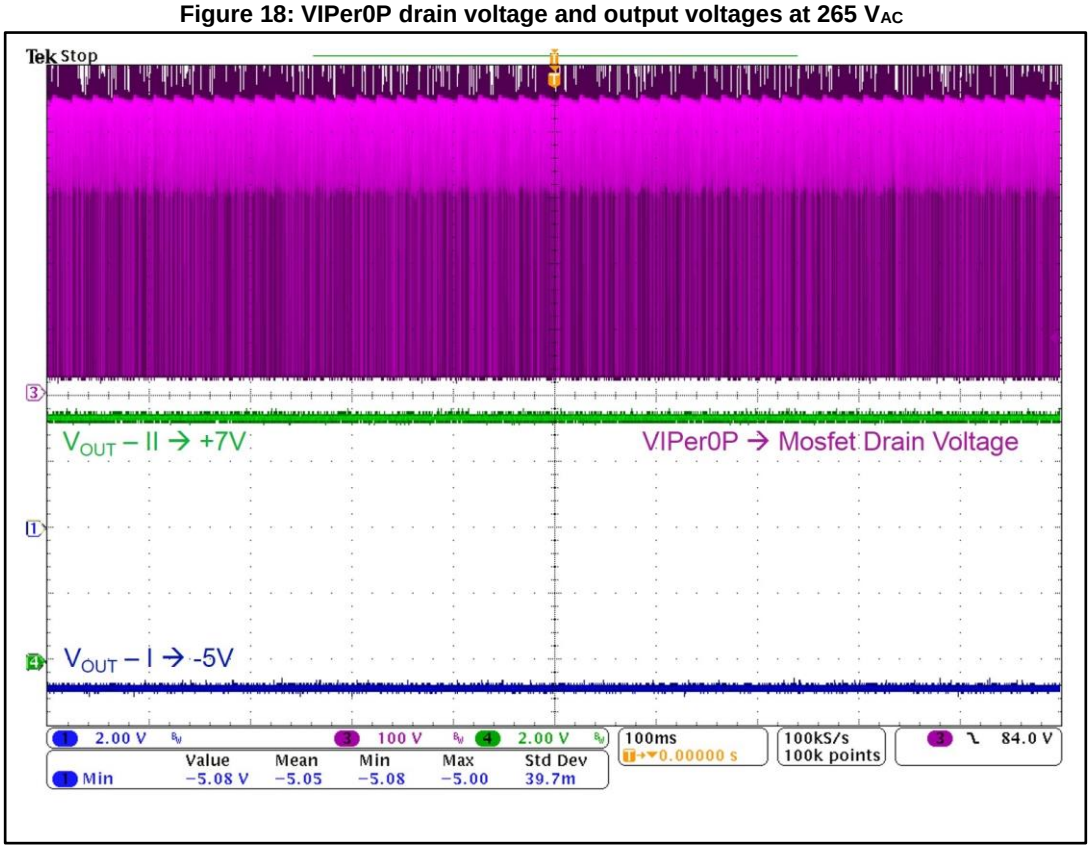
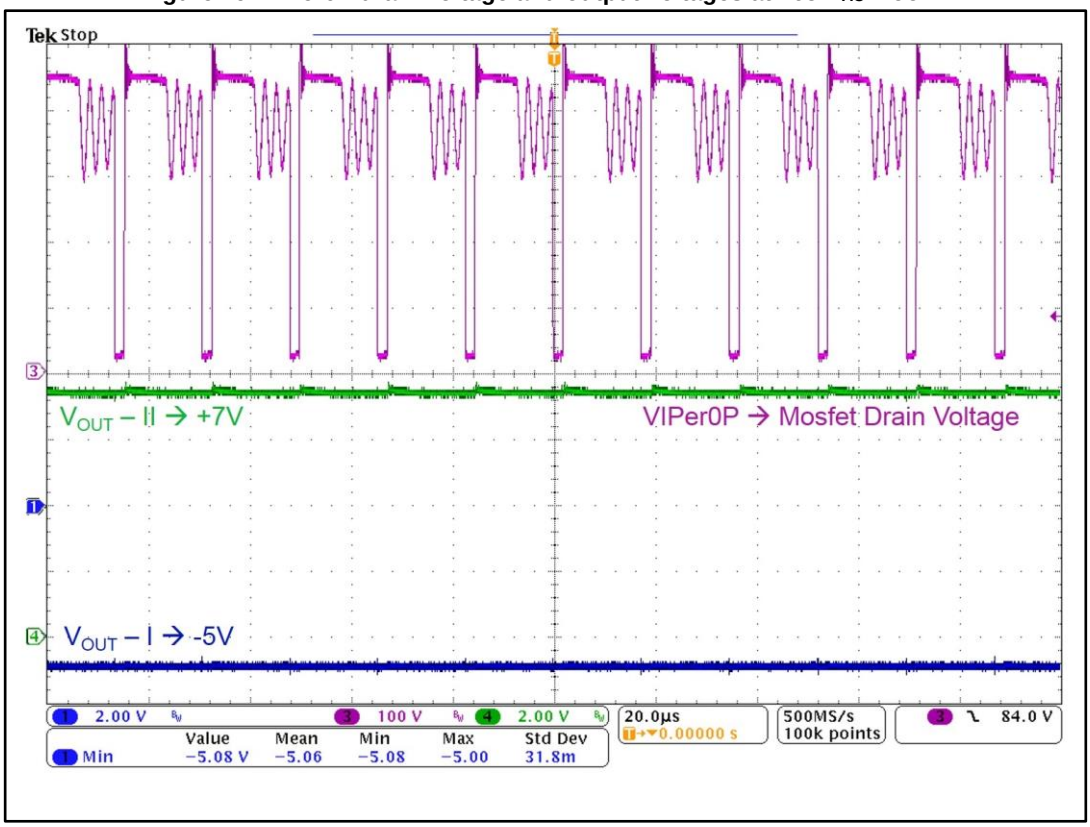


Figure 19: VIPer0P drain voltage and output voltages at 265 V_{AC}: zoom



7 VIPer0P features

VIPer0P is a high-voltage converter that smartly integrates an 800 V avalanche rugged power MOSFET with PWM current mode control.

This IC is capable of meeting the most stringent energy saving standards thanks to its very low consumption and pulse frequency modulation under light load.

The ZPM feature allows the VIPer0P to work in an idle state (the system is totally shut down). A microcontroller can be easily connected to the IC for smart ZPM management and it can be supplied by the IC itself during the idle state.

The embedded HV startup, sense FET, error amplifier and oscillator with jitter allow a complete application to be designed with a minimum number of components.

In flyback non-isolated topology, a negative output voltage is easily set thanks to the integrated error amplifier with separate ground (for further details, refer to AN4836: “STEVAL-ISA174V1: VIPer0P 7W double output non-isolated flyback” and VIPer0P datasheet on www.st.com).

7.1 Zero power mode (ZPM) interface with microcontroller

In normal operation, STEVAL-ISA192V1 behaves as a standard flyback converter. Upon a specific user command decoded by the microcontroller, the system enters the zero power mode: there is no switching activity, thus, no voltage is available at the output.

In this particular case, the microcontroller still remains ON and may also be used to switch OFF the main load (in case of larger appliances like washing machines, etc.).

The key blocks of the VIPer0P that remain alive are the “Zero-Power Logic” block and the resistive Vcc pull-ups, providing some microamperes at about 4 V from ON and OFF pins, so either of them can be used to provide a small current to supply the microcontroller during ZPM.

STEVAL-ISA192V1 is equipped with two push buttons and two capacitive touch switches, which can be used to enter or exit ZPM as per the following table.

Table 6: STEVAL-ISA192V1 user interface

STEVAL-ISA192V1 user interface	Enter ZPM	Exit ZPM
Capacitive touch	S2	S1
Push buttons	KEY2	KEY1

STEVAL-ISA192V1 enters the ZPM by pulling VIPer0P OFF pin to SGND for more than 10 ms (see *Figure 21: "Entering ZPM"*).

The evaluation board exits the ZPM by pulling VIPer0P ON pin to SGND for more than 20 µs (see *Figure 22: "Exit from ZPM"*).

Table 7: ZPM: switching modes

ENTER ZPM from normal mode	Exit ZPM to normal mode
OFF pin is forced to SGND for more than 10 ms	ON pin is forced to SGND for more than 20 µs

The ZPM is characterized by the following features:

- no switching activity, nor voltage or power output;
- HV current source charges V_{CC} at 13 V and does not perform its usual functions;
- all IC circuits, except the ones needed to exit ZPM, are turned off, reducing the controller consumption to the minimum.

In ZPM the power consumption from the mains at 230 V_{AC} can go below 5 mW; the STEVAL-ISA192V1 consumption is 30 mW: to keep capacitive touch active, the microcontroller (MCU) polls at fixed time interval by enabling voltage regulator.

Figure 20: Capacitive touch management during ZPM

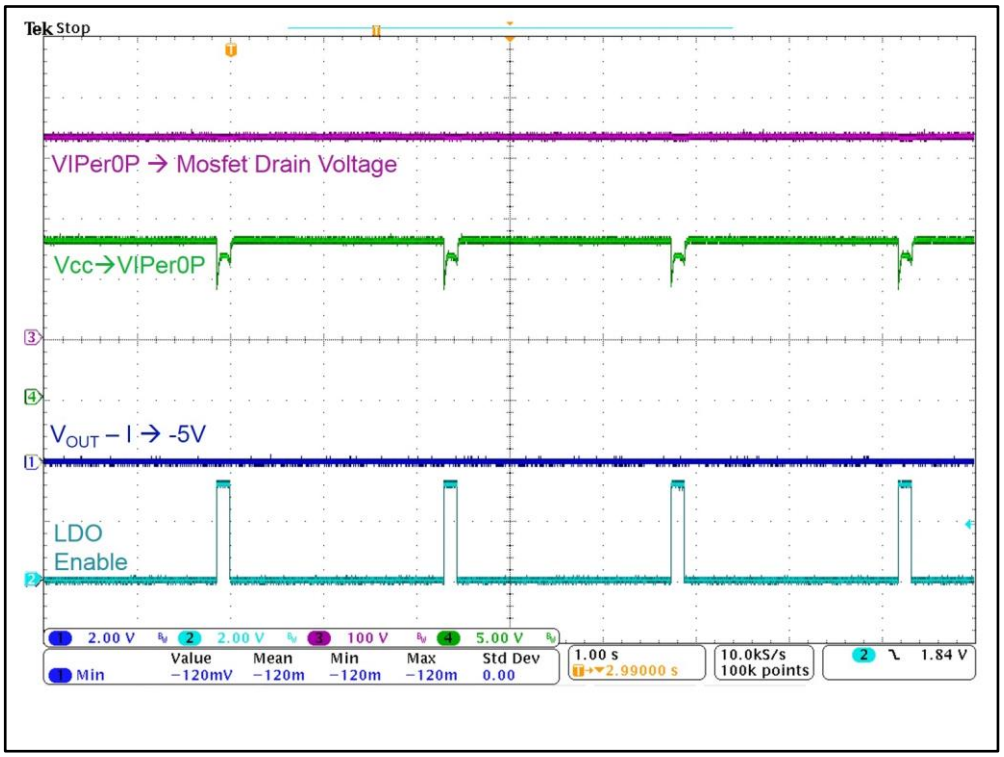


Figure 21: Entering ZPM

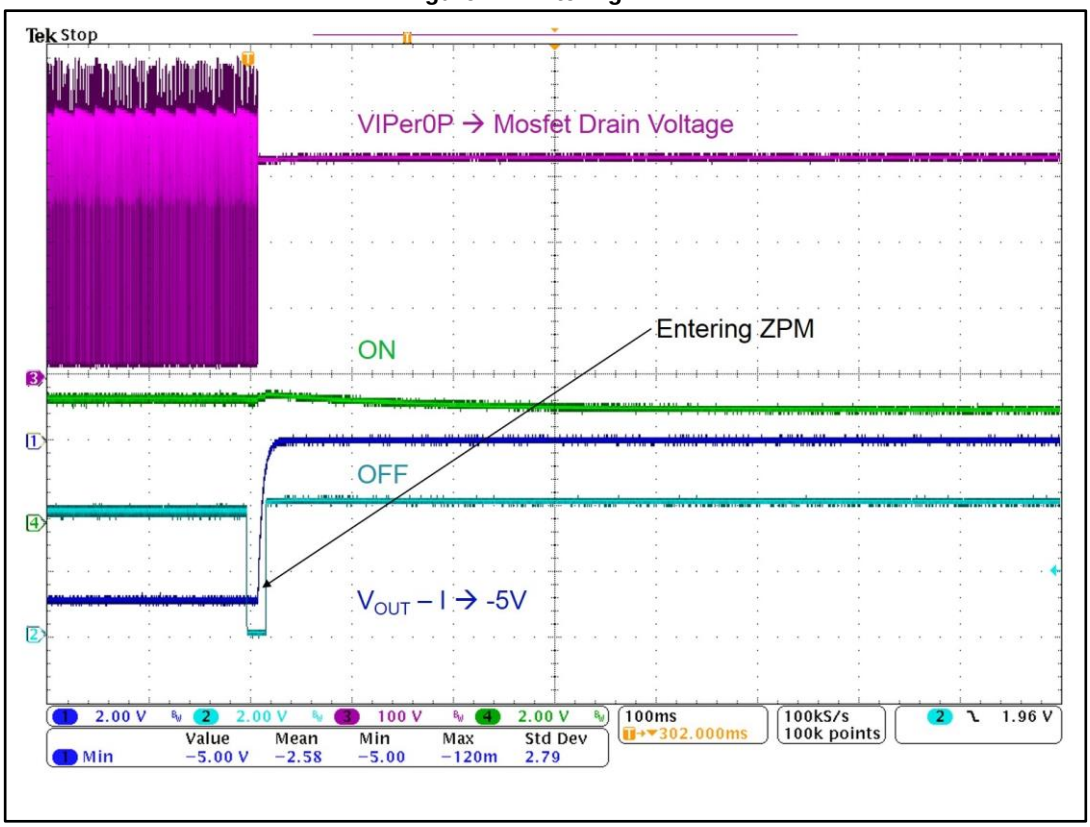
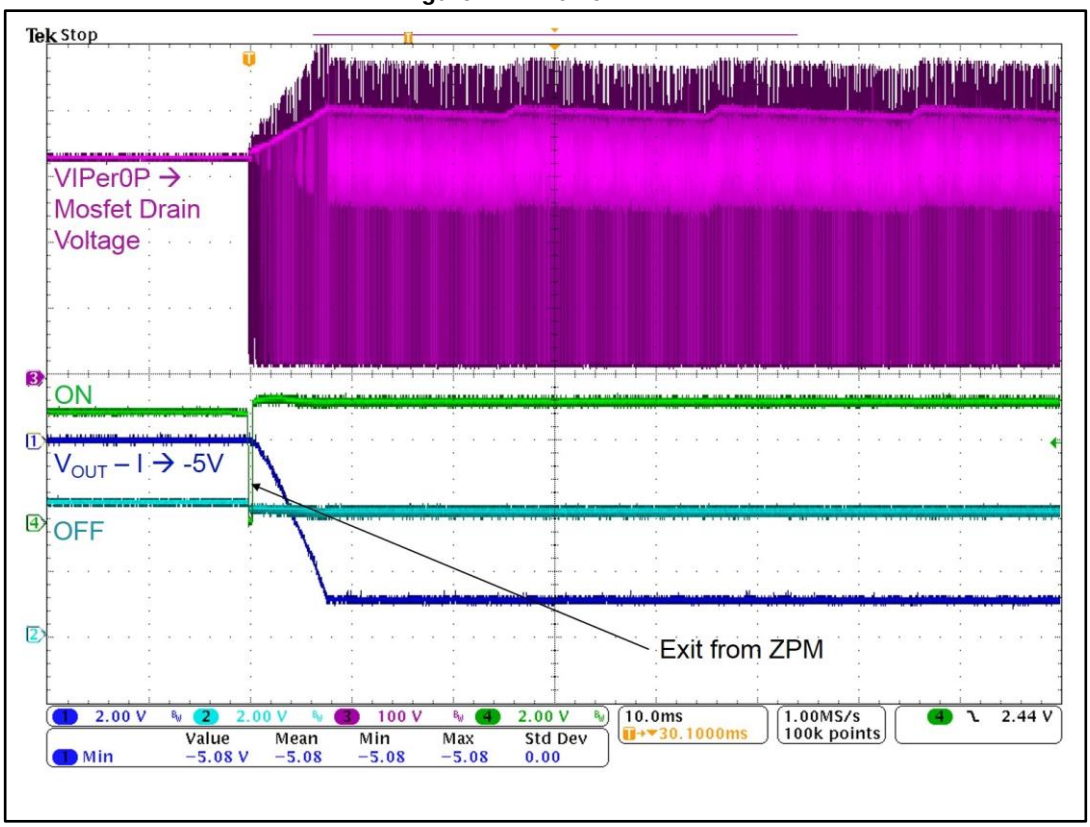


Figure 22: Exit from ZPM



During exit from zero power mode, the evaluation board LED D10 blinks three times to indicate evaluation board exit from the ZPM.

8 Firmware implementation

The STEVAL-ISA192V1 uses the VIPer0P ZPM feature through a sophisticated algorithm in the STM32 ROM as shown in *Figure 23: "Firmware implementation"*.

The CPU is powered from LDO when the SMPS is in normal switching and during ZPM CPU is powered from VIPer0P ON pin through D7 and D8 series diode.

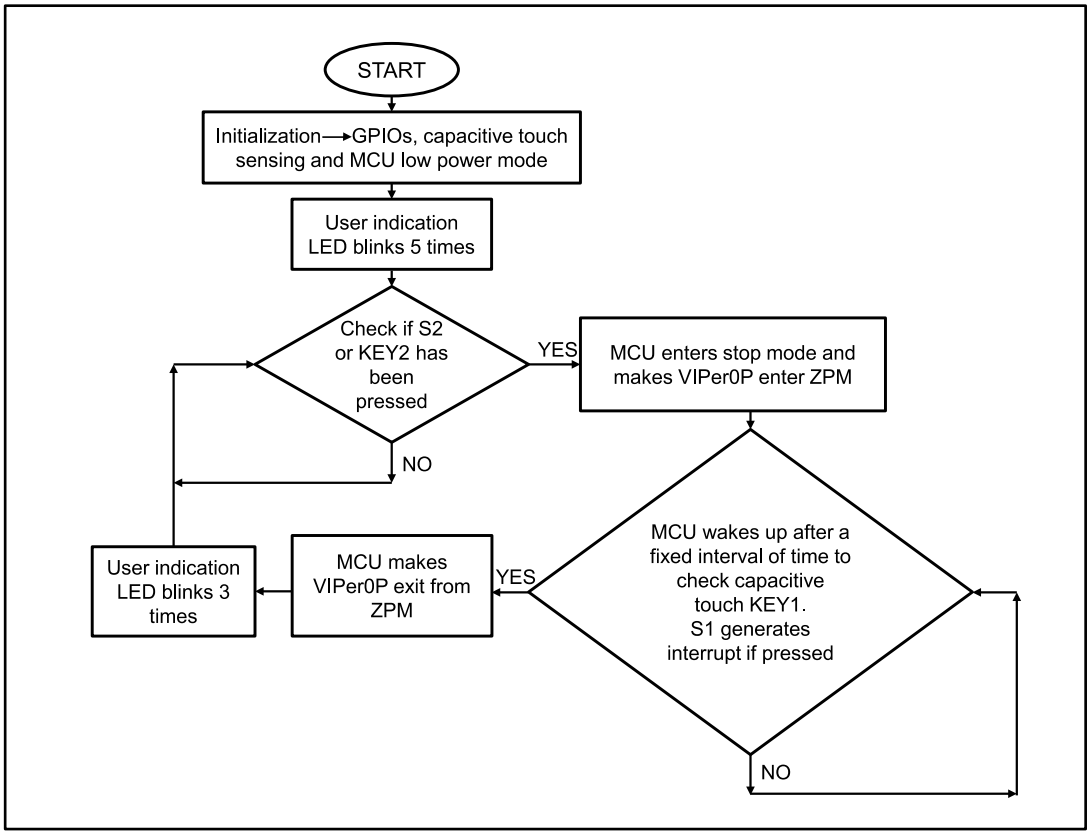
During normal switching, SWITCH S2 (push button) and KEY2 (capacitive touch) can be used to make VIPer0P enter ZPM. SWITCH S2 is connected to a microcontroller through a digital input PA3 GPIO pin and it is configured in interrupt mode. KEY 2 is connected to a microcontroller through a TSC_G1_IO3.

The microcontroller continuously polls to check if there is any capacitive touch. On a valid press, the microcontroller pulls OFF pin to SGND. After making VIPer0P enter ZPM, the microcontroller itself enters stop mode for low power consumption.

SWITCH S1 (push button) and KEY1 (capacitive touch) can be used to make VIPer0P exit from ZPM. SWITCH S1 is connected to a microcontroller through a digital input PA4 GPIO pin and it is configured as a wake up interrupt for the microcontroller. KEY 2 is connected to a microcontroller through a TSC_G1_IO2.

The microcontroller wakes up after a configured interval of time and check if there is any capacitive touch: if not, the microcontroller enters stop mode again. On a valid press, the microcontroller pulls ON pin to SGND. The time interval is a continuous polling of capacitive touch from the final user perspective.

Figure 23: Firmware implementation



9 Feedback loop calculations

For design calculations, transfer function and compensation loop, refer to AN4836 “STEVAL-ISA174V1: VIPer0P 7W double output non-isolated flyback” and VIPer0P datasheet on www.st.com.

10 Thermal measurements

A thermal analysis of the board was performed using an IR camera at 110 V_{AC} and 230 V_{AC} mains input, under full load condition with an ambient temperature of 25°C. The results are shown in the following figures.

Figure 24: STEVAL-ISA192V1 thermal measurement at 110 V_{AC} (top side)

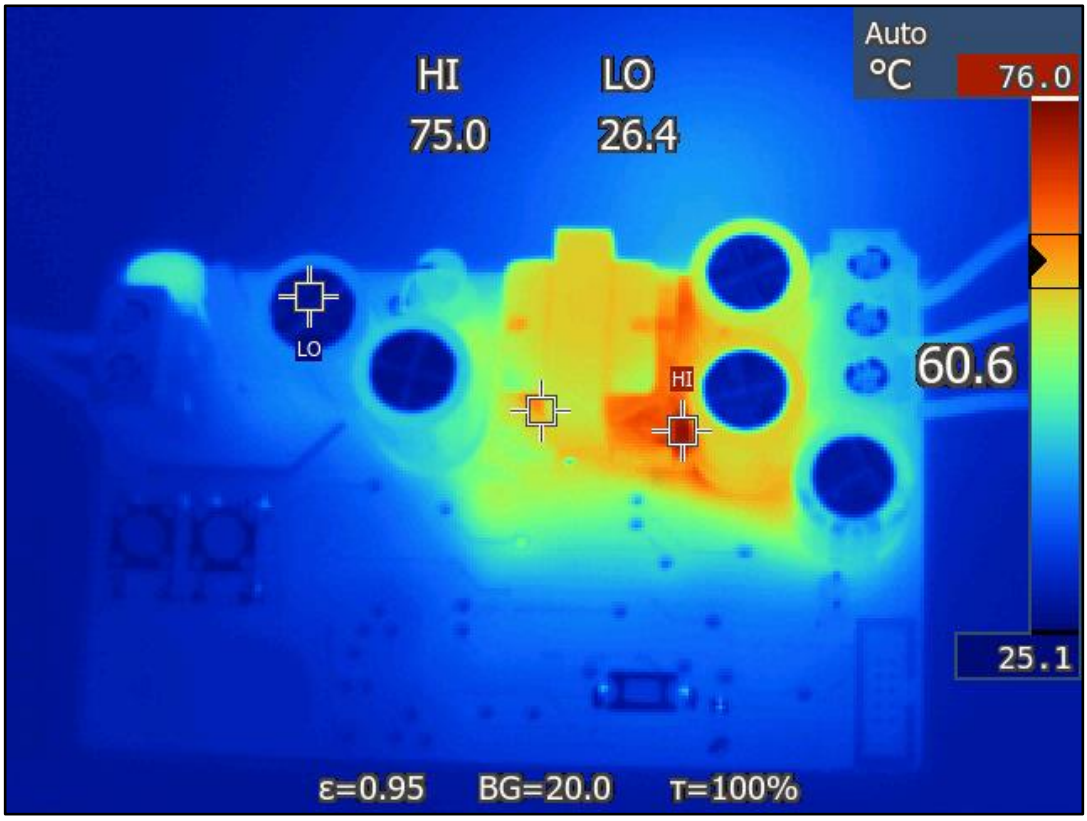


Figure 25: STEVAL-ISA192V1 thermal measurement at 110 V_{AC} (bottom side)

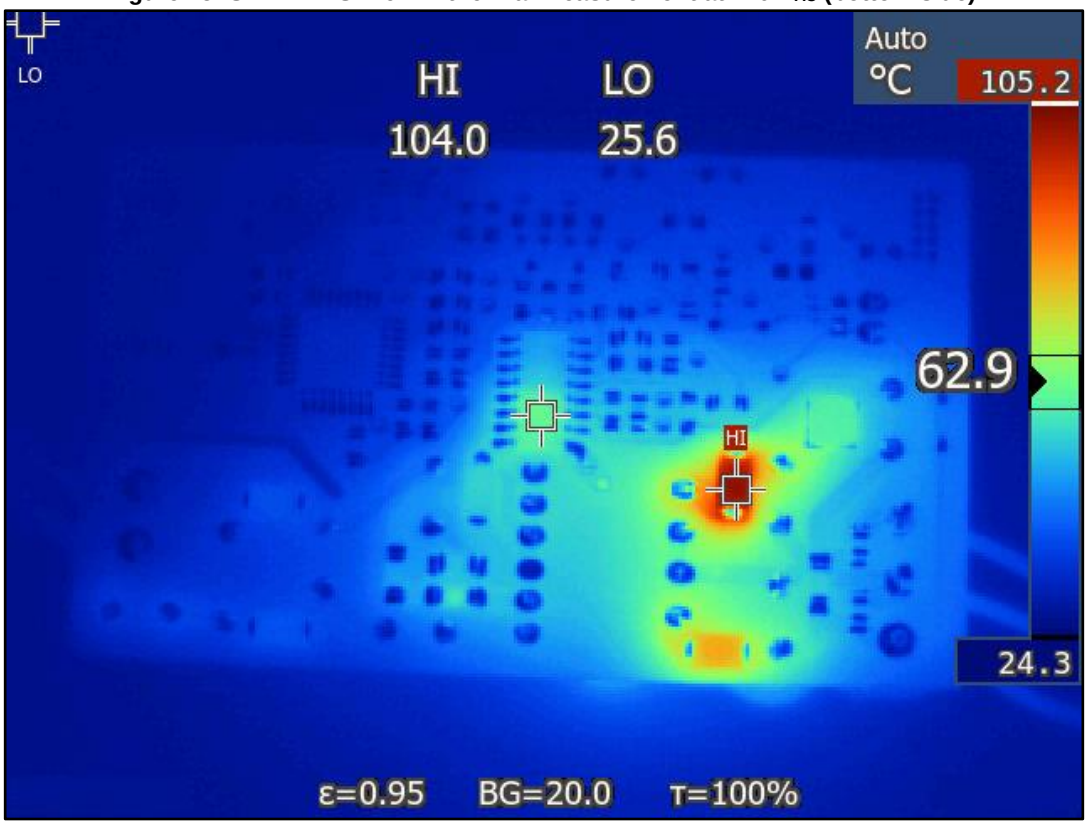


Figure 26: STEVAL-ISA192V1 thermal measurement at 230 V_{AC} (top side)

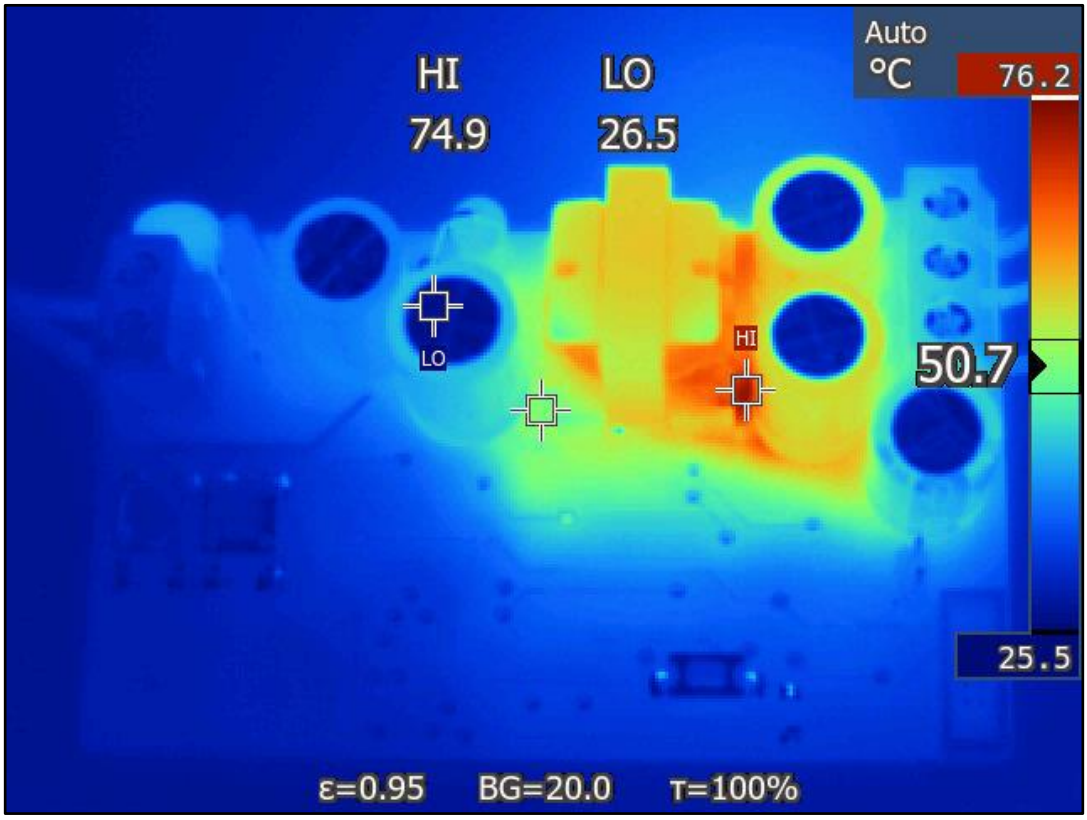
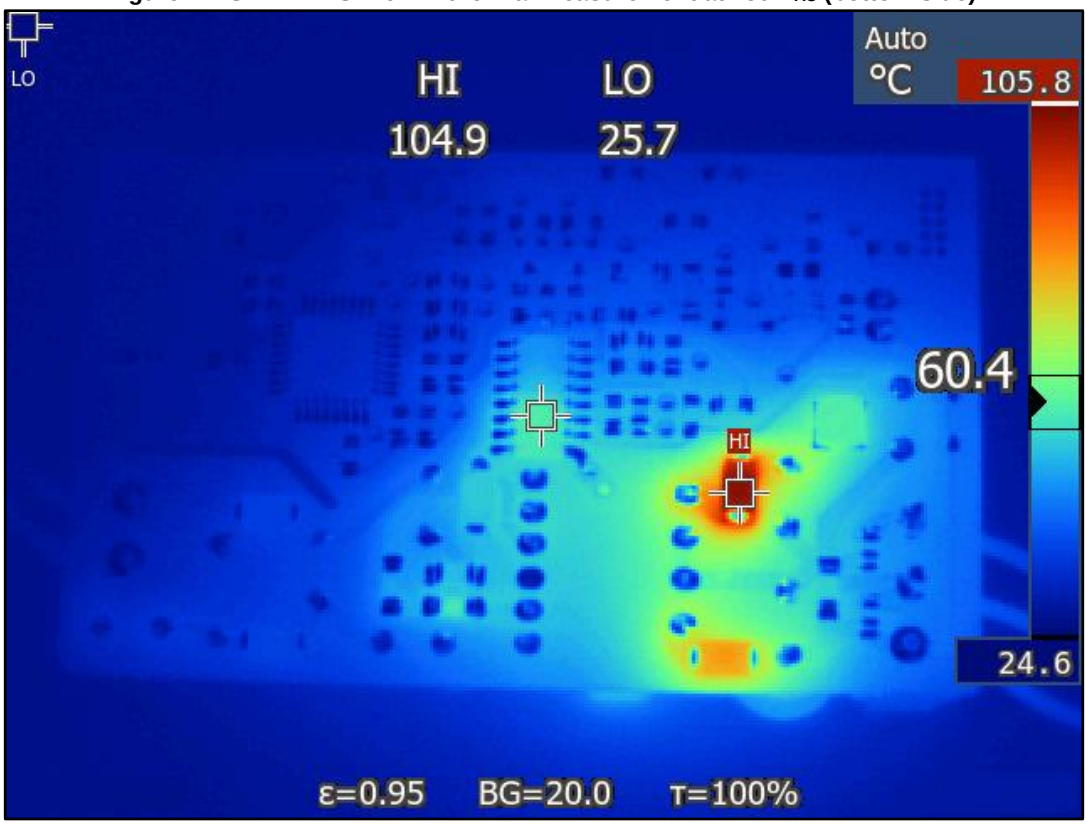


Figure 27: STEVAL-ISA192V1 thermal measurement at 230 V_{AC} (bottom side)



11 EMI measurements

A pre-compliant test to EN55022 (Class B) European normative has been performed using an EMC analyzer and a LISN. The results are shown in the following figures.

Figure 28: Average measurements at 115 V_{AC}, full load, T_{AMB} = 25°C

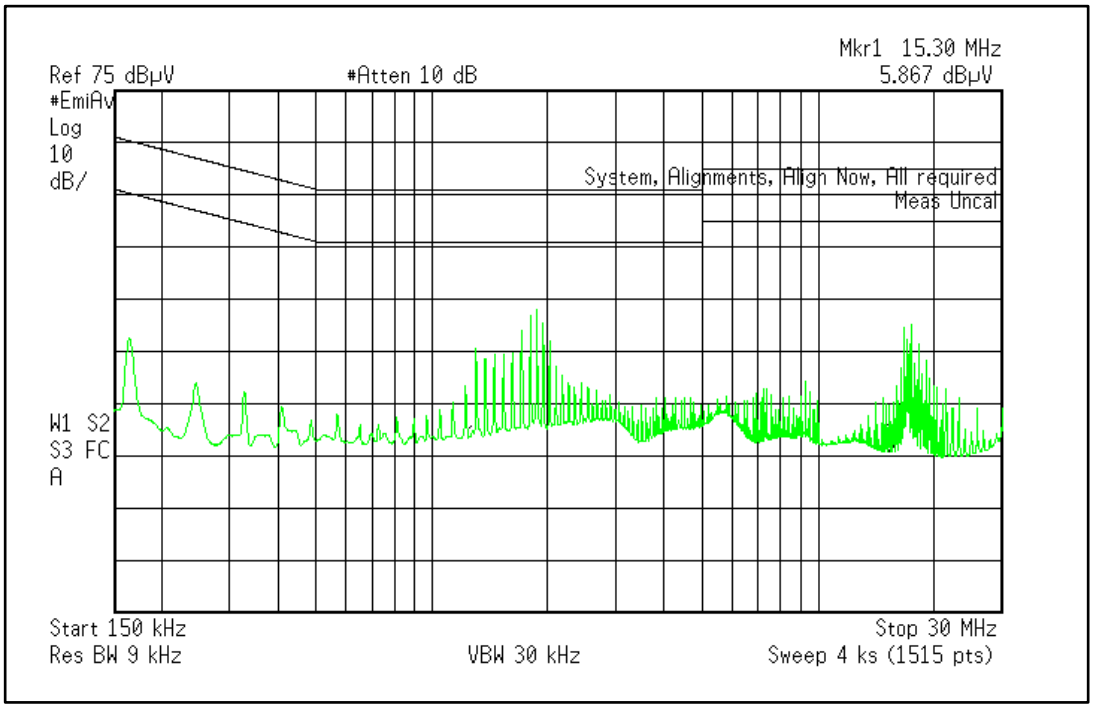
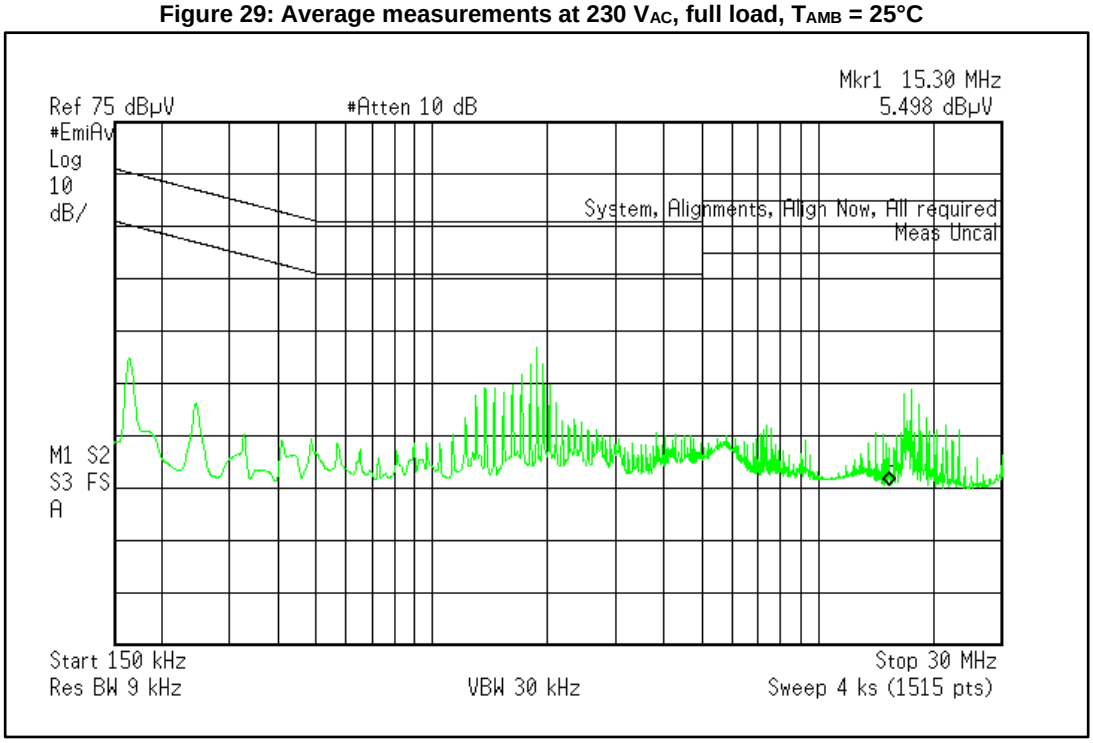


Figure 29: Average measurements at 230 V_{AC}, full load, T_{AMB} = 25°C



12 Immunity tests

The board was submitted to immunity tests according to IEC61000 and their results are classified according to the standard criteria:

- A: normal performance;
- B: temporary degradation or loss of function or performance, with automatic return to normal operation;
- C: temporary degradation or loss of function, with external intervention to re-cover normal operation
- D: degradation or loss of function, necessary substitution of damaged components to recover normal operation

12.1 Surge immunity test (IEC 61000-4-5)

The test conditions are:

- repetition rate: 1 minute (5 positive and 5 negative surges)
- applied to input lines vs. EARTH – common mode
- applied to both input lines (L vs. N) - differential mode
- reference plane connected to Protected Earth according to the normative.

In order to pass the test, the STEVAL-ISA192V1 schematic diagram has been modified with the additions highlighted in the figure below, consisting of a two 2.2 nF Y1 capacitor in series. The common point of the capacitors is the Protected Earth, which during the tests has to be connected to the reference plane, according to the normative.

The input voltage has been set to 230 V_{AC} and the output at 10% of full load, proper operation has been checked through a current probe connected to the output.

Figure 30: STEVAL-ISA192V1 surge improved circuit schematic

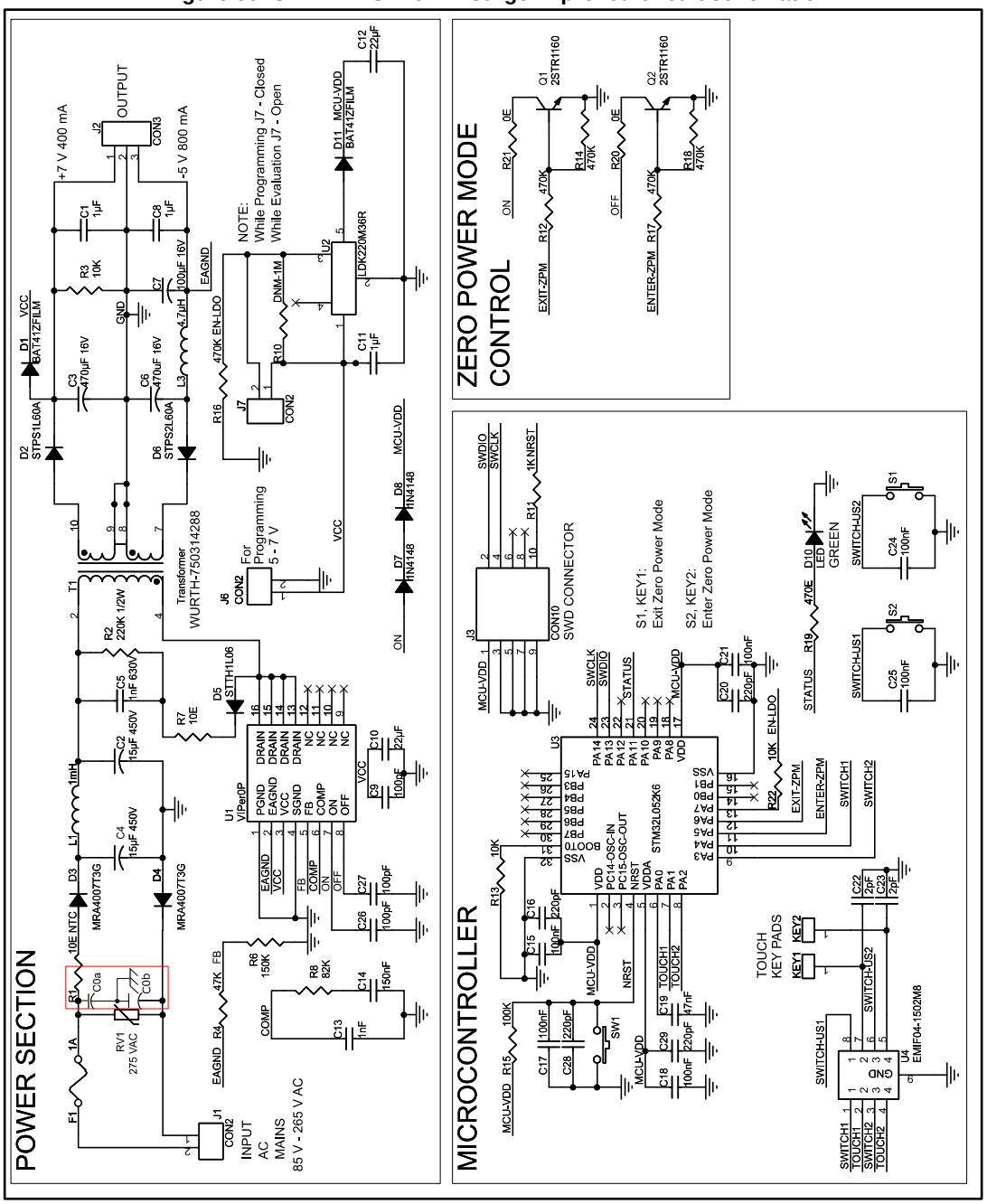


Table 8: Common mode surge test results

Noise injection	Surge level	Polarity	Result	Criterion
L vs. PE	2 kV	Positive	PASS	A
N vs. PE	2 kV	Positive	PASS	A
L vs. PE	2 kV	Negative	PASS	A
N vs. PE	2 kV	Negative	PASS	A

Table 9: Differential mode surge test results

Noise injection	Surge level	Polarity	Result	Criterion
L vs. N	2 kV	Positive	PASS	A
L vs. N	2 kV	Negative	PASS	A

Performed tests show that the board withstands the lightning disturbances applied to input line in common mode and differential mode for each severity level.

12.2 ESD immunity test (IEC 61000-4-2)

The test conditions are:

- Contact discharge and air discharge methods
- Discharge circuit150 pF/330 Ω
- Polarity: positive/negative

The setting of *Figure 30: "STEVAL-ISA192V1 surge improved circuit schematic"* allowed passing also the ESD test.

The key point is the filtering of the sensitive pins ON, OFF and EAGND through 220 pF ceramic capacitors to SGND. The purpose of the input filter (varistor and the 2.2 nF Y1 capacitors, C0a and C0b) is only to provide the Protected Earth (common point of the capacitors) for the ESD signal correct coupling according to the IEC 61000-4-2 normative.

The input voltage has been set to 230 V_{AC} and the output at 10% of full load, proper operation has been checked through a current probe connected to the output.

The test results are listed in the following tables.

Table 10: ESD contact discharge test results

Noise injection	ESD level	Polarity	Result	Criterion
L vs. PE	10 kV	Positive	PASS	A
L vs. PE	10 kV	Negative	PASS	A
N vs. PE	10 kV	Positive	PASS	A
N vs. PE	10 kV	Negative	PASS	A

Table 11: ESD contact discharge test results with PE connected on secondary GND

Noise injection	ESD level	Polarity	Result	Criterion
L vs. GND	8 kV	Positive	PASS	A
L vs. GND	8 kV	Negative	PASS	A
N vs. GND	8 kV	Positive	PASS	A
N vs. GND	8 kV	Negative	PASS	A

Table 12: ESD air discharge test results

Noise injection	ESD level	Polarity	Result	Criterion
Horizontal coupling plane	20 kV	Positive	PASS	A
Horizontal coupling plane	20 kV	Negative	PASS	A
Vertical coupling plane	20 kV	Positive	PASS	A
Vertical coupling plane	20 kV	Negative	PASS	A

12.3 Burst immunity test (IEC 61000-4-4)

The test was performed on a single test board. The input voltage was set to 230 V_{AC}, the output was loaded with 10% of the nominal load and the proper operation was verified by connecting a current probe to the output.

The test conditions are:

- polarity: positive/negative
- burst duration: 15 ms ±20 % at 5 kHz
- burst period: 300 ms ±20 %
- duration time: 1 minute
- applied to: AC lines through integrated capacitive coupling clamp.

The test can be passed with the original setting (); the key point is the filtering of the sensitive pins ON, OFF and EAGND through 220 pF ceramic capacitors to SGND. The input voltage has been set to 230 V_{AC} and the output at 10% of full load; proper operation has been checked through a current probe connected to the output.

The test results are listed in the following table.

Table 13: Burst test results

Noise injection	Burst level	Polarity	Result	Criterion
L	4 kV	Positive	PASS	A
N	4 kV	Positive	PASS	A
PE	4 kV	Positive	PASS	A
L/PE	4 kV	Positive	PASS	A
N/PE	4 kV	Positive	PASS	A
L/N	4 kV	Positive	PASS	B
L/N/PE	4 kV	Positive	PASS	A
L	4 kV	Negative	PASS	A
N	4 kV	Negative	PASS	A
PE	4 kV	Negative	PASS	A
L/PE	4 kV	Negative	PASS	A
N/PE	4 kV	Negative	PASS	A
L/N	4 kV	Negative	PASS	A
L/N/PE	4 kV	Negative	PASS	A

13 Board layout

Figure 31: STEVAL-ISA192V1 evaluation board top layer

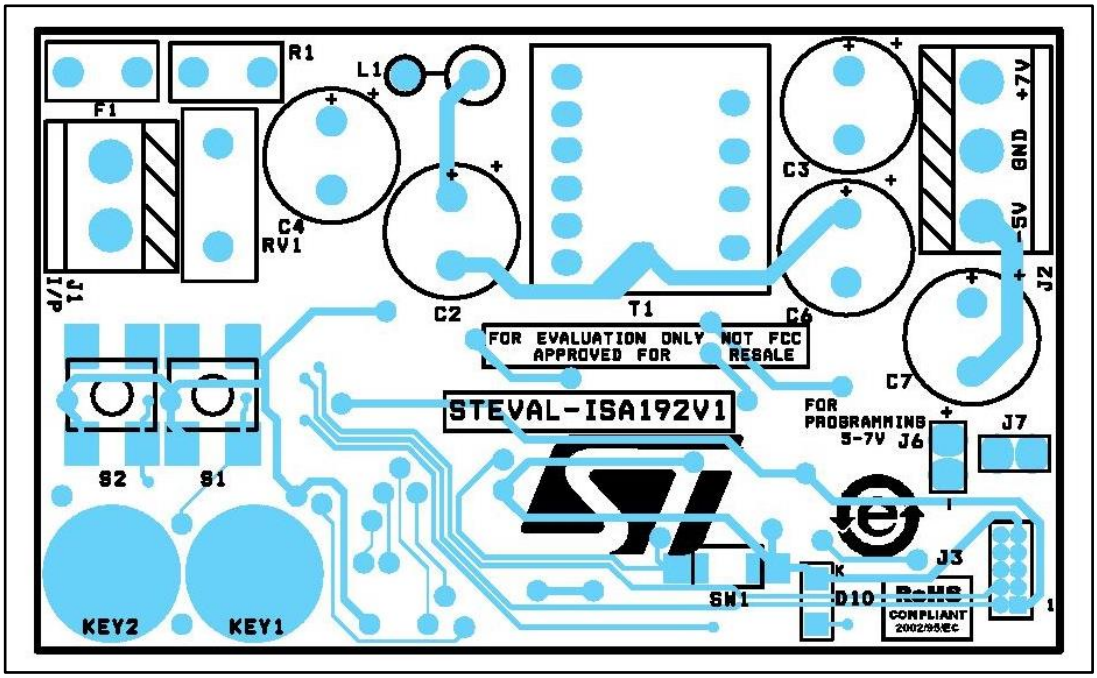
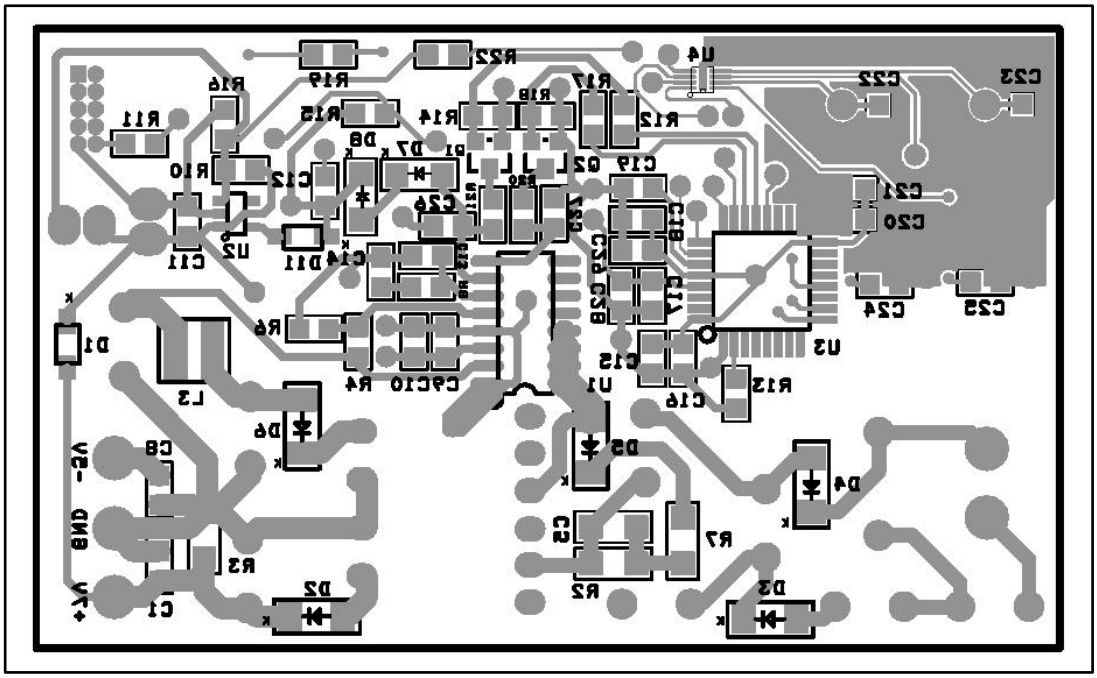


Figure 32: STEVAL-ISA192V1 evaluation board bottom layer



14 References

1. VIPer0P datasheet
2. Application note: AN4836 - STEVAL-ISA174V1: VIPer0P 7 W double output non-isolated flyback
3. STM32L052xx datasheet
4. IEC 61000-4-2
5. IEC 61000-4-4
6. IEC 61000-4-5

15 Revision history

Table 14: Document revision history

Date	Version	Changes
10-Apr-2017	1	Initial release

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