AN4830
Application note

15 W, 5 V - 12 V double output, isolated flyback converter based on Viper37LE/D

Introduction

The STEVAL-ISA184V1 and STEVAL-ISA191V1 are double output (5 V - 12 V) – 15 W power supplies in isolated flyback topology with the VIPer37L off-line high voltage converter by STMicroelectronics.

The two evaluation boards have the same electrical specifications but differently packaged converters: VIPer37LE (SDIP10 - STEVAL-ISA191V1) and VIPer37LD (SO16 - STEVAL-ISA184V1).

The devices feature an 800 V avalanche rugged power section, PWM control, cycle-by-cycle current limit with adjustable set point, on-board soft-start and safe auto-restart after a fault condition.

The available protections include thermal shutdown with hysteresis, two levels of overcurrent protection, overvoltage and overload protections.

The present flyback converter is suitable to be used as an external adapter or as an auxiliary power supply in consumer equipment.

Contents

1 Evaluation board images

Figure 1: STEVAL-ISA191V1 power supply board (top layer)

Figure 2: STEVAL-ISA191V1 power supply board (bottom layer)

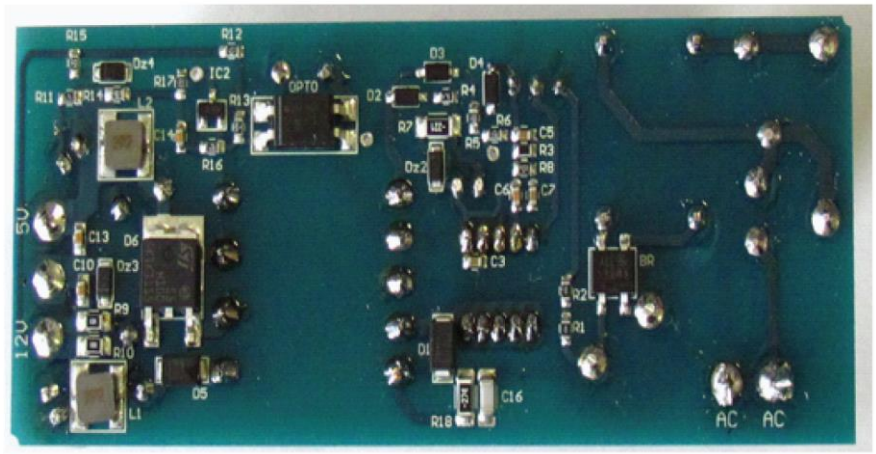


Figure 3: STEVAL-ISA184V1 power supply board (top layer)

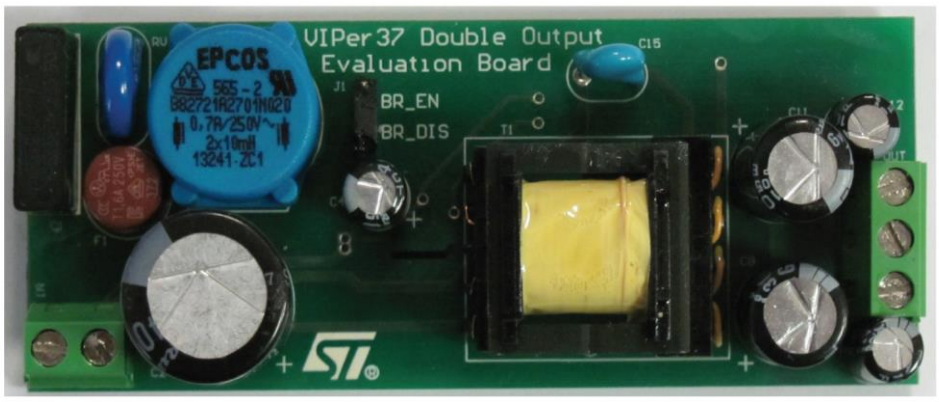


Figure 4: STEVAL-ISA184V1 power supply board (bottom layer)

2 Test board: design and evaluation

The electrical specifications of the evaluation board are listed below.

Table 1: Evaluation board electrical specification

Parameter	Min.	Typ.	Max.	Unit
AC Main Input voltage	85		265	V_{AC}
Mains frequency (f_L)	50		60	Hz
Output Voltage 1	4.75	5	5.25	V
Output Current 1			1.2	A
Output ripple voltage 1			50	mV
Output Voltage 2	10.2	12	13.8	V
Output Current 2			0.75	A
Output ripple voltage 2			50	mV
Rated output power		15		W
Input power in standby @ 230V_{AC}			40	mW
Active mode efficiency	75			%
Ambient operating temperature			60	°C

The power supply is set in isolated flyback topology. The input section includes a diode bridge (BR), an X-capacitor (C1) for differential EMC suppression and a CM choke for common mode EMC suppression. A clamp network (D1, R18, C16) is used for leakage inductance demagnetization.

The resistor connected between CONT pin and ground lowers the default current limitation of the device (according to the I_{DLIM} vs R_{LIM} graphic reported in the datasheet) to the value required for the desired power throughput to avoid overly stressing the power components. A small LC filter is added to the output to filter any high frequency ripple.

As both evaluation boards exhibit very similar cross-regulation, efficiency and light load performance, the following sections apply to both of them.

Figure 5: Schematic diagram

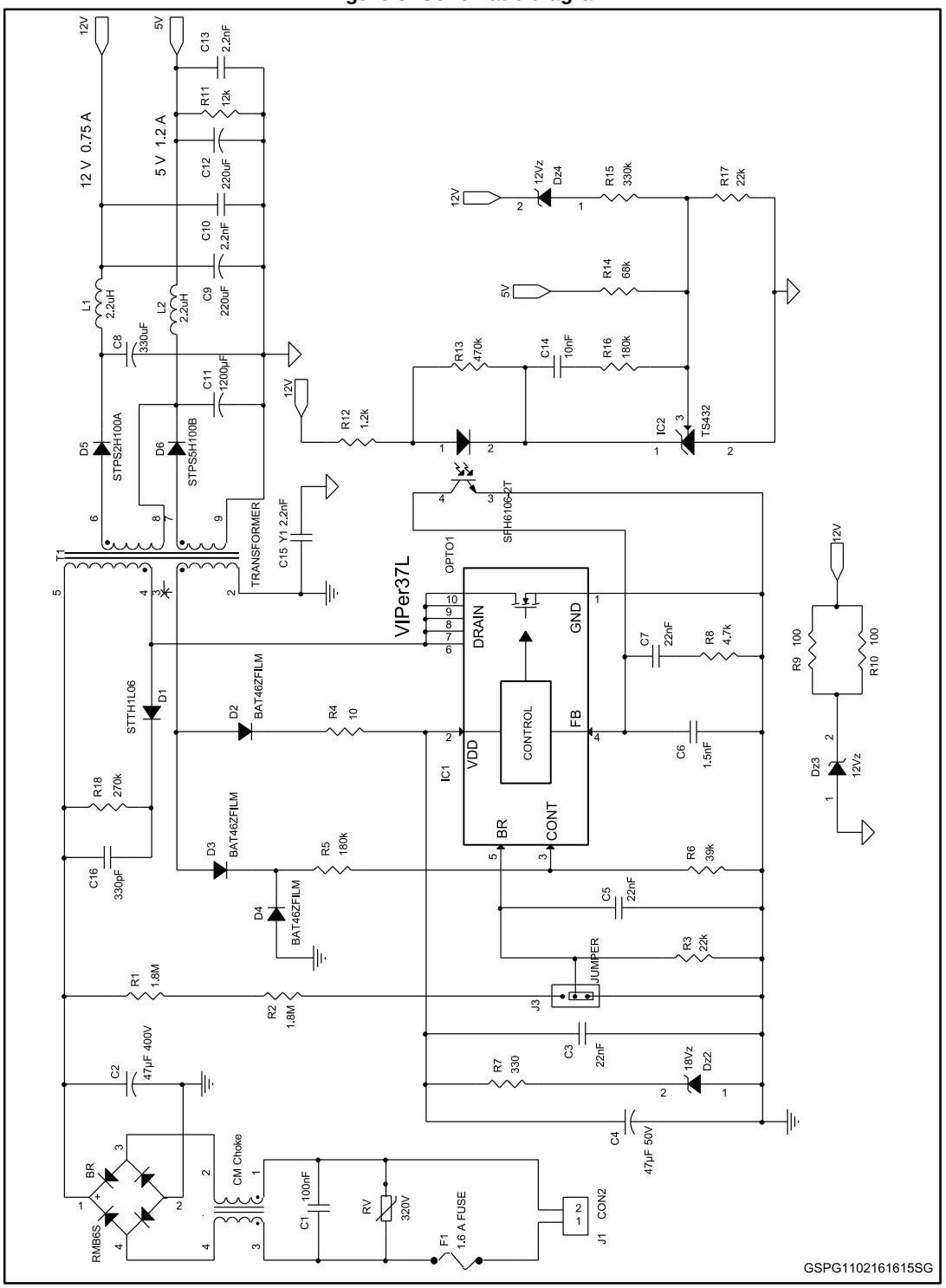


Table 2: Bill of materials (BOM)

Reference	Part	Description	Manufacturer
R1	CRCW06031M80FKEA	1.8MΩ±1% - 0.1W Resistor	Vishay
R2	CRCW06031M80FKEA	1.8MΩ±1% - 0.1W Resistor	Vishay
R3	ERJPA3F2202V	22kΩ±1% - 0.25W Resistor	Panasonic
R4	ERJ3GEYJ100V	10Ω±5% - 0.1W Resistor	Panasonic
R5	CRCW0603180KFKEA	180kΩ±1% - 0.1W Resistor	Vishay
R6	CRCW060339K0FKEA	39kΩ±1% - 0.1W Resistor	Vishay
R7	ERJT08J331V	330Ω±5% - 0.33W Resistor	Panasonic
R8	CRCW06034K70FKEA	4.7kΩ±1% - 0.1W Resistor	Vishay
R9	ERJP06J101V	100Ω±5% - 0.5W Resistor	Panasonic
R10	ERJP06J101V	100Ω±5% - 0.5W Resistor	Panasonic
R11	ERJ3GEYJ123V	12kΩ±5% - 0.1W Resistor	Panasonic
R12	ERJ3GEYJ122V	1.2kΩ±5% - 0.1W Resistor	Panasonic
R13	ERJ3GEYJ474V	470kΩ±5% - 0.1W Resistor	Panasonic
R14	CRCW060368K0FKEA	68kΩ±1% - 0.1W Resistor	Vishay
R15	CRCW0603330KFKEA	330kΩ±1% - 0.1W Resistor	Vishay
R16	CRGH0603J180K	180kΩ±5% - 0.2W Resistor	TE Connectivity
R17	CRCW060322K0FKEA	22kΩ±1% - 0.1W Resistor	Vishay
R18	ERJT08J274V	270kΩ±5% - 0.33W Resistor	Panasonic
C1	ECQUAAF104M	100nF - 275V Capacitor X2	Panasonic
C2	400BXC47MEFC16X25	47µF – Electrolytic capacitor 400V	Rubycon
C3, C5, C7	GRM188R71H223KA01D	22nF – Capacitor 50V	Murata
C4	50PK47MEFC6.3X11	47µF – Electrolytic capacitor 50V	Rubycon
C6	GRM188R71H152KA01D	1.5nF – Capacitor 50V	Murata
C8	25ZLG330MEFC10X12.5	330µF – Electrolytic capacitor 25V	Rubycon
C9	25YXJ220M6.3X11	220µF – Electrolytic capacitor 25V	Rubycon
C10	GRM188R71H222KA01D	2.2nF – Capacitor 50V	Murata
C11	16ZLK1200M10X20	1200µF – Electrolytic capacitor 16V	Rubycon
C12	25YXJ220M6.3X11	220µF – Electrolytic capacitor 25V	Rubycon
C13	GRM188R71H222KA01D	2.2nF – Capacitor 50V	Murata
C14	GRM188R71H103KA01D	10nF – Capacitor 50V	Murata
C15	DE2E3KY222MA2BM01	2.2nF Capacitor Y2	Murata
C16	GRM31A5C2J331JW01D	330pF – Capacitor 630V	Murata
D1	STTH1L06A	Ultrafast diode 1A-600V	STMicroelectronics
D2, D3, D4	BAT46ZFILM	Signal schottky 0.15A-100V	STMicroelectronics
D5	STPS2H100A	Power Schottky 100V – 2A	STMicroelectronics

Reference	Part	Description	Manufacturer
D6	STPS5H100B	Power Schottky 100V – 5A	STMicroelectronics
Dz2	DZ2W18000L	Zener Diode 18V 1W	Panasonic
Dz3, Dz4	DZ2W12000L	Zener Diode 12V 1W	Panasonic
L1, L2	SRP4020-2R2M	2.2µH	Bourns
CM	B82721A2701N20	10mH CM Choke	EPCOS
BR	RMB6S	0.5A - 600V Bridge	Taiwan Semiconductor
IC1	VIPer37L (1)	Offline primary controller	STMicroelectronics
IC2	TS432ILT	Reference	STMicroelectronics
OPTO	SFH6106-2T	Optocoupler	Vishay
T1	1715.0081	Flyback transformer	Magnetica
F1	3721160000	Fuse	Wickmann
RV	B72210S0321K101	Varistor	EPCOS

Notes:

(1)VIPer37LE for STEVAL-ISA191V1 and VIPer37LD for STEVAL-ISA184V1

The transformer characteristics are listed below:

Table 3: Transformer characteristics

Parameter	Value
Manufacturer	MAGNETICA
Part Number	1715.0081
Primary inductance (4 – 5)	890 µH ± 10%
Leakage inductance	3.1% of Primary inductance
Turn ratio (4 – 5) / (1 – 2)	5.16 ± 5%
Turn ratio (4 – 5) / (6 – 8)	9.3 ± 5%
Turn ratio (4 – 5) / (7 – 9)	13.28 ± 5%
Primary to secondary insulation	4 kV

Figure 6: Dimensional drawing and pin placement diagram - top view

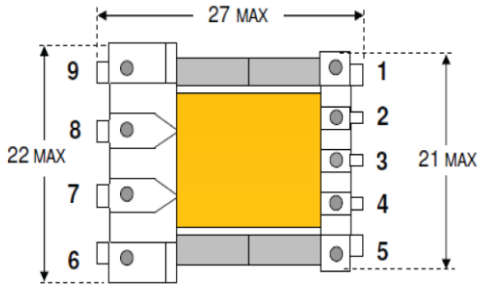


Figure 7: Dimensional drawing and pin placement diagram - side view

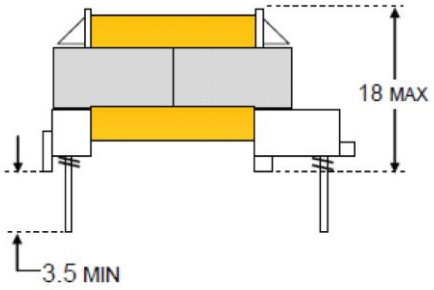


Figure 8: Dimensional drawing and pin placement diagram - bottom view

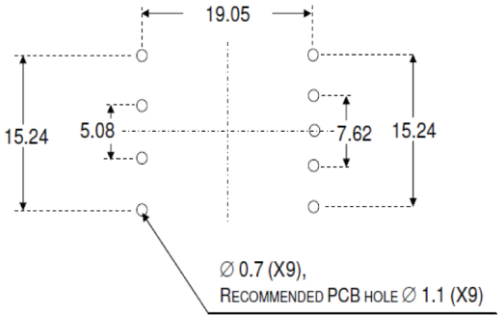
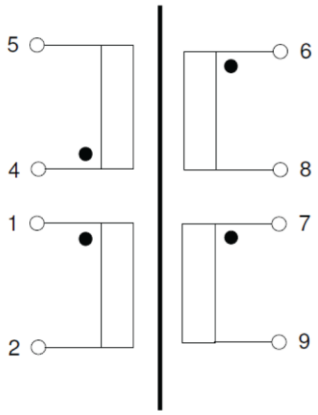


Figure 9: Dimensional drawing and pin placement diagram - electrical diagram



2.1 Output voltage characteristic

The output voltages of the boards are measured under different line and load conditions.

Figure 10: "VOUT1 line and load regulation with IOUT2 under no load" shows output voltage 1 when output voltage 2 is under a no load condition, while *Figure 11: "VOUT1 line and load regulation with IOUT2 = 750 mA"* is derived for full load conditions of the second voltage output (750 mA). The same procedure is used to obtain the diagrams of output voltage 2 when output voltage 1 is under the no load (*Figure 12: "VOUT2 line and load regulation with IOUT1 under no load"*) and full load condition (*Figure 13: "VOUT2 line and load regulation with IOUT1 = 1.2 A"*).

In a two-output flyback converter, when just one output is regulated, the unregulated output doesn't strictly adhere to the turn ratio. The unregulated output voltage value depends not only on the turn ratio, but also somewhat on the output current ratio (output current at the regulated output divided by output current of the unregulated output).

In this case, both outputs are regulated, but because the resistance connected to output voltage 2 is higher than that connected to output voltage 1, we can assume to have a single regulated output. In fact, *Figure 12: "VOUT2 line and load regulation with IOUT1*

under no load" and *Figure 13: "VOUT2 line and load regulation with IOUT1 = 1.2 A"* show how the less regulated output voltage value (output voltage 2) varies more than the other output voltage value (*Figure 10: "VOUT1 line and load regulation with IOUT2 under no load"* and *Figure 11: "VOUT1 line and load regulation with IOUT2 = 750 mA"*) for different load conditions.

However, by a variation of the line condition, both voltage output values are practically unaffected.

Figure 10: VOUT1 line and load regulation with IOUT2 under no load

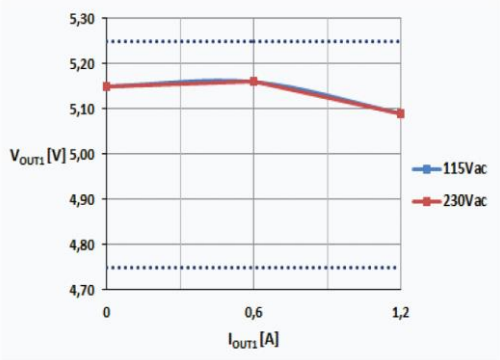


Figure 11: VOUT1 line and load regulation with IOUT2 = 750 mA

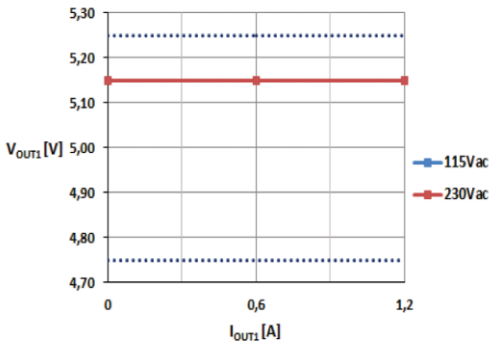


Figure 12: VOUT2 line and load regulation with IOUT1 under no load

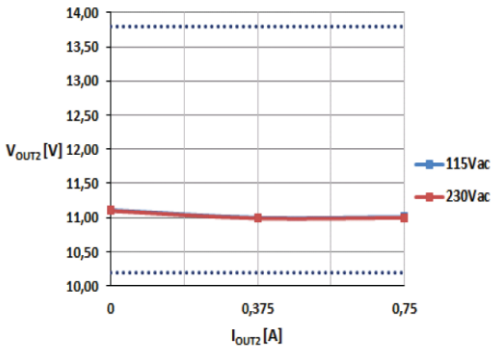
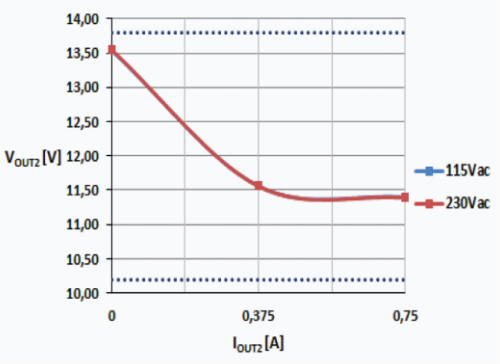


Figure 13: VOUT2 line and load regulation with IOUT1 = 1.2 A



2.2 Efficiency and light load measurements

The efficiency of the converters was measured under different load and line voltage conditions.

The efficiency measurements were performed at 25%, 50%, 75% and 100% maximum rate for both outputs, at 115 V_{AC} and 230 V_{AC}.

The results for both outputs are shown below.

Table 4: Average efficiency at 115 VAC

%Load	I_{OUT1} (A)	I_{OUT2} (A)	V_{OUT1} (V)	V_{OUT2} (V)	P_{IN} (W)	P_{OUT} (W)	Efficiency (%)
25%	0.3	0.1875	5.15	11.27	4.67	3.66	78.37
50%	0.6	0.375	5.15	11.32	9.34	7.34	78.59
75%	0.9	0.5625	5.15	11.36	14.09	11.03	78.28
100%	1.2	0.75	5.15	11.40	18.96	14.73	77.69
Average Efficiency							78.23

Table 5: Average efficiency at 130 VAC

%Load	I_{OUT1} (A)	I_{OUT2} (A)	V_{OUT1} (V)	V_{OUT2} (V)	P_{IN} (W)	P_{OUT} (W)	Efficiency (%)
25%	0.3	0.1875	5.15	11.27	4.80	3.66	76.25
50%	0.6	0.375	5.15	11.32	9.41	7.34	78.00
75%	0.9	0.5625	5.15	11.36	14.06	11.03	78.45
100%	1.2	0.75	5.15	11.40	18.78	14.73	78.43
Average Efficiency							77.78

Figure 14: Efficiency vs. output current load

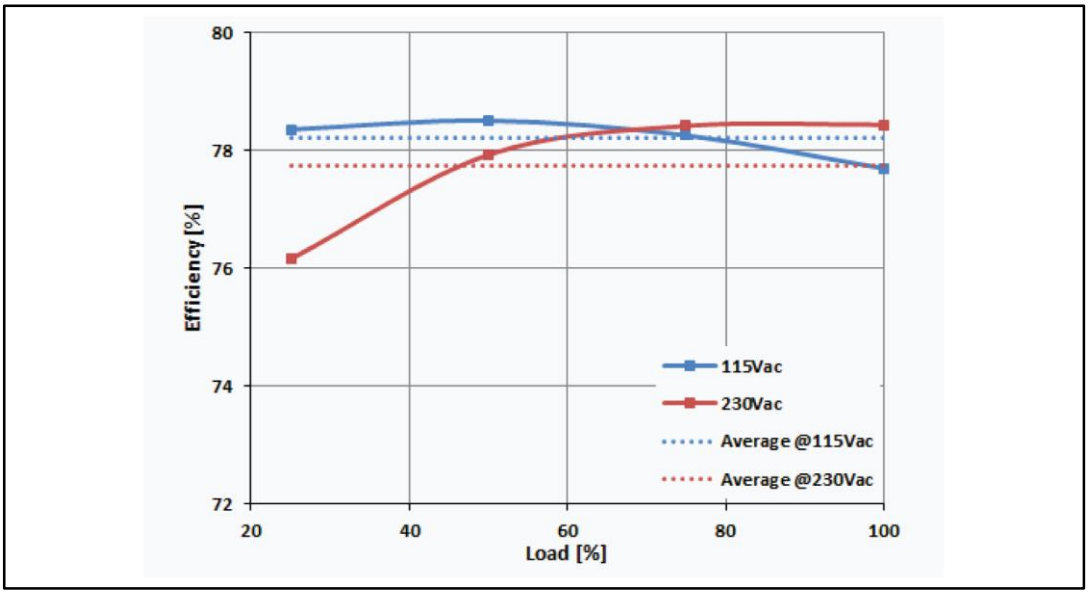
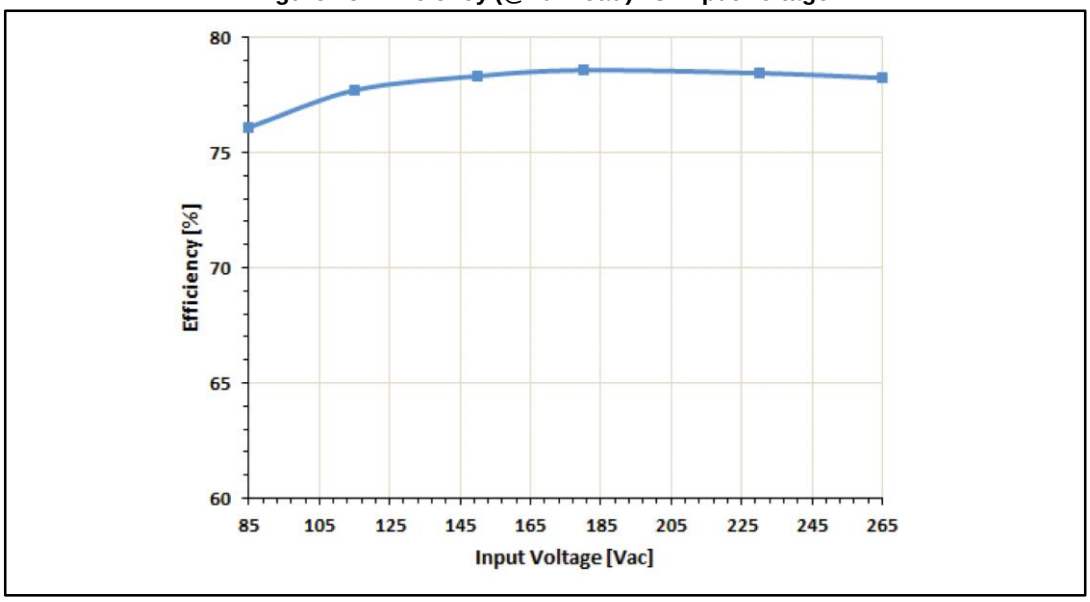


Figure 15: Efficiency (@ full load) vs. input voltage

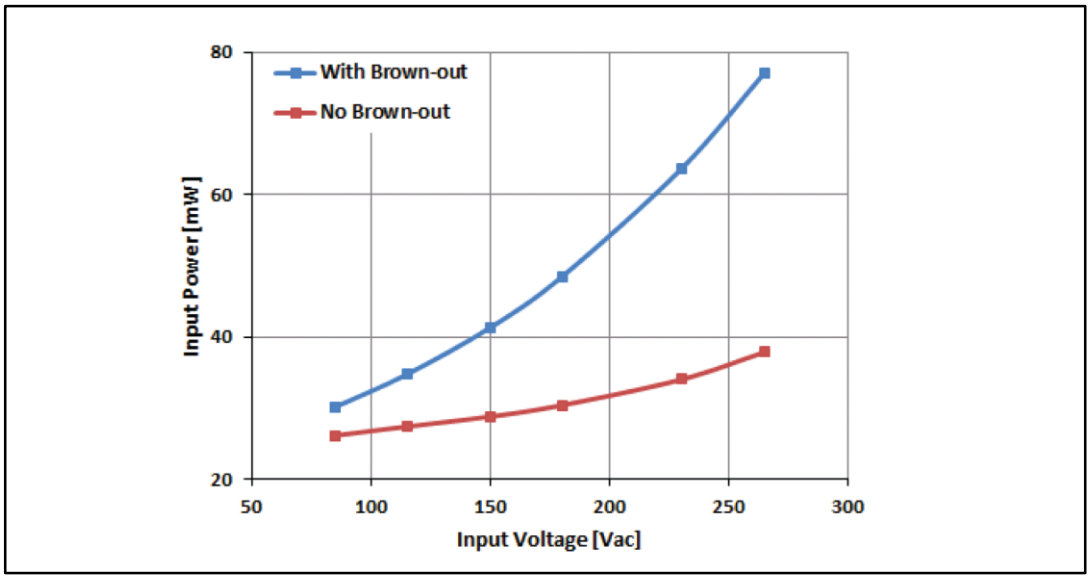


2.3 No load consumptions

The input power of the converters was measured under no load conditions, with brownout protection (see *Section 5.3: "Brownout protection"*) disabled and enabled across the entire input voltage range.

The converter under no load condition always operates in burst mode so that the average switching frequency is reduced. The presence of the brownout resistor divider (R1, R2 and R3 - see *Figure 5: "Schematic diagram"*), to sense the flyback input voltage when brownout protection is enabled, does not affect the average switching frequency but, of course, does affect the input power due to the dissipation in the resistor divider itself.

Figure 16: No load consumptions vs. input voltage



2.4 Light load consumption

The user very often requires input power consumption when the output is loaded with a few tens of mW of output power.

In particular, in the new EuP Lot 6 requirements, the input power must be lower than 0.5 W when the output is loaded with 0.25 W.

Such measurements were performed at different loads with brownout protection enabled and disabled with the results reported below.

Figure 17: Light load consumption at different output power without brownout

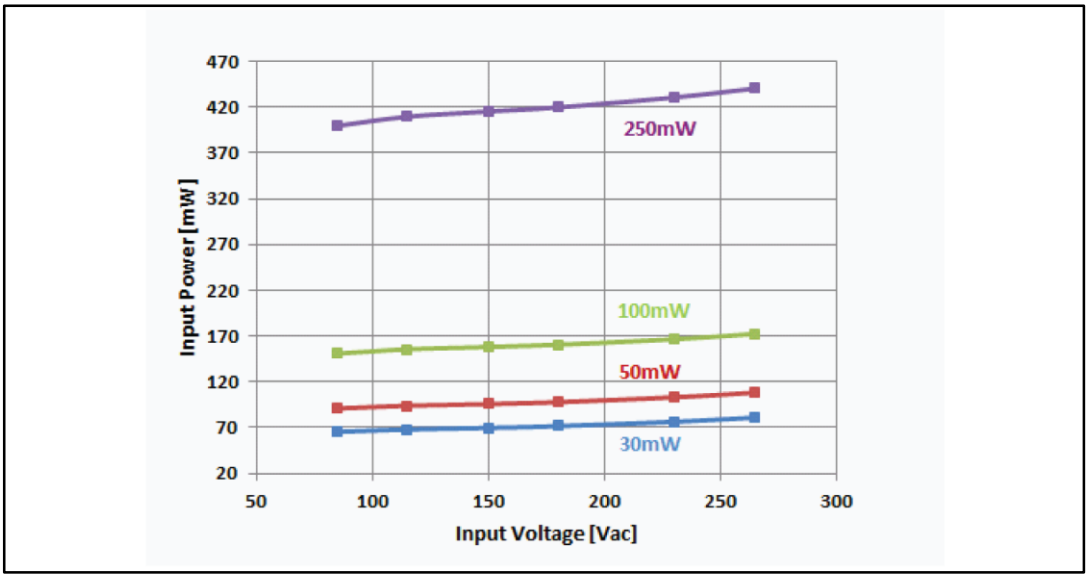
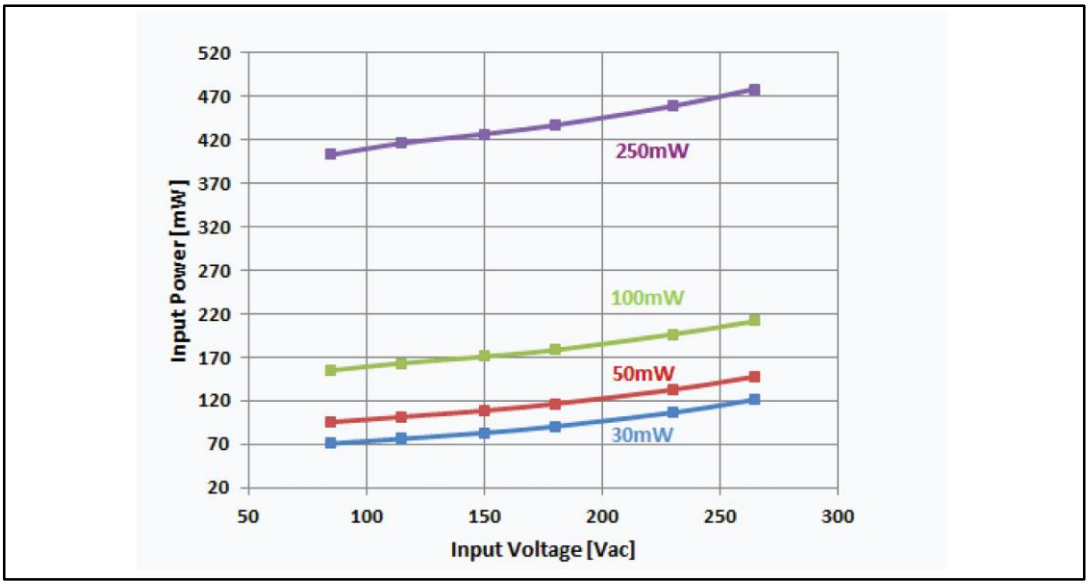


Figure 18: Light load consumptions at different output power with brownout



3 Typical board waveforms

The drain voltage and current waveforms under full load conditions are given for minimum and maximum input voltage in *Figure 19: "Drain current and voltage at full load at 85VAC"* and *Figure 20: "Drain current and voltage at full load at 265VAC"*, and for the two nominal input voltages in *Figure 21: "Drain current and voltage at full load at 115VAC"* and *Figure 22: "Drain current and voltage at full load at 230VAC"* respectively.

Figure 19: Drain current and voltage at full load at 85VAC

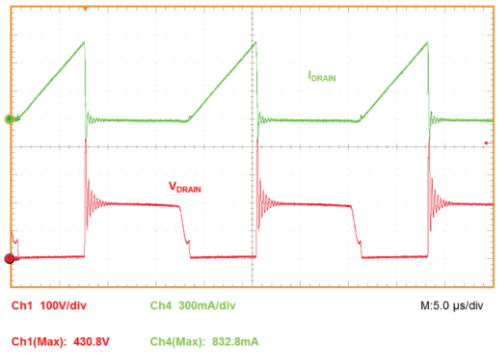


Figure 20: Drain current and voltage at full load at 265VAC

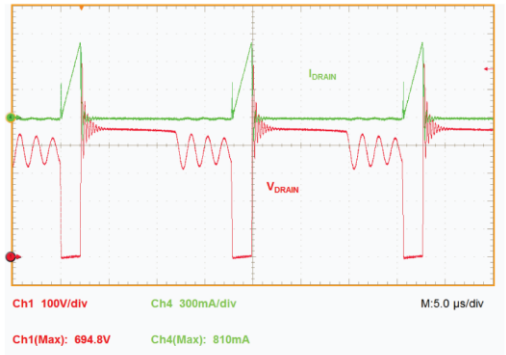


Figure 21: Drain current and voltage at full load at 115VAC

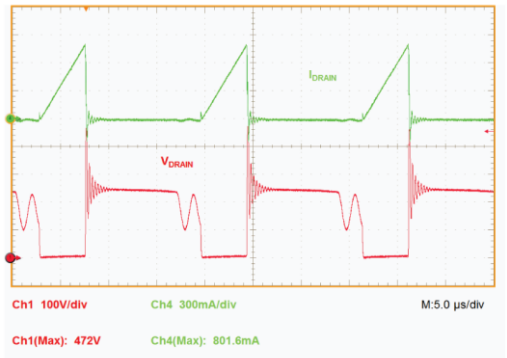
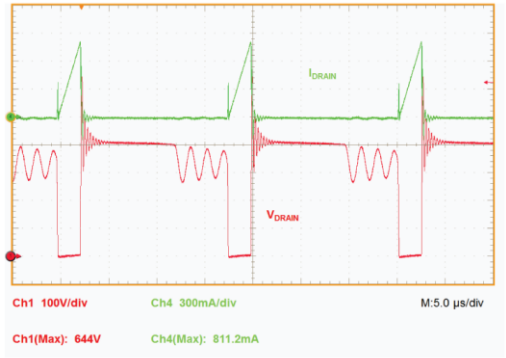


Figure 22: Drain current and voltage at full load at 230VAC



The output ripple at the switching frequency was also measured. The board is provided with LC filters on both outputs, to9 further reduce the ripple without reducing the overall ESR of the output capacitor.

The voltage ripple across the output connector (V_{OUT}) and before the LC filter (V_{OUT_PRE}) was measured for both outputs to verify the effectiveness of the LC filters. The following diagrams show voltage ripple on V_{OUT1} when the system works at full load condition: *Figure 23: "VOUT1 ripple at full load at 115VAC"* when the converter input voltage is $115V_{AC}$ and *Figure 24: "VOUT1 ripple at full load at 230VAC"* when the converter input voltage is $230V_{AC}$.

Figure 25: "VOUT1 ripple during burst mode at 115VAC" and *Figure 26: "VOUT1 ripple during burst mode at 230VAC"* show voltage ripple on V_{OUT1} when the device operates in burst mode, the measurements were performed under the same previous input voltage condition ($115V_{AC}$ and $230V_{AC}$).

The diagrams relative to V_{OUT2} ripple have been achieved under the same load and input voltage conditions seen previously (from *Figure 27: "VOUT2 ripple at full load at 115VAC"* to *Figure 30: "VOUT2 ripple during burst mode at 230VAC"*).

Figure 23: VOUT1 ripple at full load at 115VAC

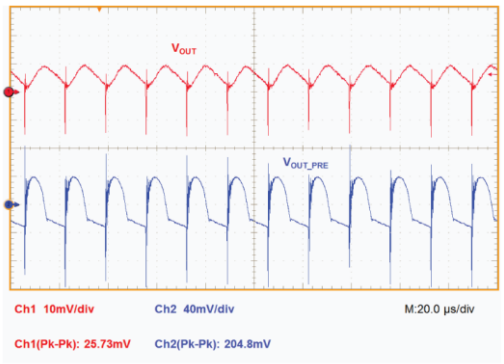


Figure 24: VOUT1 ripple at full load at 230VAC

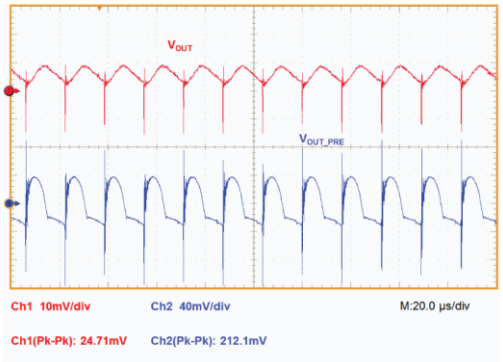


Figure 25: VOUT1 ripple during burst mode at 115VAC

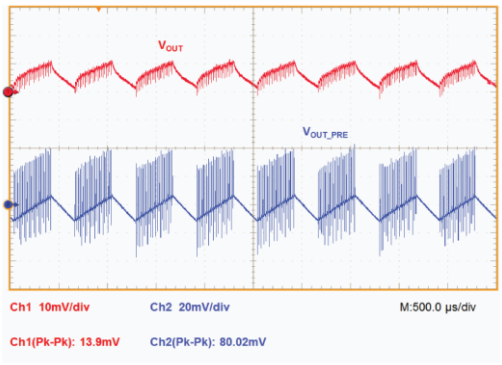


Figure 26: VOUT1 ripple during burst mode at 230VAC

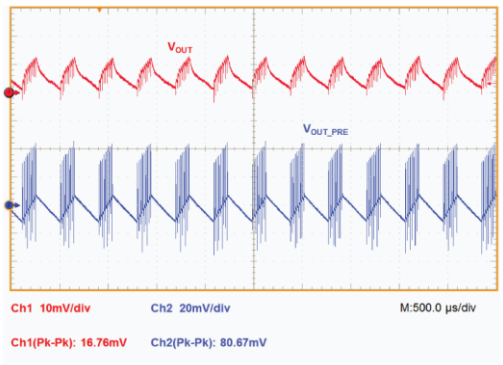


Figure 27: VOUT2 ripple at full load at 115VAC

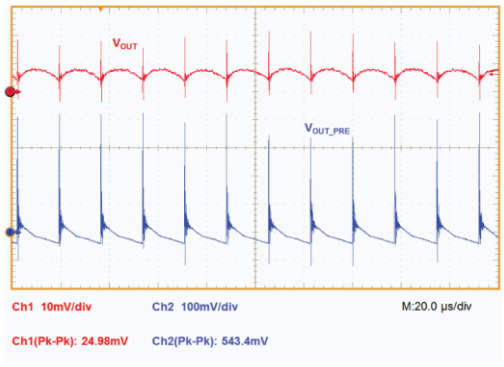


Figure 28: VOUT2 ripple at full load at 230VAC

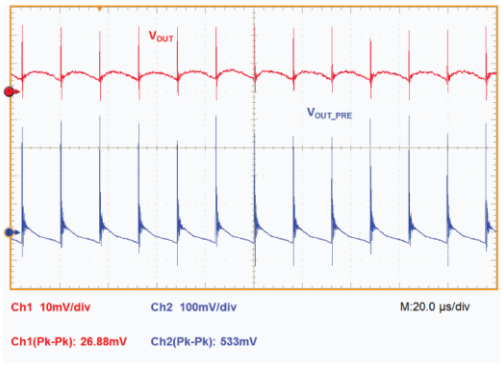


Figure 29: VOUT2 ripple during burst mode at 115VAC

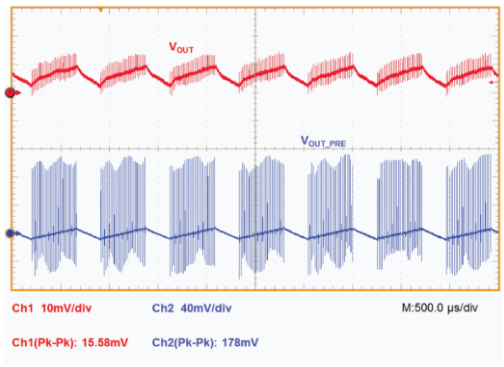
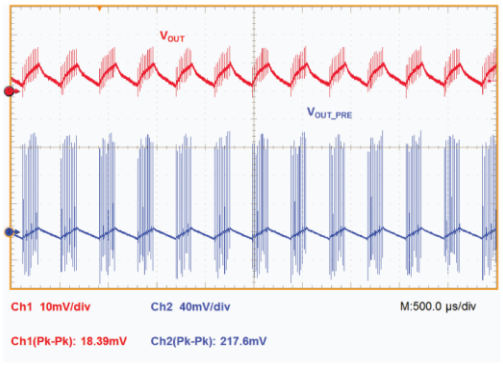


Figure 30: VOUT2 ripple during burst mode at 230VAC



3.1 Dynamic step load regulation

In any power supply, it is important to measure the output voltage when the converter is subject to dynamic load variations, to be certain that stability is good and no overvoltage or undervoltage occurs.

The test was performed for both nominal input voltages by varying the output 1 current load from 0 to 100% of nominal value and keeping the other output current load once at 50% and once at 100% of its nominal value.

The output 2 current load from 0 to 100% of nominal value was varied in the same way, keeping output 1 load once at 50% and once at 100% of its nominal current load value.

In every tested conditions, no abnormal oscillations were noticed on the outputs and over/under shoot were well within acceptable values.

Figure 31: Dynamic step load (0 to 100% output load 1 - 50% output load 2) at 115VAC

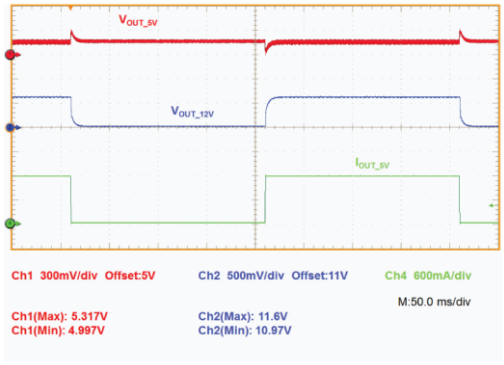


Figure 32: Dynamic step load (0 to 100% output load 1 - 50% output load 2) at 230VAC

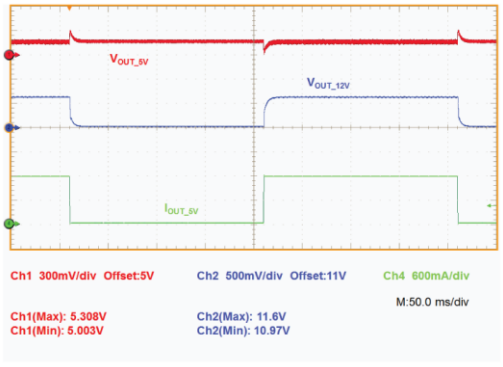


Figure 33: Dynamic step load (0 to 100% output load 1 - 100% output load 2) at 115VAC

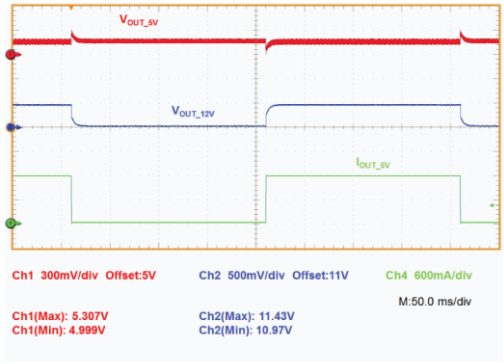


Figure 34: Dynamic step load (0 to 100% output load 1 - 100% output load 2) at 230VAC

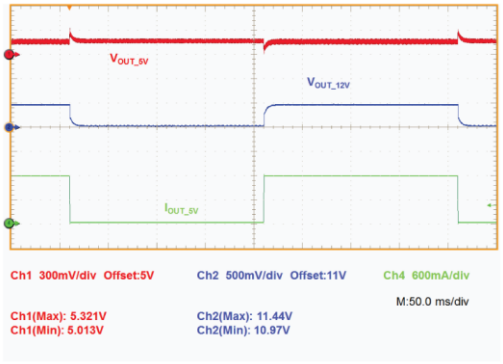


Figure 35: Dynamic step load (0 to 100% output load 2 - 50% output load 1) at 115VAC

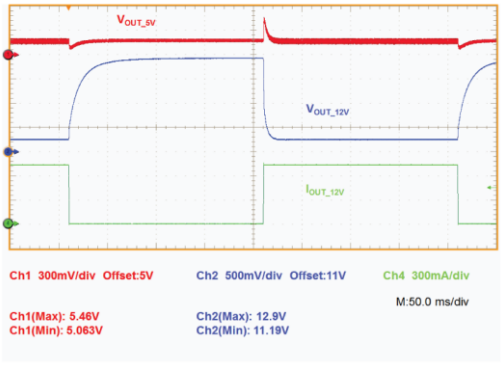


Figure 36: Dynamic step load (0 to 100% output load 2 - 50% output load 1) at 230VAC

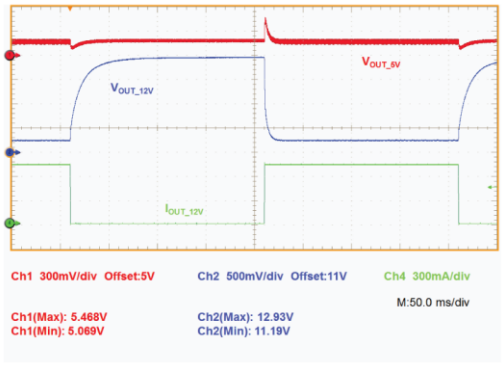


Figure 37: Dynamic step load (0 to 100% output load 2 - 100% output load 1) at 115VAC

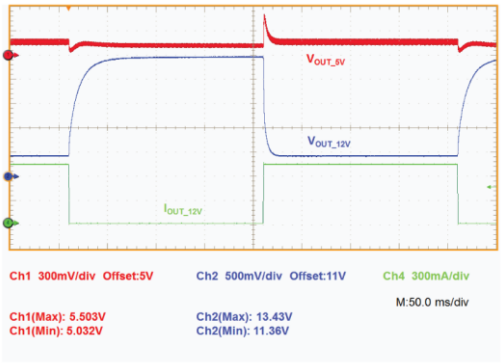
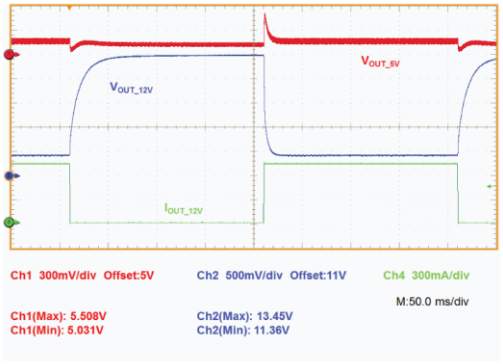


Figure 38: Dynamic step load (0 to 100% output load 2 - 100% output load 1) at 230VAC



4 Soft-start

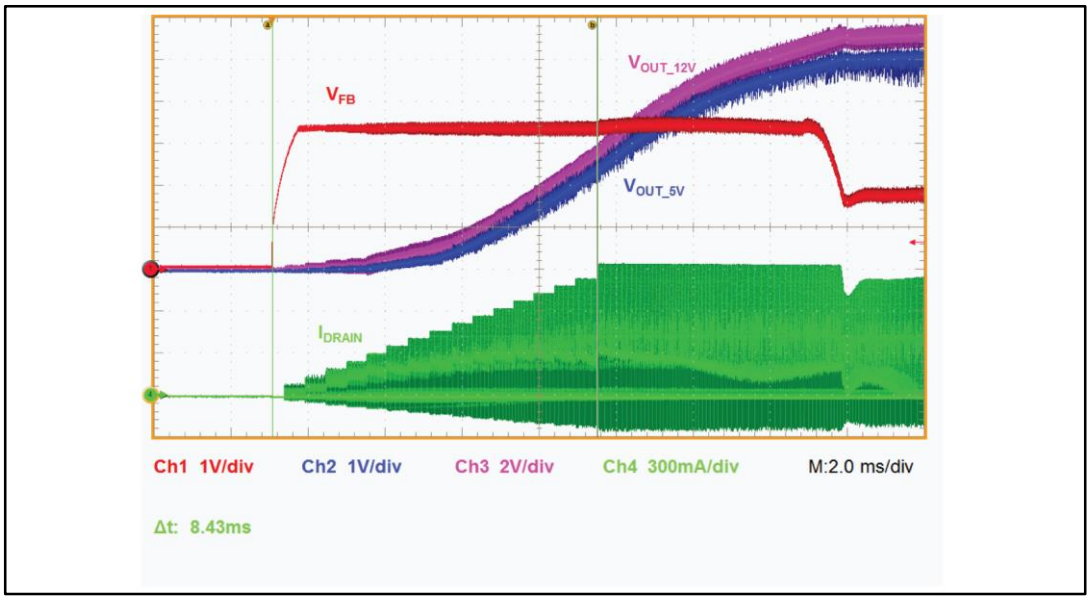
When the converter starts, the output capacitor is discharged and needs some time to reach the steady-state condition. During this time, the power demand from the control loop is at its maximum, while the reflected voltage is low. These two conditions may lead to a deep continuous operating mode of the converter.

Also, when the MOSFET is switched on, it cannot be switched off immediately as the minimum on-time (T_{ON_MIN}) has to elapse. Because of the deep continuous working mode of the converter, during this T_{ON_MIN}, an excess of drain current can overstress the converter components as well as the device itself, the output diode and the transformer. Transformer saturation is also possible under these conditions.

To avoid all od these these undesirable effects, the VIPer37L implements an internal soft-start feature. As the device starts functioning, the drain current is allowed to increase from zero to the maximum value gradually, regardless of the control loop request.

The drain current limit is increased in steps, and the values range from 0 to the fixed drain current limitation value (which can be changed through an external resistor) is divided into 16 steps. Each step length is 64 switching cycles. The total length of the soft-start phase is about 8.5 ms. *Figure 39: "Soft start feature"* shows the soft-start phase of the presented converter when it is operating at minimum line voltage and maximum load.

Figure 39: Soft start feature



5 Protection features

In order to increase end-product safety and reliability, VIPer37Lfeatures overload protection, overvoltage protection, shorted secondary rectifier detection and transformer saturation protection.

These protections are tested in the following sections.

5.1 Overload and short circuit protection

When the load power demand increases, the feedback loop reacts, increasing the voltage on the pin. In this way, the PWM current set point increases and the power delivered to the output rises. This process ends when the delivered power equals the load power request.

In case of overload or output short circuit (see *Figure 40: "Overload event, OLP triggering"*), the voltage on the FB pin reaches the V_{FBlin} value (3.5 V typical) and the drain current is limited to I_{Dlim} (or the one set by the user through the R_{LIM} resistor) by the OCP comparator. Under these conditions, an internal current generator is activated to charge capacitor C7; when the voltage on the FB pin reaches the V_{FBolp} threshold (4.8 V typical), the converter is turned off and is not allowed to switch again until the V_{DD} voltage falls below the $V_{DD\_RESTART}$ (4.5 V typical) and then rises to V_{DDon} (14 V typical).

The overload condition can be achieved shorting the output connector. After the V_{DD} voltage reaches the V_{DDon} value, if the short-circuit is not removed, the system enters auto-restart mode (see *Figure 41: "Overload event, continuous overload"*): in this case, the MOSFET switches for a short period of time, where the converter tries to deliver as much power to the output as it can, and a longer period where the device is not switching and no power is processed.

As the duty cycle of power delivery is very low (around 1.39%), the average power throughput is also very low, resulting in a very safe operation.

Figure 40: Overload event, OLP triggering

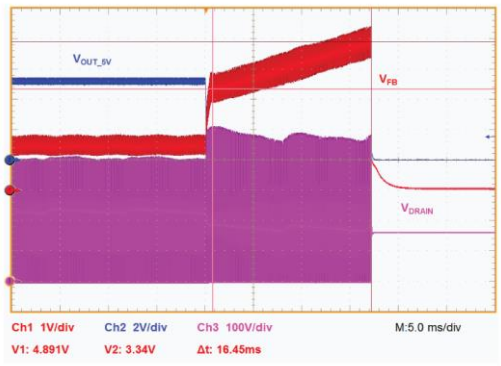


Figure 41: Overload event, continuous overload

5.2 Overvoltage protection

An output overvoltage protection is implemented by monitoring the voltage across the auxiliary winding during the MOSFET turn-off time, through the diode D3 and the resistor divider R5 and R6 connected on the CONT pin of the VIPer37L. If this voltage exceeds the V_{OVP} (3 V typ.) threshold, an overvoltage event is assumed and an internal counter is activated. If this event occurs four times consecutively, the controller recognizes an

overvoltage condition and the device stops switching. This counter provides high noise immunity and avoids spikes erroneously tripping the protection. The counter is reset every time the OVP signal is not triggered in one oscillator cycle.

After the device has stopped switching, to re-enable operation, the V_{DD} voltage must be recycled.

The protection can be tested by opening the resistors connected to the output voltages (R14 for output voltage 1 and R15 for output voltage 2). In this way, the converter operates in an open loop and the excess power with respect to the load charges the output capacitance, thus increasing the output voltage until the OVP is tripped and the converter stops switching.

Figure 42: "Overload event" and *Figure 43: "Overvoltage magnification"* show how the output voltages increase and, consequentially, the CONT pin voltage increases; as it reaches the value of 3 V, the converter stops switching (at the same time, output voltage 1 reaches the value of 7.3 V while the output voltage 2 is about 15 V)

Figure 42: Overload event

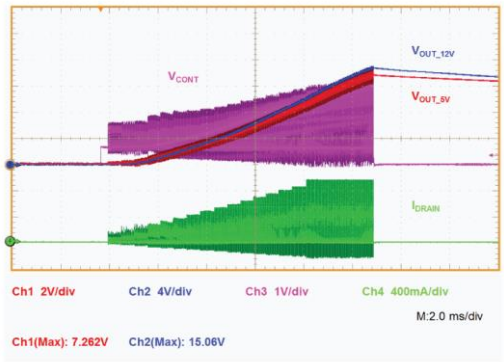
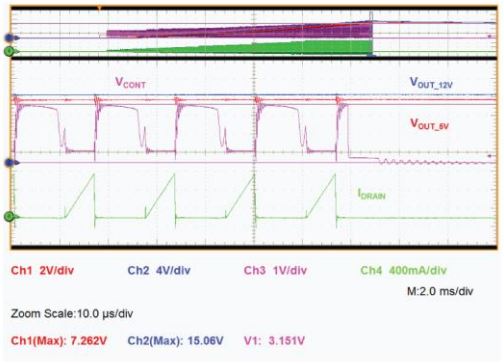


Figure 43: Overvoltage magnification



5.3 Brownout protection

Brownout protection is basically an unlatched device shutdown function typically used is to sense mains undervoltage or disconnection. The VIPer37L has a dedicated BR pin for this function which must be connected to the DC HV bus through a voltage divider.

If the protection is not required, it can be disabled by connecting the pin to ground. In the presented converter, brownout protection is implemented but can be disabled by changing the position of the jumper JMP.

Converter shutdown is accomplished by means of an internal comparator, internally referenced to 450 mV, which disables the PWM if the voltage applied at the BR pin is below this internal reference.

PWM operation is re-enabled when the BR pin voltage rises above 450 mV plus 50 mV voltage hysteresis, to ensures noise immunity. The brownout comparator is also provided with current hysteresis. An internal 10 µA current generator is ON as long as the voltage applied at the brownout pin is below 450 mV and is OFF if the voltage exceeds 450 mV plus the voltage hysteresis.

Figure 44: "Brownout protection: Converter power down phase" shows how the converter powers down when the input bulk voltage goes below about 55 V_{AC}. As this value is lower than V_{DRAIN_START}, the auto-restart mode is disabled. To activate the auto-restart, the input

bulk voltage must rise to V_{DRAIN_START}. By changing the resistor divider value connected to the BR pin, we can power down the converter with an input bulk voltage greater than V_{DRAIN_START} in order to keep the auto-restart mode active.

Figure 45: "Brownout protection: Converter wake up" and *Figure 46: "Brownout protection: Converter wake up - magnification"* show brownout protection during the wake-up phase (with an input bulk voltage greater than V_{DRAIN_START}): once the DC bus reaches about 80 V_{AC}, when the voltage on the V_{DD} pin is higher than V_{DDon}, the IC starts switching.

Figure 44: Brownout protection: Converter power down phase

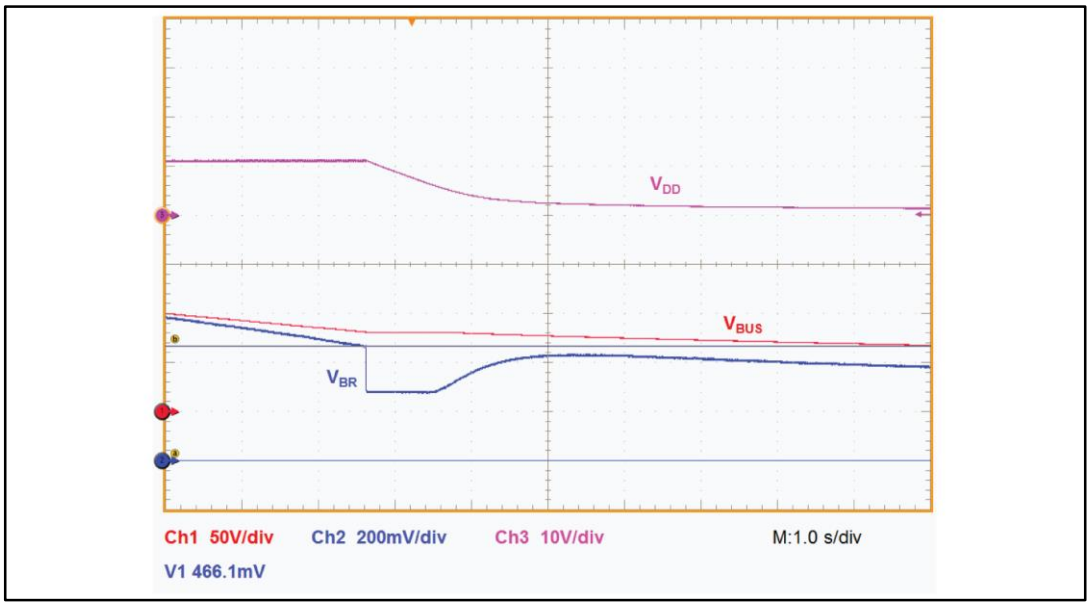


Figure 45: Brownout protection: Converter wake up

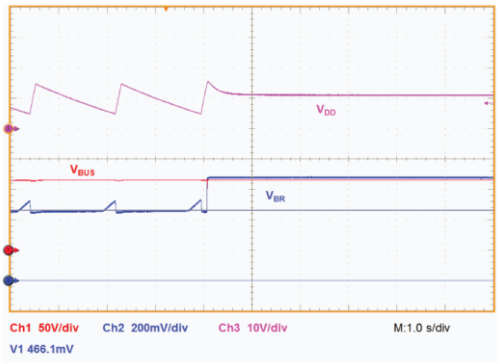
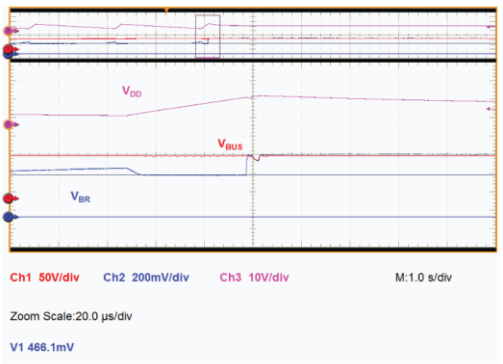


Figure 46: Brownout protection: Converter wake up - magnification



6 Conducted noise measurements

The VIPer37L frequency jittering feature allows the spectrum to be spread over frequency bands rather than being concentrated on single frequency value. Especially when measuring conducted emission with the average detection method, the level reduction can be several dBµV.

A pre-compliance test for the EN55022 (Class B) European normative was performed and average measurements of the conducted noise emissions at full load and nominal mains voltages are shown from *Figure 47: "STEVAL-ISA191V1. CE average measurement at 115VAC full load"* to *Figure 50: "STEVAL-ISA184V1. CE average measurement at 230VAC full load"* for both evaluation boards. As seen in the diagrams, the measurements remain well within the limits under all test conditions.

Figure 47: STEVAL-ISA191V1. CE average measurement at 115VAC full load

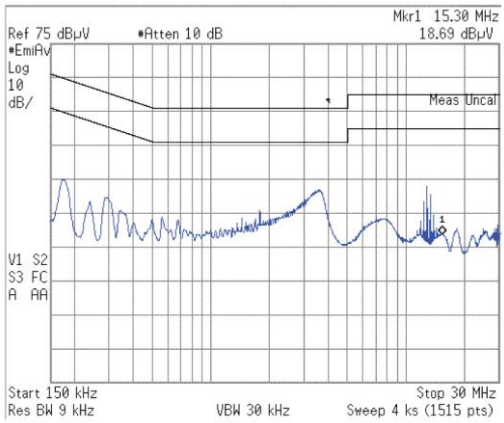


Figure 48: STEVAL-ISA191V1. CE average measurement at 230VAC full load

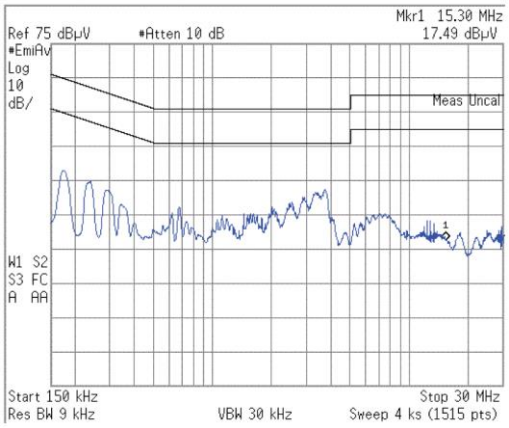


Figure 49: STEVAL-ISA184V1. CE average measurement at 115VAC full load

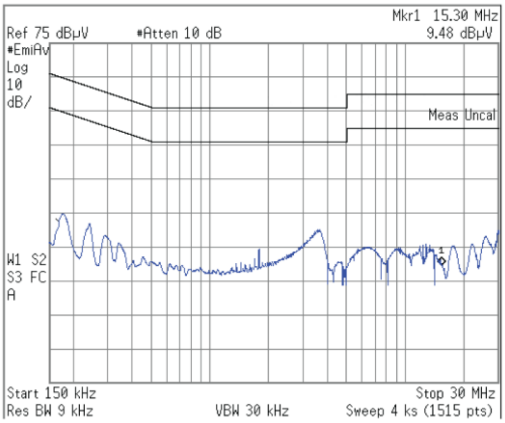
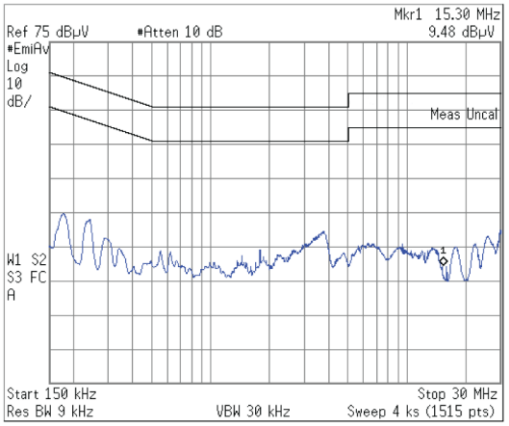


Figure 50: STEVAL-ISA184V1. CE average measurement at 230VAC full load



7 Thermal measurements

A thermal analysis of the boards was performed using an IR camera for the two nominal input voltages (115 V_{AC} and 230 V_{AC}) under full load condition.s The results are shown in *Figure 51: "STEVAL-ISA191V1. Thermal map at 115VAC full load, top layer"* to *Figure 54: "STEVAL-ISA191V1. Thermal map at 230VAC full load, bottom layer"* for the SDIP10 package, from *Figure 55: "STEVAL-ISA184V1. Thermal map at 115VAC full load, top layer"* to *Figure 58: "STEVAL-ISA184V1. Thermal map at 230VAC full load, bottom layer"* for the SO16 package, and summarized in *Table 6: "STEVAL-ISA191V1 - temperature of key components"* and *Table 7: "STEVAL-ISA184V1 - temperature of key components"*.

Figure 51: STEVAL-ISA191V1. Thermal map at 115VAC full load, top layer

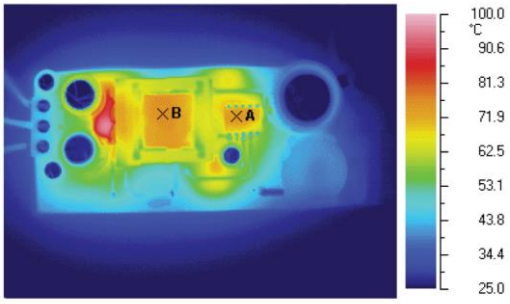


Figure 52: STEVAL-ISA191V1. Thermal map at 115VAC full load, bottom layer

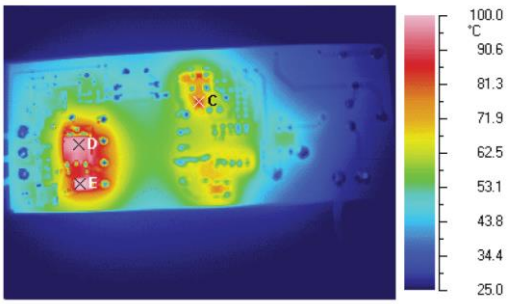


Figure 53: STEVAL-ISA191V1. Thermal map at 230VAC full load, top layer

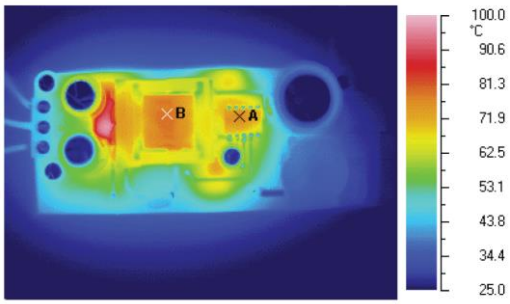


Figure 54: STEVAL-ISA191V1. Thermal map at 230VAC full load, bottom layer

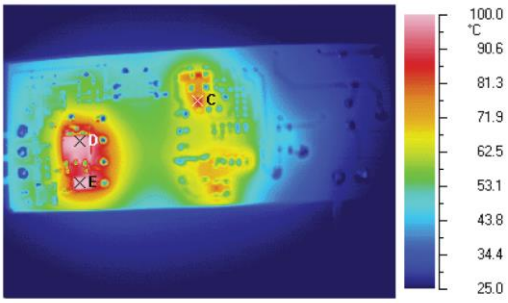


Figure 55: STEVAL-ISA184V1. Thermal map at 115VAC full load, top layer

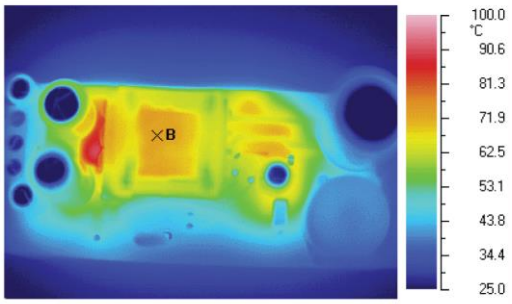


Figure 56: STEVAL-ISA184V1. Thermal map at 115VAC full load, bottom layer

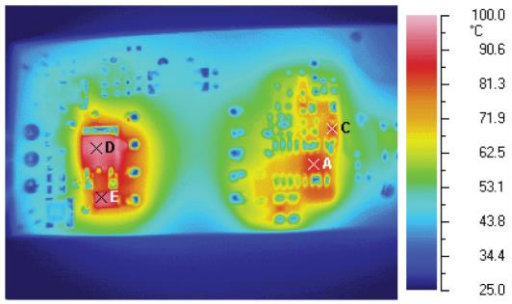


Figure 57: STEVAL-ISA184V1. Thermal map at 230VAC full load, top layer

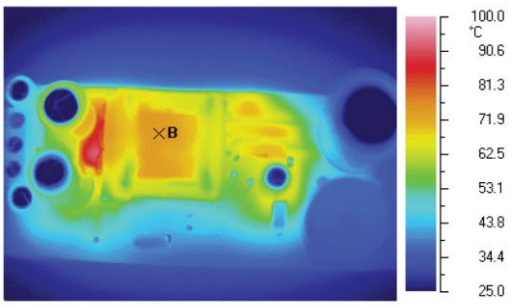
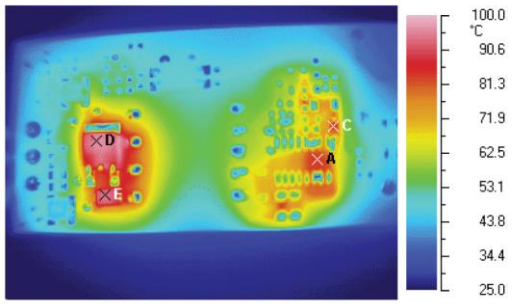


Figure 58: STEVAL-ISA184V1. Thermal map at 230VAC full load, bottom layer



(T_{amb} = 25°C, emissivity = 0.95 for all points).

Table 6: STEVAL-ISA191V1 - temperature of key components

Point	Temp. (°C)		Reference
	115V_{AC}	**230V_{AC}**	
A	75.9	76.9	VIPer37LE
B	76.5	79.3	Transformer
C	85.8	87.1	Zener diode on V_{DD} pin
D	99.1	101	Output 1 diode
E	101.7	103.3	Output 2 diode

(T_{amb} = 25°C, emissivity = 0.95 for all points).

Table 7: STEVAL-ISA184V1 - temperature of key components

Point	Temp. (°C)		Reference
	$115V_{AC}$	$230V_{AC}$	
A	85.1	84.3	VIPer37LE
B	73.9	75.1	Transformer
C	84.8	84.2	Zener diode on V_{DD} pin
D	96.5	97.7	Output 1 diode
E	99.7	100.6	Output 2 diode

8 Conclusions

In the characterization of our flyback converters, special attention was paid to efficiency and low load performance and the results were highly positive, with very low input power under light load conditions. In comparison with the requirements of the EC CoC and DoE regulation programs for external AC-DC adapter, the measured active mode efficiency always exceeded the respective minimum required.

EMI emissions also remained quite low, despite the low cost input filter.

9 Evaluation tools and documentation

The VIPer37LE evaluation board order code is: STEVAL-ISA191V1.

The VIPer37LD evaluation board order code is: STEVAL-ISA184V1.

Further information about this product is available in the VIPer37 datasheet at www.st.com.

10 Revision history

Table 8: Document revision history

Date	Revision	Changes
17-Feb-2016	1	Initial release.

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