AN4940
Application note

12 V, 7.2 W VIPer0P IR remote controlled flyback topology for air conditioning applications using VIPer0P

Introduction

This document describes IR remote controlled single output switch mode power supply set in isolated flyback topology with VIPer0PH and ST ARM Cortex M3 CPU. This SMPS is particularly suitable for air conditioning market and for all kind of power supply that needs to be remotely switched on/off during their working lifecycle.

The STEVAL-ISA181V1 evaluation board features:

- Smart standby architecture using Zero Power Mode (ZPM) with IR remote on/off control suitable for Air Conditioning subsystems and other applications
- Based on VIPer0P high voltage converter with embedded 800V avalanche rugged power MOSEFET and a current mode PWM controller with a set of protections for enhanced system reliability
- Input power consumption in Zero Power Mode lower than 8 mW at $230V_{AC}$ (switched-off by remote IR control) while supplying microcontroller and IR receiver
- Input power consumption at no load less than 30 mW at $230V_{AC}$, including microcontroller consumption
- Average efficiency > 80.2% compliant with EuCoC rev. 5 – Tier 2 and EPS of DOE USA
- Meets IEC55022 Class B conducted EMI even with reduced EMI filter, thanks to the frequency jittering feature
- Meets IEC61000-4-2(ESD), IEC61000-4-4 (EFT) and IEC61000-4-5 (Surge)
- RoHS compliant

Figure 1: STEVAL-ISA181V1 evaluation board (top view)

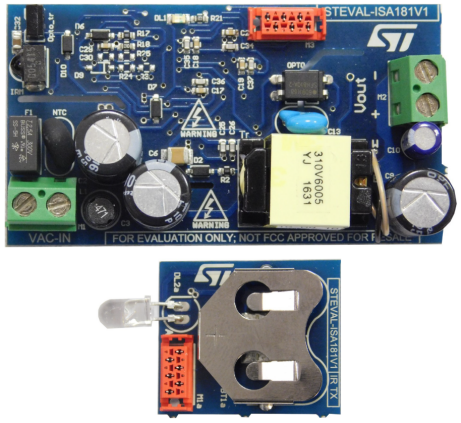
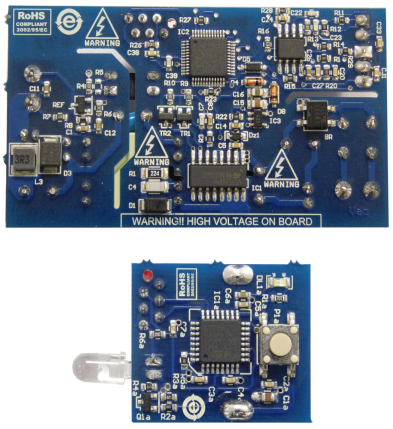


Figure 2: STEVAL-ISA181V1 evaluation board (bottom view)



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1 SMPS features and specifications

This SMPS system features an isolated flyback converter based on VIPer0P and special STM32 core logic to manage the VIPer0P for extremely low power consumption during ZPM while supplying the microcontroller and IR receiver and still maintaining relatively high overall efficiency during normal operation. The IR remote interface consists of a dedicated IR TX board and very low consumption TIA / band pass filter RX.

In the ZPM idle state, the device is shut down fully and the residual consumption from the 230V_{AC} mains is below 5 mW. The IC enters ZPM by pulling the OFF pin to SGND for more than 10 ms and exits ZPM (resuming normal switching) by pulling the ON pin to SGND for more than 20 µs.

This function can be tested by acting on the tactile switches connected to the ON and OFF pins.

The proposed power supply is set in isolated flyback topology with 12 V output voltage and 7.2 W nameplate power.

- Topology: flyback
- Isolation: yes
- Input power consumption:
  - Less than 8 mW at 230 V_{AC} in Zero-Power Mode
  - Less than 30 mW at 230 V_{AC} in no-load condition
  - compliant with EuCoC rev. 5 – Tier 2 and EPS of DOE USA input voltage: 85 V_{AC} - 265 V_{AC}
- Output voltage: 12 V, 600 mA
- Converter frequency: 120 kHz with jittering
- Max ambient temperature: 60 °C
- Automatic restart protections: OLP, VCC clamp, max duty cycle counter, thermal shutdown
- Pulse-skip protection to prevent the flux-runaway
- SMPS board dimensions: 68 mm x 36 mm
- IR TX control board: 28 mm x 25 mm

2 Circuit description

2.1 SMPS

The power supply is set in isolated flyback topology, the switching frequency of the VIPer0PH is 120 kHz (see *Section 3: "Schematic diagrams"* and *Section 4: "Bill of materials"*).

On the SMPS board, the input section includes a fuse and an NTC for protection in series against destructive bench tests; a Pi filter is placed immediately after these for EMC suppression.

Due to the isolated topology, the EAGN pin (floating error amplifier ground reference) and the FB pin (inverting input of the internal error amplifier) are shorted to SGND (see VIPer0P datasheet).

This SMPS requires secondary regulation, so the V_{OUT} is obtained through the transformer secondary windings; the ratio is 9.58:1 and precision and regulation are managed by a TS432ILT external error amplifier on the converter secondary side, working together with the optocoupler and the VIPer0P COMP pin.

The COMP pin (output of the internal error amplifier) is disabled in this configuration; it also is the point where the regulation loop is closed and a compensation network (C7, C8 and R3) placed between itself and SGND pin is required to achieve stability and good dynamic performance.

The PGND pin must be connected to the SGND pin with the shortest track and with the lowest impedance to avoid mismatches between the IC signal ground references and its power section.

On power-up, as V_{DRAIN} exceeds $V_{HVSTART}$, the internal HV current generator charges V_{CC} capacitor C5 to V_{CCon} and the integrated output Power MOSFET starts switching, the current generator is turned off and the VIPer0P is supplied by the energy stored in C5 and can then be externally biased through Schottky rectifier D2 from the transformer auxiliary winding.

2.2 STM32 built-in government unit and algorithm

Zero power mode (ZPM) is a key feature of the VIPer0P; it is an idle state in which the device is totally shut down and the residual consumption from the mains at 230 V_{AC} is kept below 5 mW.

The VIPer0P enters ZPM by pulling the OFF pin to SGND for more than 10 ms and exits ZPM (resuming normal switching) by pulling the ON pin to SGND for more than 20 µs.

The STEVAL-ISA181V1 uses VIPer0P ZPM feature through a sophisticated algorithm in the STM32 ROM. The CPU is powered from LDO when the SMPS is in normal switching and by VIPer0P ON pin integrated current generator through D4 and D8 series diode.

The CPU manages on/off VIPer0P signaling via the following event sequence, assuming that the overall SMPS (both VIPer0P and STM32) is in ZPM:

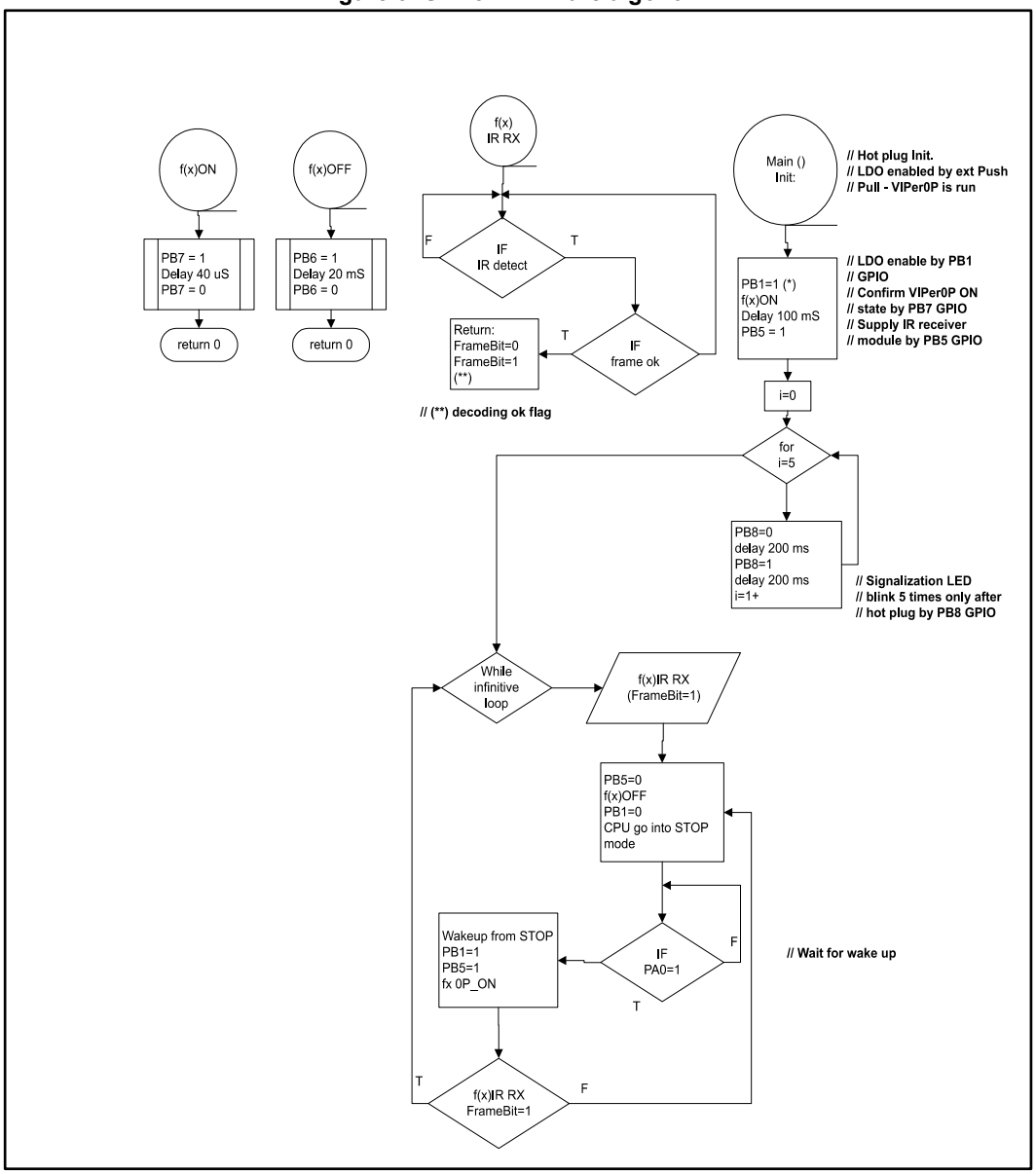
1. when a valid IR signal is detected by the IR receiver block, a wakeup vector is addressed to the microcontroller through PA0 GPIO pin
2. the CPU is in STOP mode and exits from this low power mode
3. shortly after, it supplies the IR receiver module through the PB5 GPIO pin.

The IR receiver module communicates the IR sequence to the microcontroller through a dedicated digital input PA6 GPIO pin, and then performs validates the received IR frame

with respect to the loaded communication protocol. If a power on command is addressed to the right remote controller, it signals the VIPer0P to exit the zero power state mode.

A few milliseconds later, the overall system is switched on and the microcontroller is supplied by the transformer converter auxiliary winding. On the contrary, assuming that the SMPS is switched on, there is no need to wake up the CPU because it is already running, but if the IR receiver module detects a valid IR frame, the CPU cuts off the supply on the IR module, disables the LDO device and gives the switch off signal pulse to VIPer0P. Now the overall system is in ZPM and the SMPS consumption drops below about 8 mW in the worst case.

Figure 3: STM32 firmware algorithm



2.3 Remote infrared receiver

The infrared photodiode is a special device able to generate voltage across its terminal pins when the light (in the order of about 950 nm) strikes its exposed PN junction.

Typically, its equivalent model includes:

- a light-dependent current source in parallel with a high shunt resistor (in the range of few hundreds of MΩ);
- a shunt capacitor in parallel (in the range of 50 pF for a small junction diode or a photo-transistor to hundreds of pF for bigger junction diodes);
- a series resistor (close to 0 Ω).

This equivalent circuit is shown in the figure below.

Figure 4: Photodiode equivalent model

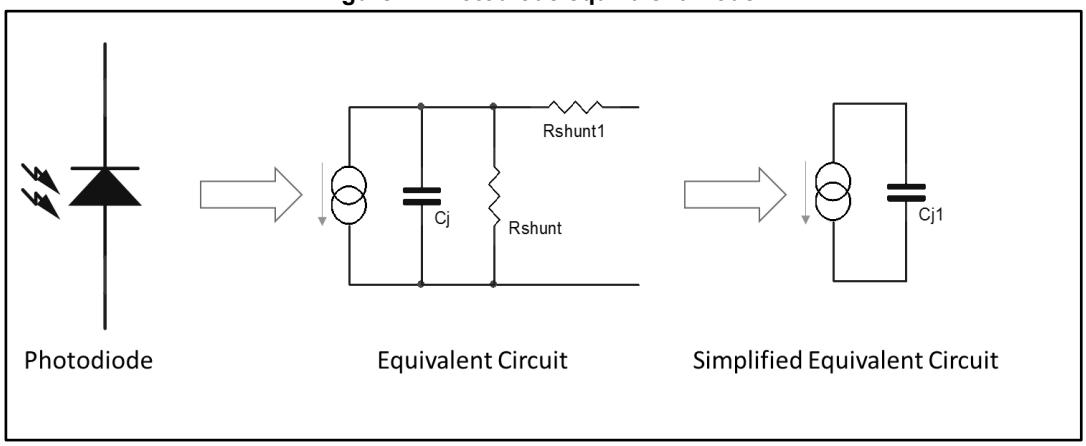
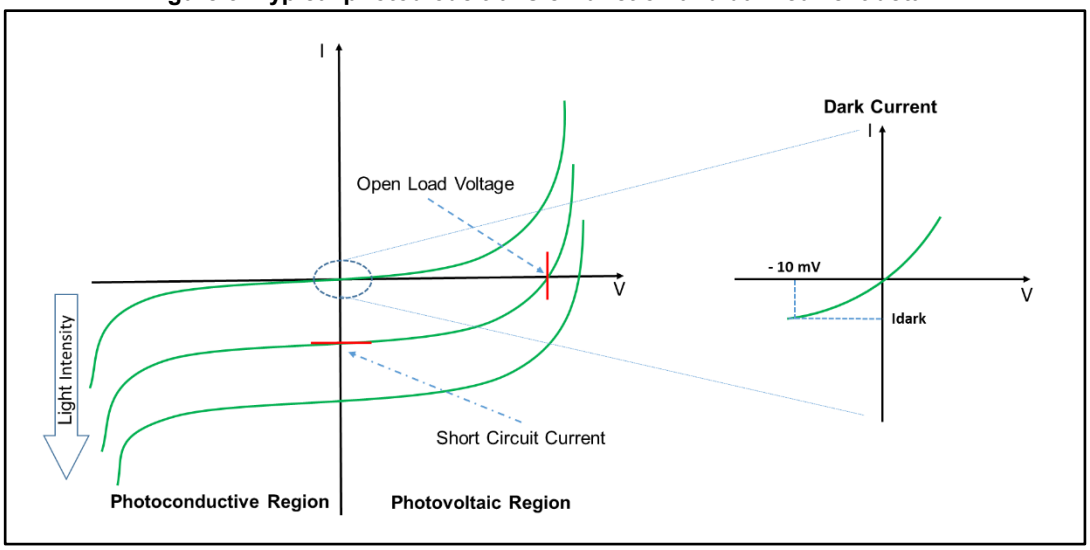


Figure 5: "Typical photodiode transfer function and dark current detail" shows a typical photodiode transfer function: the V/I characteristic is very similar to a normal diode, but the entire curve shifts up and down as a function of the incident light on the exposed PN junction.

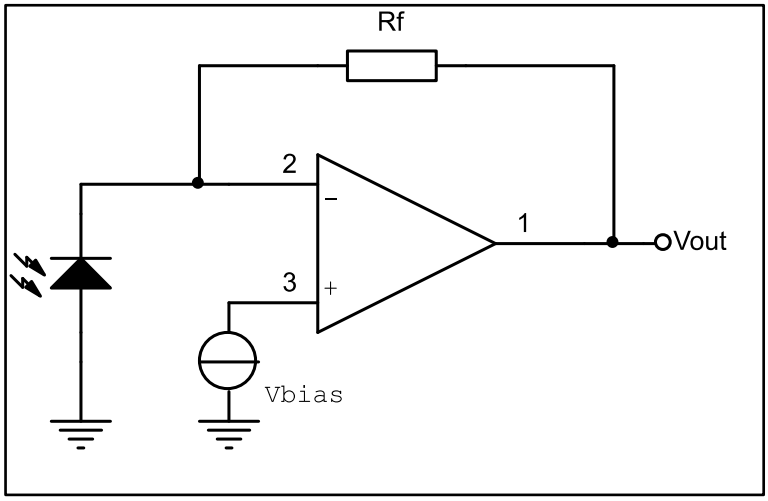
This figure shows also the behavior around the origin, where there is no light: as the photodiode voltage and current are not equal to zero, this phenomena is known as dark current. This parameter is typically specified on the supplier datasheet at minus 10 mV reverse bias.

Figure 5: Typical photodiode transfer function and dark current detail



The dark current is the origin of the output bias error when the signal is amplified by using a photodiode in photovoltaic mode; for this reason, it is convenient to amplify the photodiode signal by using its photoconductive behavior with a trans-impedance amplifier (henceforth called TIA).

Figure 6: TIA basic configuration



In the basic configuration, as showed in *Figure 6: "TIA basic configuration"*, TIA is made by one operational amplifier with a feedback resistor connected between output and inverting input. The photodiode current flows from cathode to anode when the light strikes the photodiode exposed PN junction.

Most photodiode current flows through R_f generating an output voltage equal to the photodiode current multiplied by R_f.

The dark current does not disappear completely because the amplifier input offset voltage results in a small error across the photodiode terminals.

Taking into account that the IR receiver circuit performs two important functions (IR signal conversion into a pulse train to decode the 38.8 KHz remote control signals and wake up signal generation for the CPU), TIA configuration could generate a false CPU awakening due to dark current or ambient light dependence (ambient light can be thought of as a

continuous slowly varying magnitude). Thus, it may be useful to interpose a capacitor between the photodiode and the operation amplifier input to eliminate the component due to dark current and ambient light bias and slow variation in the time domain, implementing an infinite gain multiple feedback (IGMF) band pass filter.

Figure 7: Infinite gain multiple feedback (IGMF) band pass filter

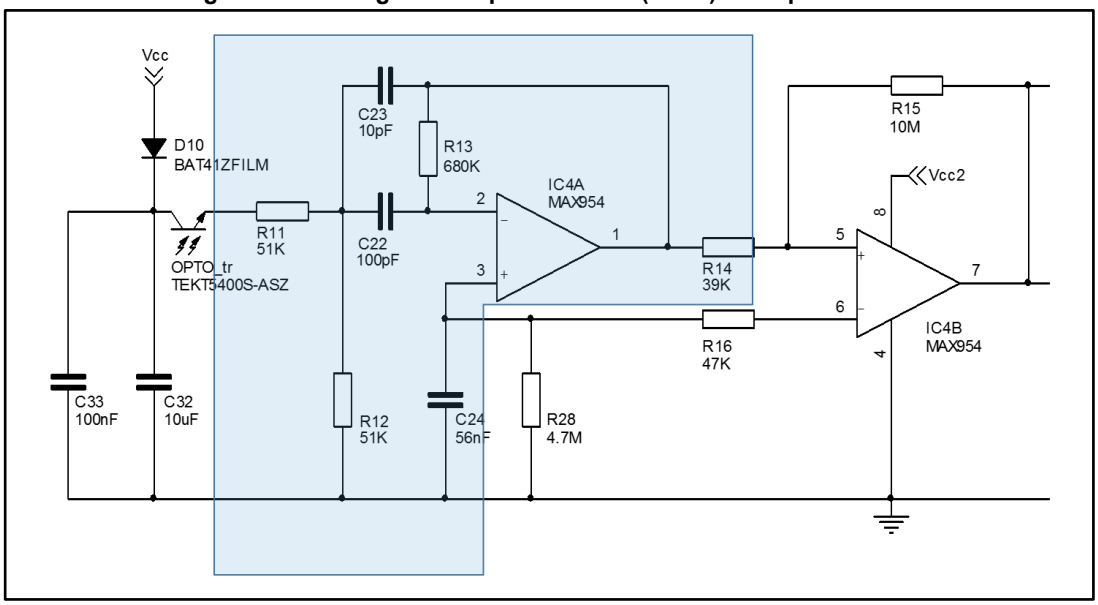


Figure 7: "Infinite gain multiple feedback (IGMF) band pass filter" shows the circuit detail implemented in the STEVAL-ISA181V1 evaluation board. This specific active band pass filter is based on a negative feedback active filter with a high Q factor, a good amplitude response and a steep roll-off on both sides with respect to its center frequency.

The active filter frequency response is very similar to a resonant circuit; for this reason, the filter center frequency is called resonant frequency, f_r.

The resonant frequency response of this second order IGMF band pass filter is calculated by analyzing the response of the two reactive components, C_{22} and C_{23}.

As a result of these two reactive components, the IGMF band pass filter has a peak response at its center frequency, f_c, and it is equal to f_r. The center frequency is calculated inside the oscillation region by geometric means between the two -3dB frequencies, f_L and f_H, and the lower cut-off point up the resonant frequency.

Equation 1

$$f_r = \sqrt{f_L \cdot f_H}$$

where:

- f_r is the resonant or center frequency;
- f_L is the lower -3dB cut-off frequency point;
- f_H is the upper -3dB cut-off frequency point.

This IGMF band pass filter circuit uses the full gain of the operational amplifier, with multiple negative feedback applied via R_{13} resistor and C_{23} capacitor.

The IGMF band pass filter characteristics can also be described as per the following equations:

Equation 2

$$f_r = \frac{1}{2\pi\sqrt{R_{11} \cdot R_{13} \cdot C_{22} \cdot C_{22}}}$$

Equation 3

$$Q_{BC} = \frac{f_r}{BW(3dB)} = \frac{1}{2}\sqrt{\frac{R_{13}}{R_{11}}}$$

Equation 4

$$AV_{max} = -\frac{R_{13}}{2 \cdot R_{11}} = -2Q^2$$

By *Equation 2* it is possible to calculate the frequency at which the maximum amplitude occurs; *Equation 3* underlines the relationship between R_{11} and R_{13} and allows determining the quality factor Q; by *Equation 4* it is possible to calculate the circuit maximum gain that at the end is equal to $-2Q^2$: the related transfer function can calculated by:

Equation 5

$$T(s) = \frac{Vout(s)}{Vin(s)} = \frac{-\frac{1}{R11 \cdot C23} \cdot s}{s^2 + s \cdot (\frac{1}{R13 \cdot C22}) + \frac{1}{R13 \cdot C23 \cdot C22} \cdot (\frac{1}{R11} + \frac{1}{R12})}$$

In all band pass filter circuits the width of the pass band between the upper and lower -3dB corner points determines the circuit Q factor which provides information on the filter selectivity with respect to a given frequency range.

Generally, when the filter gain increases, the selectivity increases too.

The Q factor is also indicated by α and is known as the alpha-peak frequency where:

Equation 6

$$\alpha = \frac{1}{Q}$$

The damping ratio is given by:

Equation 7

$$\xi = 2\alpha$$

The Q factor is given also by the ratio between f_r and the bandwidth (BW):

Equation 8

$$Q = \frac{ResonanteFrequency}{Bandwith}$$

A new approximation to improve the filter design and obtain the best frequency response is arranging the previous formula as per the following equations.

The center frequency is given by:

Equation 9

$$f_0 = \frac{1}{2\pi}\sqrt{\frac{1}{R_{13} \cdot C_{23} \cdot C_{22}}\left(\frac{1}{R_{11}} \cdot \frac{1}{R_{12}}\right)}$$

The Q factor is given by:

Equation 10

$$\boldsymbol{Q} = \frac{1}{2\boldsymbol{\xi}}$$

The transfer function is given by:

Equation 11

$$\boldsymbol{T(s)} = \frac{\boldsymbol{Vout(s)}}{\boldsymbol{Vin(s)}} = \frac{2\boldsymbol{\xi}(2\boldsymbol{\pi f}_0)\boldsymbol{Ks}}{\boldsymbol{s}^2 + 2\boldsymbol{\xi}(2\boldsymbol{\pi f}_0)\boldsymbol{s} + (2\boldsymbol{\pi f}_0)^2}$$

where K is the gain at f_0 and is given by:

Equation 12

$$\boldsymbol{K} = \frac{\boldsymbol{R}_{13}}{\boldsymbol{R}_{11}} \cdot \frac{-\boldsymbol{C}_{22}}{\boldsymbol{C}_{23} + \boldsymbol{C}_{22}}$$

3 Schematic diagrams

Figure 8: SMPS board schematic

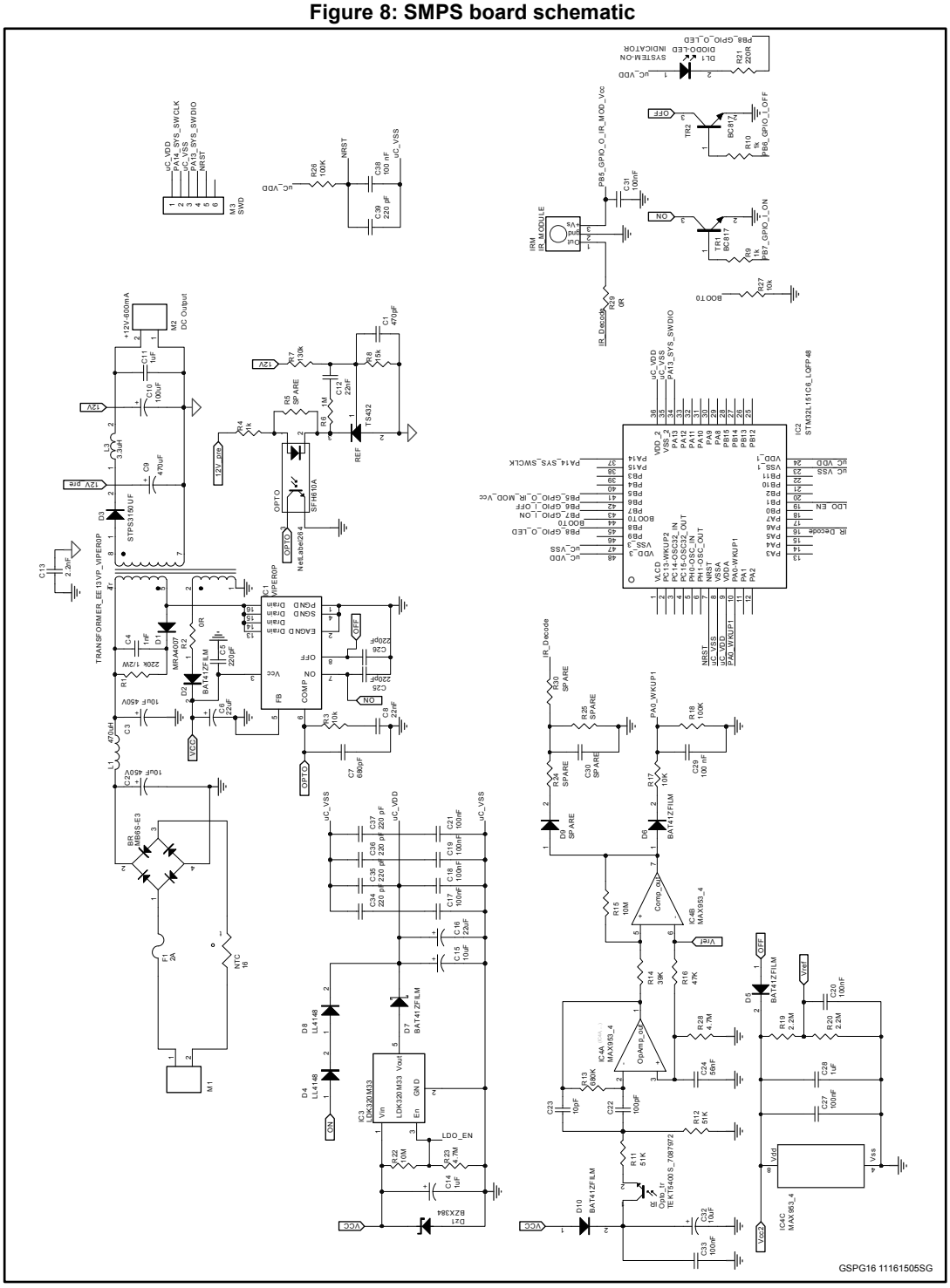
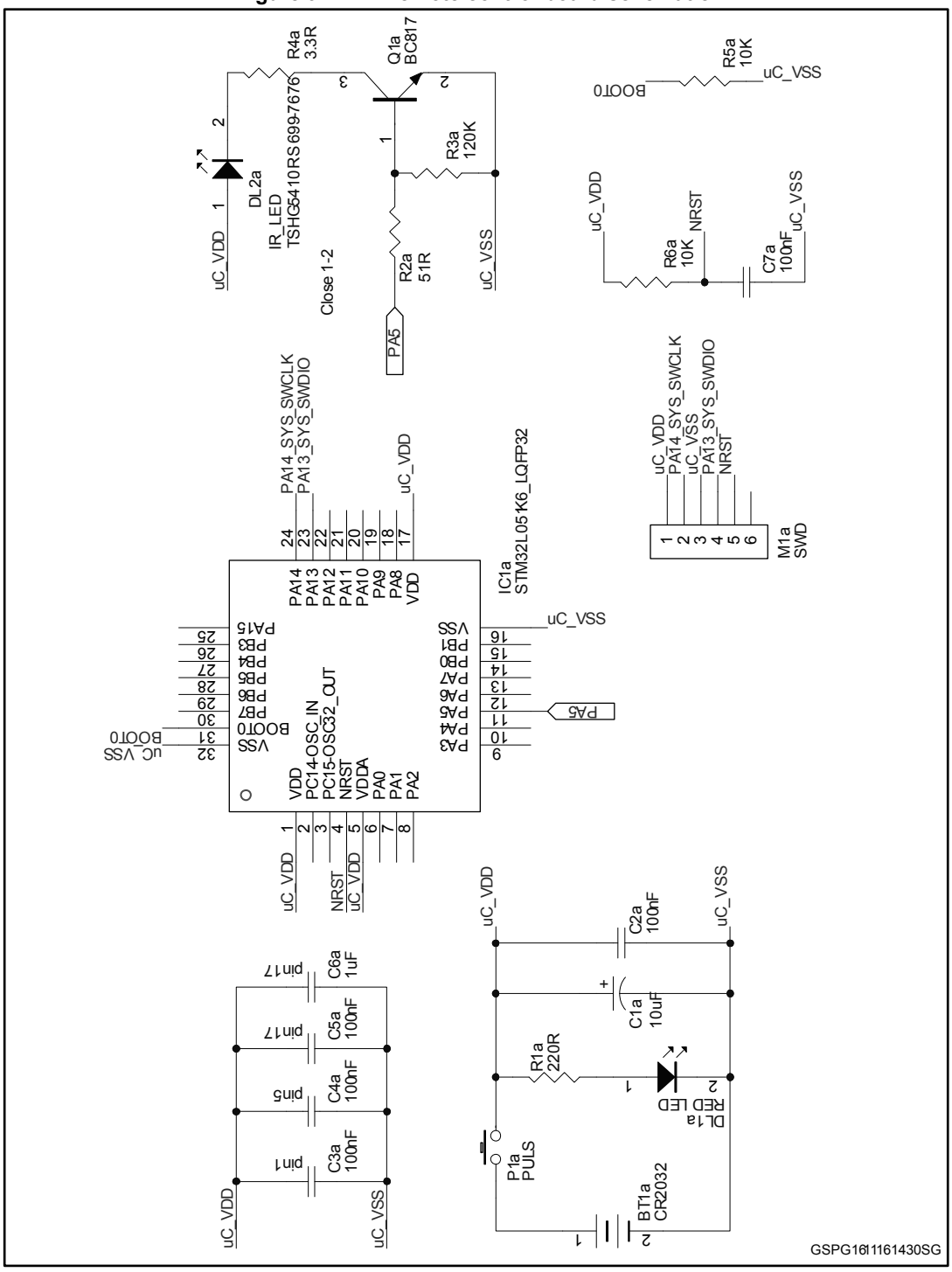


Figure 9: IR TX remote control board schematic



4 Bill of materials

Table 1: SMPS bill of materials

Item	Q.ty	Reference	Value	Description	Manufacturer	Order code
1	1	R1	220 KΩ - 0.33 W - 200 V ± 5 %	TH resistor		ERJ-P08J224V
2	1	R2	0 Ω – 0.1 W ± 1%	SMD resistor		CRCW06030000Z0EB
3	1	R3	10 KΩ - 0.1 W ± 1%	SMD resistor		CRCW060310K0FKEA
4	1	R4	1 KΩ - 0.1 W ± 5 %	SMD resistor		ERJ3GEYJ102V
5	1	R5				Not connected
6	1	R6	1 MΩ - 0.1 W ± 1%	SMD resistor		CRG0603F1M0
7	1	R7	130 KΩ - 0.2 W ± 1%	SMD resistor		ERJP03F1203V
8	1	R8	15 KΩ - 0.2 W ± 1 %	SMD resistor		ERJP03F1502V
9	1	R9	1 KΩ - 0.1 W ± 1 %	SMD resistor		ERJ3GEYJ102V
10	1	R10	1 KΩ - 0.1 W ± 5 %	SMD resistor		ERJ3GEYJ102V
11	2	R11, R12	51 KΩ - 0.1 W ± 1 %	SMD resistor		CRCW060351K0FKEA
12	1	R13	680 KΩ - 0.1 W ± 1 %	SMD resistor		
13	1	R14	39 KΩ - 0.1 W ± 1 %	SMD resistor		CRCW060339K0FKEA
14	1	R15	10 MΩ - 0.1 W ± 1 %	SMD resistor		CRCW060310M0FKEA

Item	Q.ty	Reference	Value	Description	Manufacturer	Order code
15	1	R16	47 KΩ - 0.1 W ± 1 %	SMD Resistor		CRG0603F47K
16	1	R17	10 KΩ - 0.1 W ± 1 %	SMD resistor		CRCW060310K0FKEA
17	1	R18	100 KΩ - 0.1 W ± 1 %	SMD resistor		CRG0603F100K
18	2	R19, R20	2.2MΩ - 0.1W ± 1 %	SMD resistor		CRCW06032M20FKEA
19	1	R21	220 Ω - 0.1 W ± 1 %	SMD resistor		CRG0603F220R
20	1	R22	10 MΩ - 0.1 ± 1 %	SMD resistor		CRCW060310M0FKEA
21	1	R23	4.7 MΩ - 0.1 W ± 1 %	SMD resistor		CRCW06034M70FKEA
22	1	R24				Not connected
23	1	R25				Not connected
24	1	R26	100 KΩ - 0.1 W ± 1 %	SMD resistor		CRG0603F100K
25	1	R27	10 KΩ - 0.1 W ± 1 %	SMD resistor		CRCW060310K0FKEA
26	1	R28	4.7 MΩ - 0.1 W ± 1 %	SMD resistor		CRCW06034M70FKEA
27	1	R29	0 Ω – 0.1 W – ± 1 %	SMD resistor		CRCW06030000Z0EB
28	1	R30				Not connected
29	1	C1	470 pF - 50 V ± 10 %	Ceramic capacitor	Murata	GRM188R71H471KA01D
30	2	C2, C3	10 µF - 400 V ± 20 % - 105°C	Electrolytic capacitor	Rubycon	400AX10MEFC10X12.5
31	1	C4	1 nF- 630 V	Ceramic capacitor	TDK	C3216C0G2J102JT

Item	Q.ty	Reference	Value	Description	Manufacturer	Order code
32	1	C5	220 pF - 16 V	Ceramic capacitor	Murata	GRM188R71H221KA01D
33	1	C6	22 µF- 25 V ± 20 %	X5R ceramic capacitor	Murata	GRM32ER61E226ME15L
34	1	C7	680 pF - 50 V ± 5 %	Ceramic capacitor	Murata	GRM1885C1H681JA01D
35	2	C8, C12	22 nF - 50 V ± 10 %	Ceramic capacitor	Murata	GRM188R71H223KA01D
36	1	C9	470 µF - 25 V ± 20 % 105 °C	Electrolytic capacitor	Rubycon	25ZLJ470M10X12.5
37	1	C10	100 µF - 16 V ± 20% - 105 °C	Electrolytic capacitor	Rubycon	16YXF100M6.3X11
38	2	C11, C14	1 µF – 25 V ± 10%	X6S Ceramic capacitor	Murata	GRM188C81E105KAADD
39	1	C13	2.2 nF - 250 V_{ac}	X1/Y1 Ceramic capacitor	Murata	DE2E3KY222MA2BM01
40	2	C15, C32	10 µF- 25 V ± 10 %	X5R Ceramic capacitor	TDK	C2012X5R1E106K125AB
41	1	C16	22 µF - 6.3 V ± 20 %	Ceramic capacitor	Kemet	C0805C226M9PACTU
42	8	C17, C18,C19, C20, C21, C29, C31, C33	0.1 µF - 16 V ± 10%	X7R Ceramic capacitor	Kemet	C0603C104K4RACTU
43	2	C22, C23	100 pF - 50 V ± 5 %	Ceramic capacitor	Kemet	C0603C101J5GACTU
44	1	C24	56 nF - 50 V ± 10 %	Ceramic capacitor	Kemet	C0603C563K5RACTU
45	6	C25, C26, C34, C35, C36, C37, C39	220 pF - 50 V ± 5 %	Ceramic capacitor	Kemet	C0603C221J5GACTU

Item	Q.ty	Reference	Value	Description	Manufacturer	Order code
46	2	C27, C38	0.1 µF - 16 V ± 10 %	X7R Ceramic capacitor	Kemet	C0603C104K4RACTU
47	1	C28	1 µF – 25 V ± 10%	X6S Ceramic Capacitor	Murata	GRM188C81E105KAADD
48	1	C30				Not connected
49	1	BR	1 A – 600 V	Bridge		RMB6S
50	1	D1	1 A - 1000 V	Standard recovery rectifier		MRA4007T3G
51	1	D2	0.15 A - 100 V	Signal Schottky rectifier	STMicroelectronics	BAT41ZFILM
52	1	D3	3 A – 150 V	Signal Schottky rectifier	STMicroelectronics	STPS3150U
53	1	D4, D8	0.2 A - 100 V	Fast switching diodes		FDLL4148X
54	4	D5, D6, D7, D10	0.15 A - 100 V	Signal Schottky rectifier	STMicroelectronics	BAT41ZFILM
55	1	D9				Not connected
56	1	DZ1	300 mW - 18 V	Zener diode	NXP Semiconductors	BZX384
57	1	IC1		Offline primary controller	STMicroelectronics	VIPer0PH
58	1	IC2		ARM Cortex M3 32 MHz 32 kByte CPU	STMicroelectronics	STM32L151C6T6
59	1	IC3		Low drop voltage regulator	STMicroelectronics	LDK320M33
60	1	IC4		OPAMP and comparator IC	MAXIM	MAX954ESA+
61	2	TR1, TR2	45 V - 500 mA - 250 mW	Bipolar junction transistor		BC817-40LT3G
62	1	REF		Voltage reference IC	STMicroelectronics	TS432ILT
63	1	OPTO		Optocoupler	Vishay	SFH610A-2
64	1	DL1		Green LED	Lite-On	LTST-C170GKT

Item	Q.ty	Reference	Value	Description	Manufacturer	Order code
65	1	OPT_TR		IR – Phototransistor	Vishay	TEKT5400S-ASZ
66	1	IRM		IR – receiver module	Sharp	GP1UX310QS
67	1	NTC	20 Ω	NTC	Ametherm	SL08 20002
68	1	Tr		Flyback Transformer	YuJingtech	11999-310V600510
69	1	L1	470 µH	Axial Inductor	Wurth Elektronic	7447462471
70	1	L3	3.3 µH	Power inductor	Wurth Elektronic	74404043033A
71	1	F1		Fuse	Cooper Bussmann	SS-5H-2-5A-BK
72	1	M3		Six contact connector	TE Connectivity	338068-6

Table 2: Infrared transmitter controller board bill of materials

Item	Q.ty	Reference	Value	Description	Manufacturer	Order code
1	1	BT	3 V – 210 mAh	CR2032 Li-Ion battery		
2	1	BT1a		Battery holder for CR2032	Keystone	3003
3	1	C1a	10 µF - 25 V ± 10 %	X5R Ceramic capacitor	TDK	C2012X5R1E106K125AB
4	5	C2a, C3a, C4a, C5a, C7a	0.1 µF - 16 V ± 10 %	X7R Ceramic capacitor	Kemet	C0603C104K4RACTU
5	1	C6a	1 µF - 25 V ± 10 %	X6S Ceramic capacitor	Murata	GRM188C81E105KAADD
6	1	DL1a		Green LED	Lite-On	LTST-C170GKT
7	1	DL2a	Pwr. intensity 900 mW/sr – λ 850 nm	R LED	Vishay	TSHG5410
8	1	IC1a		ARM Cortex M0 32 MHz 32 kByte CPU	STMicroelectronics	STM32L051K6
9	1	M1a		Six contact connector	TE Connectivity	338068-6
10	1	P1a	0.05 A – 24 V	Tactile push button	Omron	B3S-1000

Item	Q.ty	Reference	Value	Description	Manufacturer	Order code
11	1	Q1a	45 V – 500 mA - 250 mW	Bipolar junction transistor		BC817-40LT3G
12	1	R1a	1 KΩ – 0.1 W ± 5 %	SMD resistor	Panasonic	ERJ3GEYJ102V
13	1	R2a	51 Ω – 0.1 W ± 1 %	SMD resistor	Vishay	CRCW060351R0FKEA
14	1	R3a	130 KΩ - 0.2 W ± 1%	SMD resistor	Panasonic	ERJP03F1203V
15	1	R4a	3.3 Ω – 0.1 W ± 5%	SMD resistor	Bourns	CRL0603-JW-3R30ELF
16	1	R5a	10 KΩ – 0.1 W ± 1%	SMD resistor	Vishay	CRCW060310K0FKEA
17	1	R6a	100 KΩ – 0.1 W ± 1%	SMD resistor	TE Connectivity	CRG0603F100K

5 Transformer

Table 3: Transformer electrical specifications

Parameter	Value	DRC (Ω)
Manufacturer	Yujing Technology CO. LTD.	
Order code	11999-310V600210 V1.0	
Primary inductance (pins 5 - 4)	850 µH ± 10%	2.8 max.
Leakage inductance (pins 5 - 4)	40 µH max.	
Secondary inductance (wire F1 – F2)	22 µH	0.17 max.
Auxiliary inductance (pins 1 - 2)	32 µH	0.57 max.
Primary to secondary turn ratio (4 - 2)/(8 - 7)	(9.58):(1.00), ± 1 %	

Table 4: Transformer electrical strength

Parameter	Limit value	Apply to
Withstanding voltage	4.0 KV / 3 sec. / AC / 5 mA	Primary to secondary winding
	1.0 KV / 3 sec. / AC / 5 mA	Primary winding to core
	3.0 KV / 3 sec. / AC / 5 mA	Secondary winding to core

Figure 10: Dimensional drawing and pin placement diagram (electrical diagram)

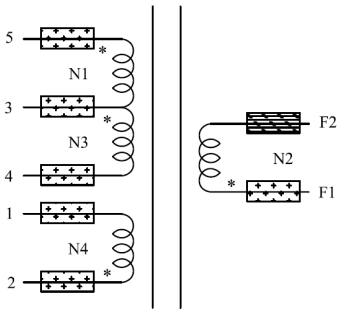


Figure 11: Dimensional drawing and pin placement diagram (bottom view)

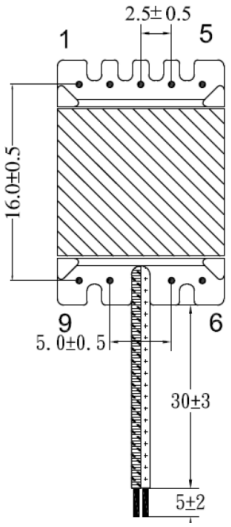
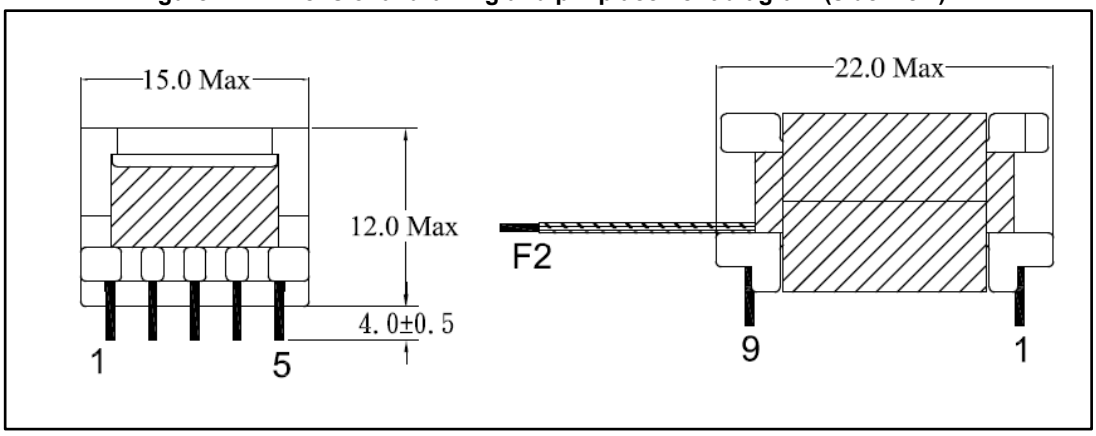


Figure 12: Dimensional drawing and pin placement diagram (side view)



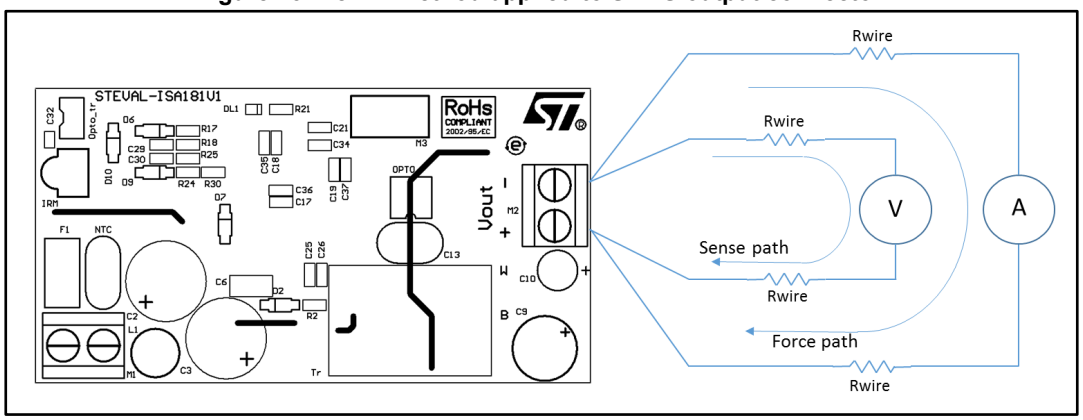
6 Testing the board

6.1 Efficiency

The active mode efficiency is defined as the average of the efficiencies measured at 25%, 50%, 75% and 100% of the maximum load, at nominal input voltages, V_{IN} is in the range of 115 V_{AC} and 230 V_{AC}. External power supplies are contained in a separate housing from the end-use devices they are powering and they need to comply with the Code of Conduct, version 5 "Active mode efficiency" criterion, which, for a power throughput of 7 W, states an active mode efficiency higher than 77% (CoC5 tier1, effective since January 2014); this limit has been increased to 80% since January 2016 (CoC5 tier2). Another standard to be applied is the DOE (department of energy) recommendation, whose active mode efficiency requirement for the same power throughput is 79.8%.

STEVAL-ISA181V1 output V/I characterization is performed by using the four-wire Kelvin method as shown in the following figure.

Figure 13: Kelvin method applied to SMPS output connector



The SMPS is compliant with the Code of Conduct 5 Tier1 at both 115 V_{AC} and 230 V_{AC} and compliant with the Code of Conduct 5 Tier2 and DOE only at 230 V_{AC}:

Table 5: Active mode efficiency

V_{IN}	STEVAL-ISA181V1 performance	CoC5 requirements for P_{OUT} = 7 W Tier2	DOE requirement for P_{OUT} = 7 W
115 V_{AC}	82.5%	80%	79.8%
230 V_{AC}	82.2%		

Figure 14: Efficiency vs. output current load

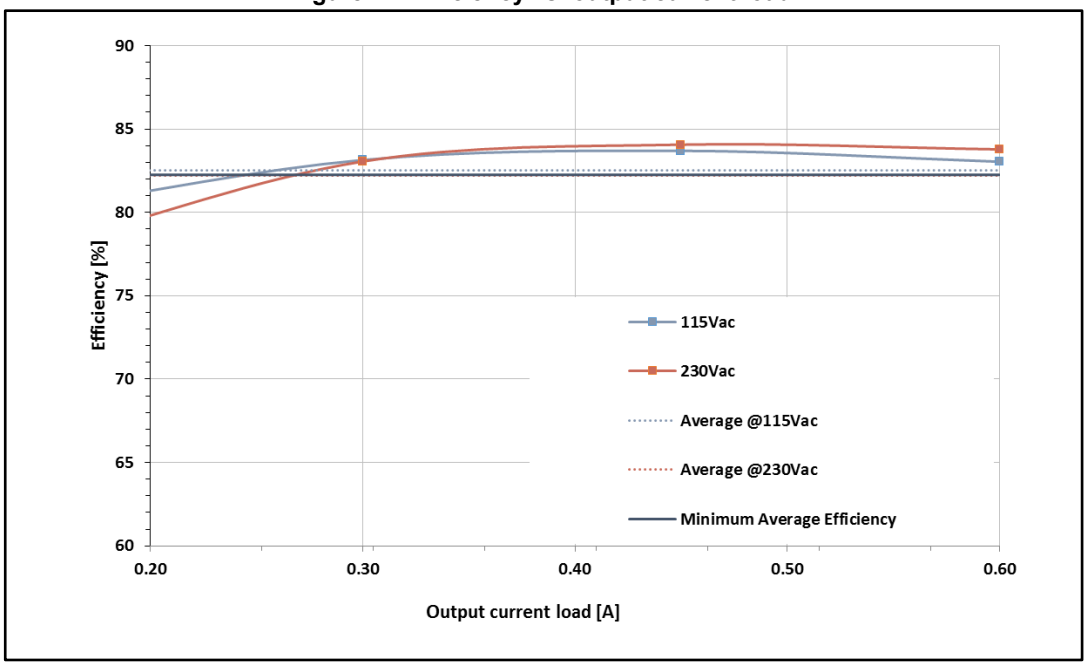


Figure 15: Efficiency vs. input voltage at different output current load

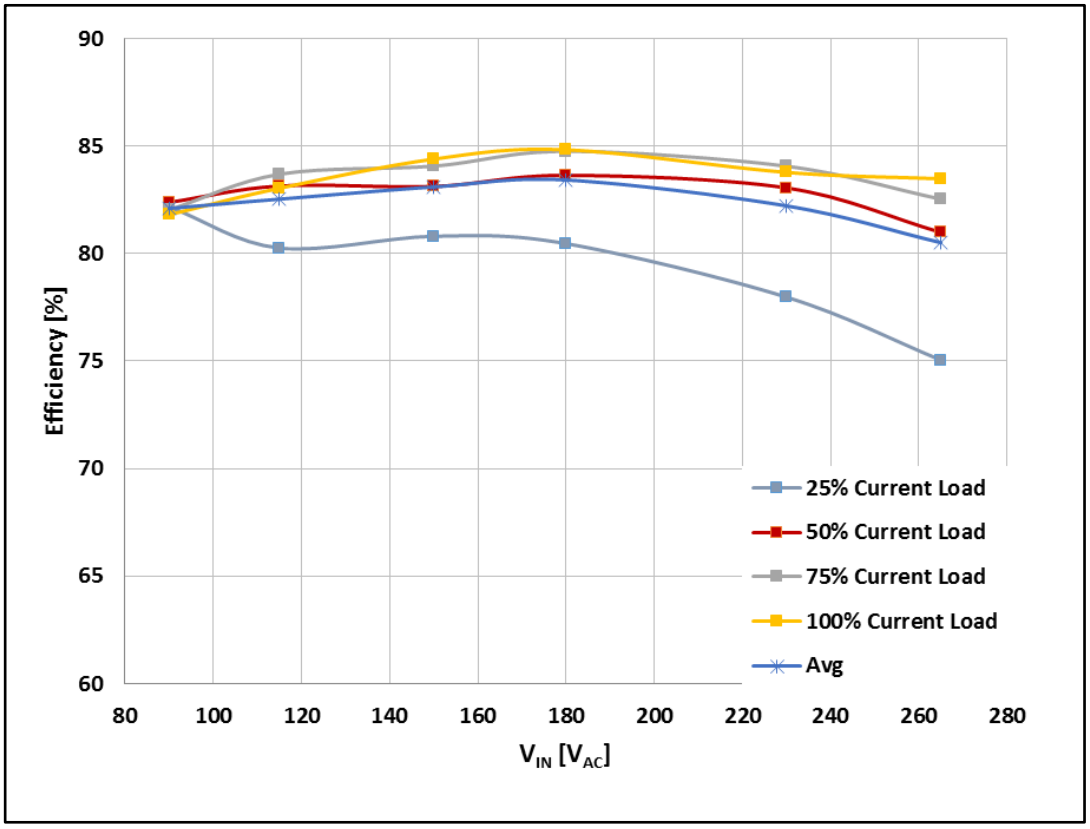


Table 6: "STEVAL-ISA181V1 input power consumption at no load and in ZPM" shows the consumption in zero power mode (ZPM). In this idle state the VIPer0P is totally shut down, the STM32 is in low power consumption “STOP mode” and the SMPS overall consumption is reduced below 10 mW, which is considered zero consumption.

Table 6: STEVAL-ISA181V1 input power consumption at no load and in ZPM

V_{IN} [V_{AC}]	P_{IN} [mW]	
	Consumption at no load	Consumption in ZPM
115	28	3
230	28	5

6.2 Output voltage characteristics

The STEVAL-ISA181V1 output voltage is measured at different line regulations and load conditions. *Figure 16: "Output voltage load regulation at 115 V_{AC} - 230 V_{AC}"* shows the output voltage whereas the diagram in *Figure 17: "Line regulation at full load and no load"* is derived for full load condition (600 mA).

Considering a line input variation and the different load conditions, the output voltage values is practically unaffected.

Figure 16: Output voltage load regulation at 115 V_{AC} - 230 V_{AC}

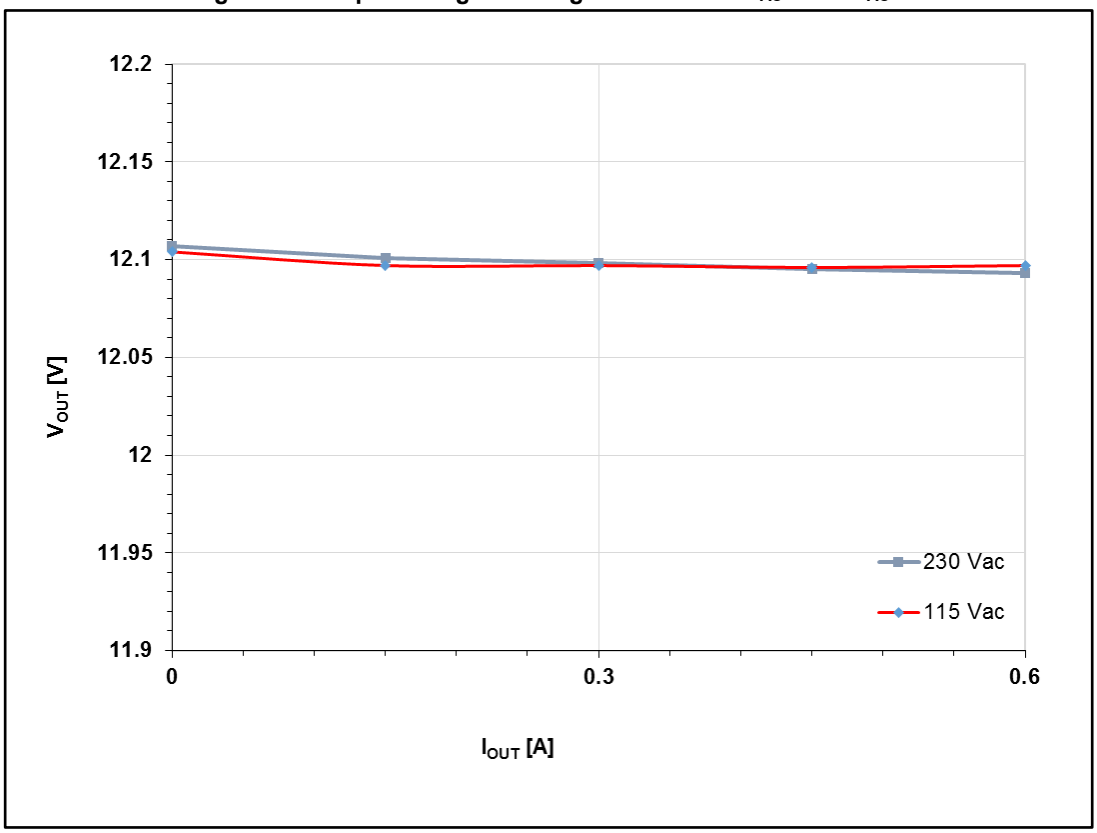
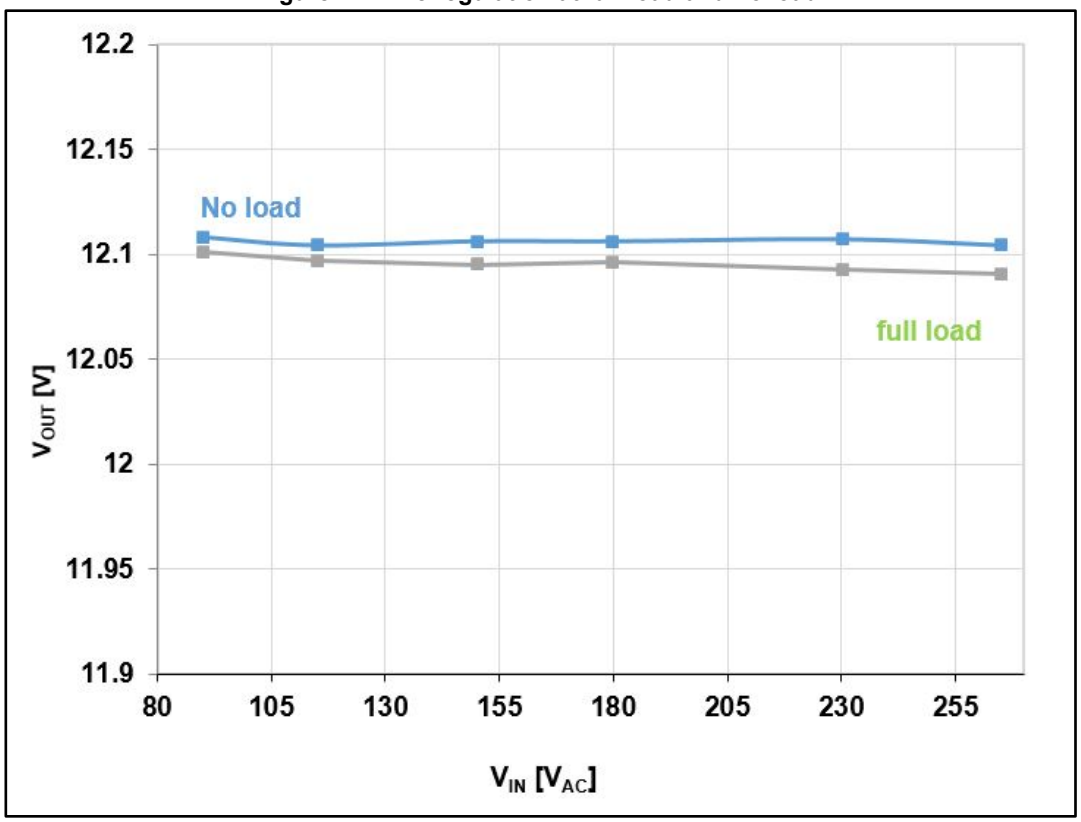


Figure 17: Line regulation at full load and no load



6.3 Typical waveforms

Drain voltage and current waveforms at full load condition are shown in *Figure 18: "Drain current/voltage at 115 V_{AC}, max. load"* and *Figure 19: "Drain current/voltage at 230 V_{AC}, max. load"* for the two nominal input voltages and in *Figure 20: "Drain current/voltage at 90 V_{AC}, max. load"* and *Figure 21: "Drain current/voltage at 265 V_{AC}, max. load"* for the minimum and maximum input voltage respectively.

The converter is designed to operate in continuous conduction mode (CCM) at full load condition.

The CCM allows the root mean square currents value to be reduced, at the primary side, in the VIPer0P power switch and in the transformer primary winding; at the secondary side, in the D3 output diode and in the C9 and C10 output capacitors.

Reducing RMS currents means reducing the power dissipation in the VIPer0P and the stress of the secondary side components.

Figure 18: Drain current/voltage at 115 V_{AC}, max. load

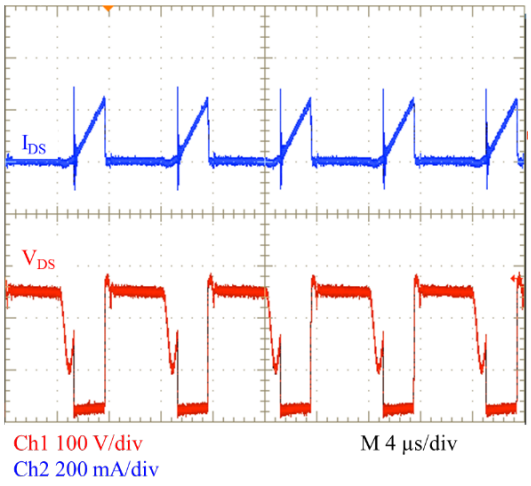


Figure 19: Drain current/voltage at 230 V_{AC}, max. load

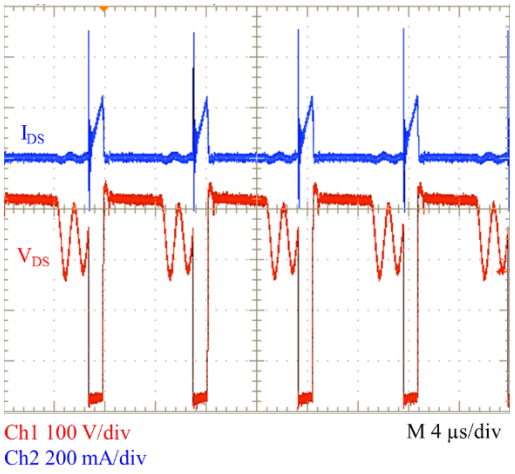


Figure 20: Drain current/voltage at 90 V_{AC}, max. load

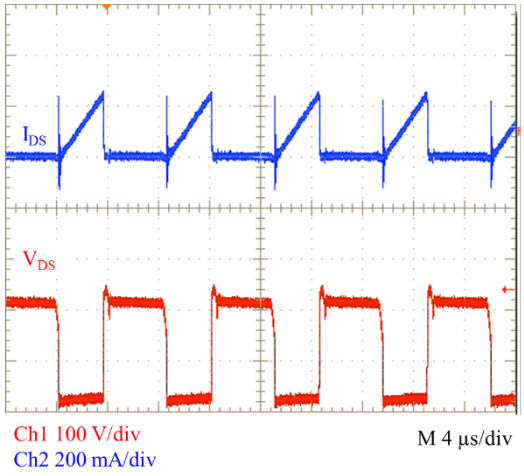
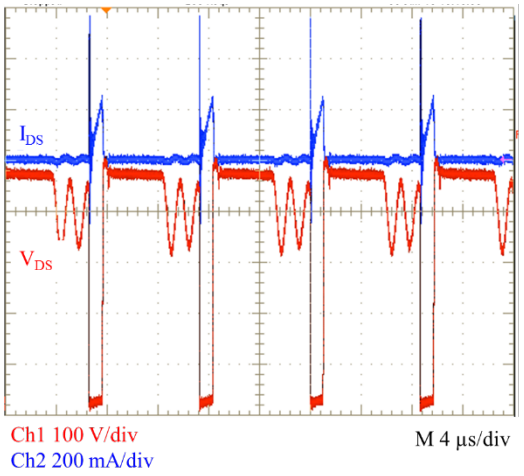


Figure 21: Drain current/voltage at 265 V_{AC}, max. load



The ripple at the switching frequency superimposed at the output voltage has also been measured.

The evaluation board is provided with LC filters on the output, to further reduce the ripple without reducing the overall output capacitor ESR.

The voltage ripple across the output connector (12 V net in the schematic) and before the LC filter (12V_pre net in the schematic) is measured, to verify the LC filter effectiveness.

Figure 22: "Output voltage ripple at 115 V_{AC}, full load" and *Figure 23: "Output voltage ripple at 230 V_{AC}, full load"* show voltage ripple on output voltage at full load.

Figure 24: "Output voltage ripple at 115 V_{AC}, burst mode" and *Figure 25: "Output voltage ripple at 230 V_{AC}, burst mode"* show voltage ripple on output voltage when the device works in burst mode.

Figure 22: Output voltage ripple at 115 V_{AC}, full load

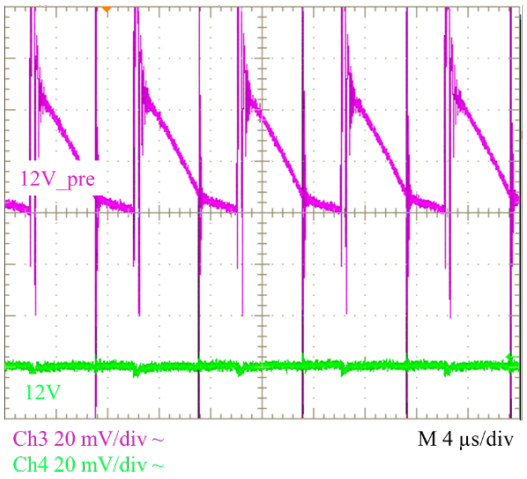


Figure 23: Output voltage ripple at 230 V_{AC}, full load

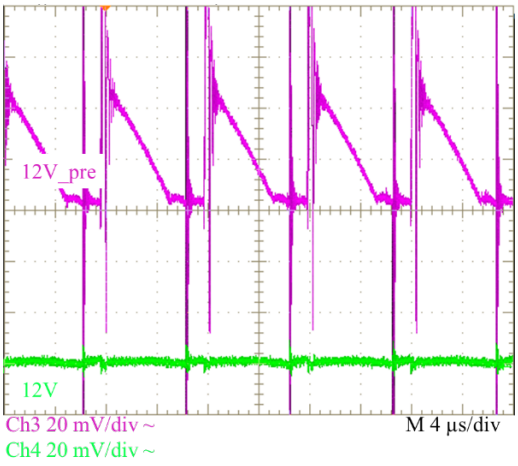


Figure 24: Output voltage ripple at 115 V_{AC}, burst mode

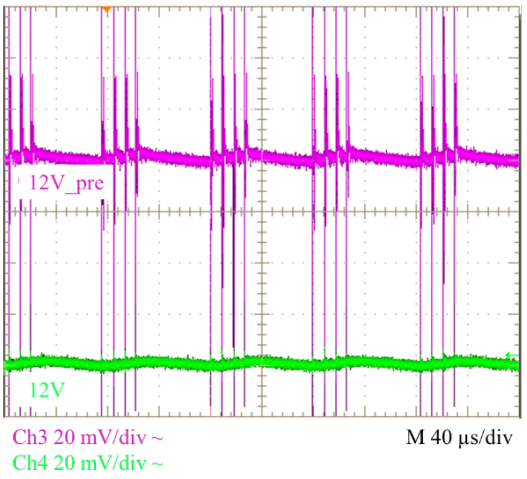
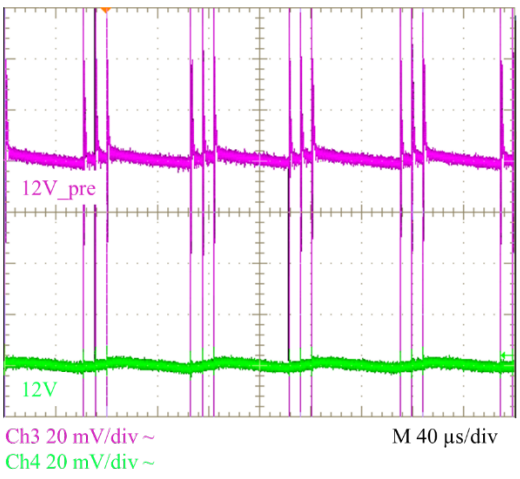


Figure 25: Output voltage ripple at 230 V_{AC}, burst mode



6.4 Soft start and hot plug

When the converter starts, the output capacitor is discharged and needs some time to reach the steady state condition. During this time, the control loop power demand is at the maximum, whereas the reflected voltage is low. These conditions could lead to the converter deep continuous working mode.

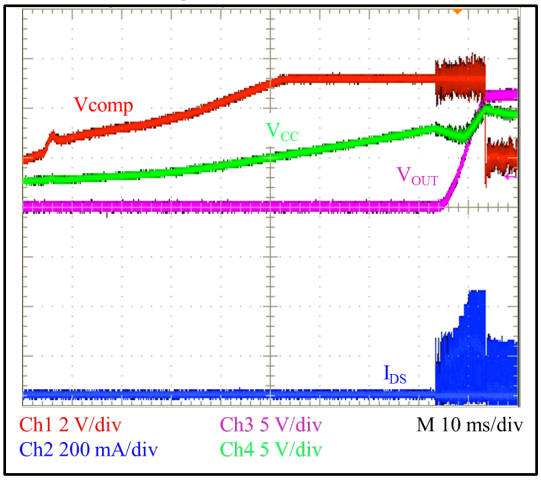
Furthermore, when the MOSFET is switched on, it cannot be immediately switched off as the minimum on time (T_{ON_MIN}) must have elapsed. Because of the converter deep continuous working mode, during T_{ON_MIN}, a drain current excess can overstress the converter component, the device itself, the output diode and the transformer. Transformer saturation can also occur.

To avoid all these negative effects, the VIPer0P implements an internal soft start feature. As the device starts working, no matter the control loop request, the drain current is allowed to gradually increase the cycle-by-cycle current limitation set point from zero up to I_{DLIM} in 8 steps of 50 mA each.

In this way, the drain current is limited during the output voltage increase, thus reducing the stress on the secondary diode. This function is activated at any attempt of converter start up and after a fault event.

The following figure shows the converter soft start phase when operating at minimum line voltage and under maximum load.

Figure 26: Soft start



When the converter starts for the first time, a clever solution (called hot plug condition) is implemented to overcome the transient extra current sink from CPU, typically hundreds of µA, due to STM32 quiescent current (typical of all microcontrollers not specific to 8 or 32 bit STMicroelectronics microcontroller architecture).

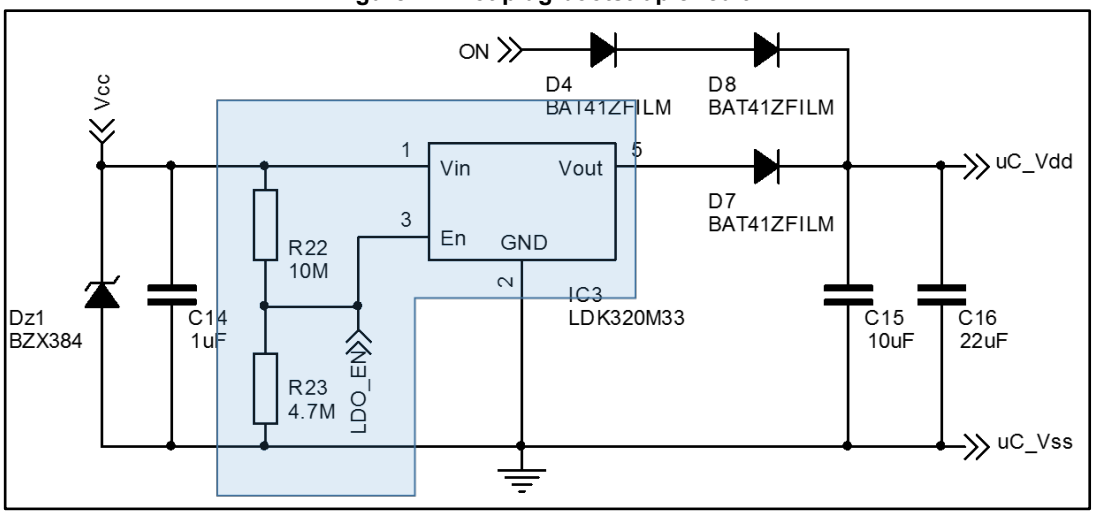
This extra current consumption could be a startup problem as, during “hot plug”, the LDO_EN net is uncontrolled by the CPU and the LDO voltage regulator (IC3 in *Figure 27: "Hot plug bootstrap circuit"*) is in off state.

With the LDO voltage regulator switched off, the CPU is powered on only through a 10 µA pin integrated current generator, as when the system is in zero power mode, but with the fundamental difference that the CPU firmware has not yet started.

To ensure a proper sequence of events even before the implemented Finite State Machine takes control, a bootstrap circuit made by R22 and R23 series resistor is implemented. As soon as the V_{CC} increases, the resistor partition ratio allows the V_{LDO_EN} to reach the LDO voltage regulator power-on threshold and it ensures the proper CPU power up.

After that, the CPU decides whether to maintain the whole system turned on or to push the VIPer0P in zero power mode and bring itself into the designed low power consumption mode (only a few hundreds nA needed by the CPU and about 1 µA for the IR receiver block).

Figure 27: Hot plug bootstrap circuit



6.5 Overload and short-circuit protection

In case of over load or short-circuit, the drain current value reaches I_{DLIM}. Every cycle this condition is met, an internal OCP counter is incremented; if the overload is maintained continuously for the time t_{OVL} (typically 50 ms internally fixed as shown in *Figure 28: "OLP: short-circuit applied during steady state"*), the counter reaches its end-of-count and the protection is tripped; the power section is turned off and the converter is disabled for a $t_{RESTART}$ time (typically 1 s).

After this time has elapsed, the VIPer0P resumes switching and, if the short is still present, the protection occurs indefinitely in the same way (see *Figure 29: "OLP: short-circuit applied during steady state ($t_{RESTART}$)"*). This ensures restart attempts of the converter at a low repetition rate, so that it works safely with extremely low power throughput and avoiding the VIPer0P overheating in case of repeated overload events.

Moreover, every time the protection is tripped, the internal soft start-up function is invoked as shown in *Figure 30: "OLP: short-circuit maintained (t_{SS} and t_{OVL})"*, to reduce the stress on the secondary diode.

After the short removal, the VIPer0P resumes working normally. If the short is removed during t_{SS} or t_{OVL} (as before the protection tripping), the counter is decremented on a cycle-by-cycle basis down to zero and the protection is not tripped.

If the short-circuit is removed during $t_{RESTART}$, the VIPer0P has to wait until $t_{RESTART}$ has elapsed before resuming to switch (see *Figure 31: "OLP: short-circuit removed and auto-restart"*).

Figure 28: OLP: short-circuit applied during steady state

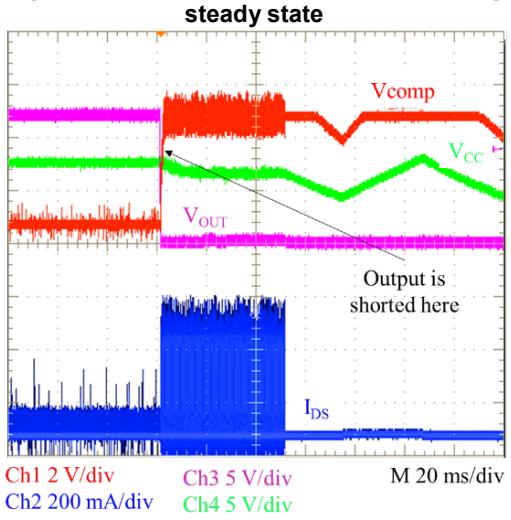


Figure 29: OLP: short-circuit applied during steady state ($t_{RESTART}$)

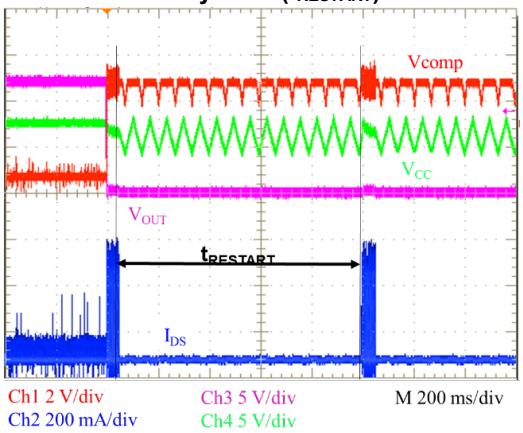


Figure 30: OLP: short-circuit maintained (t_{SS} and t_{OVL})

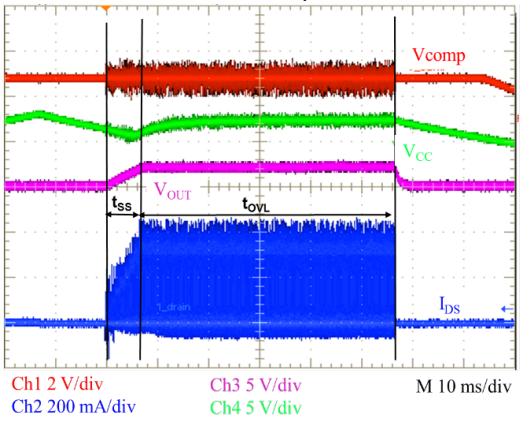
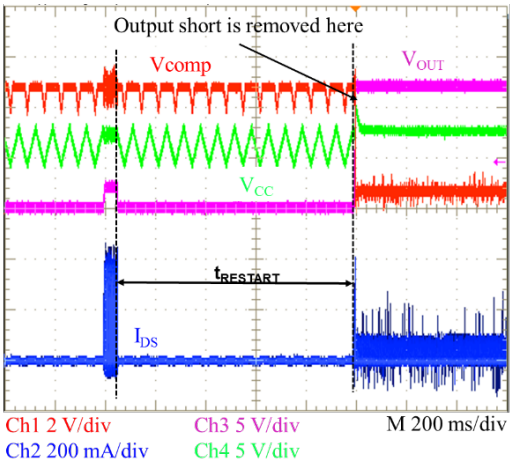


Figure 31: OLP: short-circuit removed and auto-restart



6.6 Zero power mode

The zero power mode is a state of the SMPS characterized by:

- no switching activity; thus, no voltage nor power available on the output in the converter secondary side;
- controller consumption reduced to a very low value, as all VIPer0P blocks are turned off, except the two current generators inside ON and OFF pins and the bias block inside V_{CC} pin need to supply external CPU and IR receiver sub-block to guarantee exit from ZPM.

With an adequate design of all the STEVAL-ISA181V1 components, in ZPM the SMPS could draw less than 8mW at 230 V_{AC} from the mains (as described in *Table 6: "STEVAL-ISA181V1 input power consumption at no load and in ZPM"*), which is considered a “zero power consumption” condition.

Figure 32: "Entering ZPM" shows as, through the CPU dedicated GPIO pin, the OFF pin is forced to SGND for more than t_{DEB_OFF} (typically 10 ms) the VIPer0P enters ZPM, switching is stopped, V_{CC} is charged up to 13 V, most of the internal blocks are disabled and the consumption is reduced to a low value. Consequentially, also the CPU enters a specific low power consumption state named STOP mode to collapse its current consumption to hundreds of nA.

Figure 32: Entering ZPM

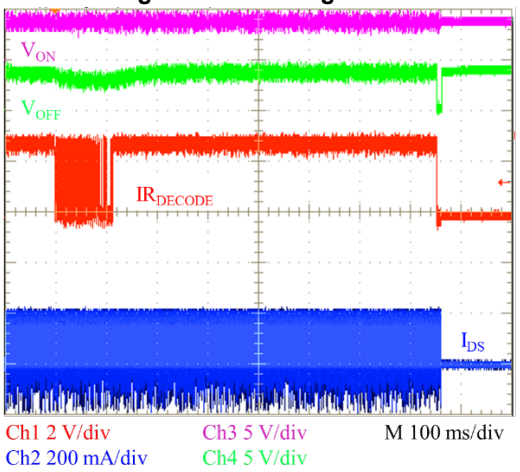
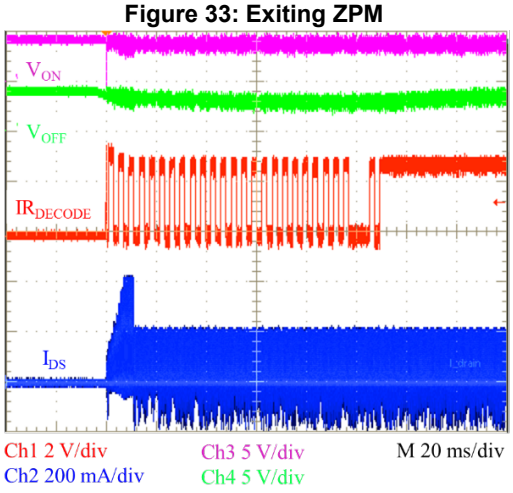


Figure 33: Exiting ZPM



As already explained in *Section 2.2: "STM32 built-in government unit and algorithm"*, when a valid IR signal is detected and decoded by the IR receivers, the CPU, through a dedicated GPIO pin, forces the ON pin to SGND for more than t_{DEB_ON} (typically 20 µs), after that the VIPer0P exits from ZPM (*Figure 33: "Exiting ZPM"*) and resumes switching with a soft start phase delivering again power to the output.

7 Conducted noise measurements

A pre-compliant test to EN55022 (Class B) European normative has been performed using an EMC analyzer and a LISN.

Peak and average measurements have been conducted as reported in *Figure 34: "Peak measurements at 230 V_{AC}, full load, T_{AMB} = 25°C"* and *Figure 35: "Average measurements at 230 V_{AC}, full load, T_{AMB} = 25°C"* respectively.

Figure 34: Peak measurements at 230 V_{AC}, full load, T_{AMB} = 25°C

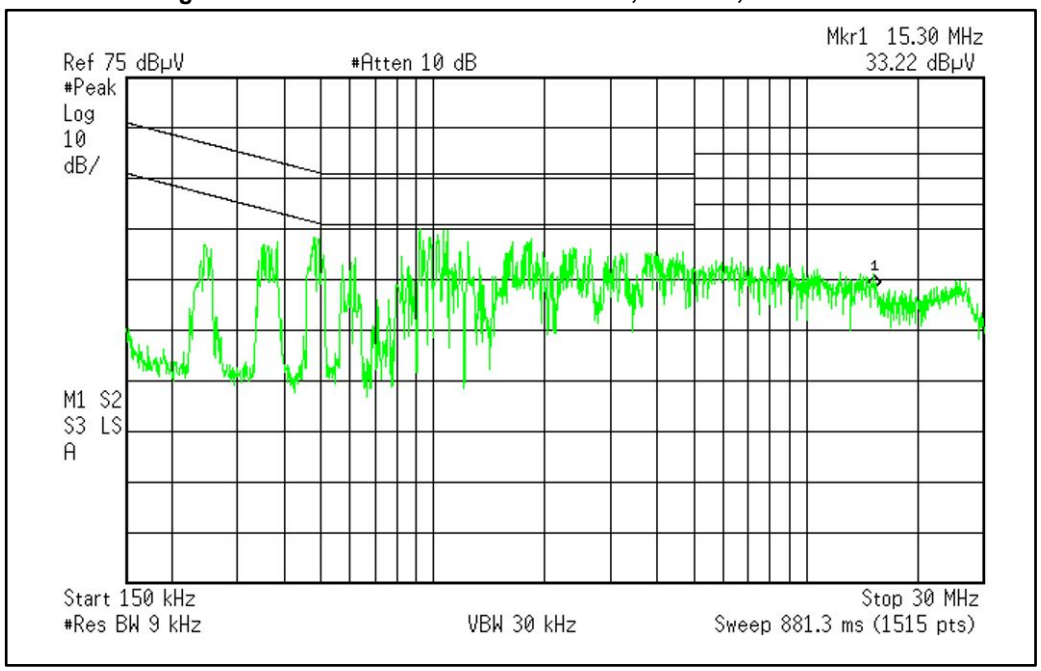
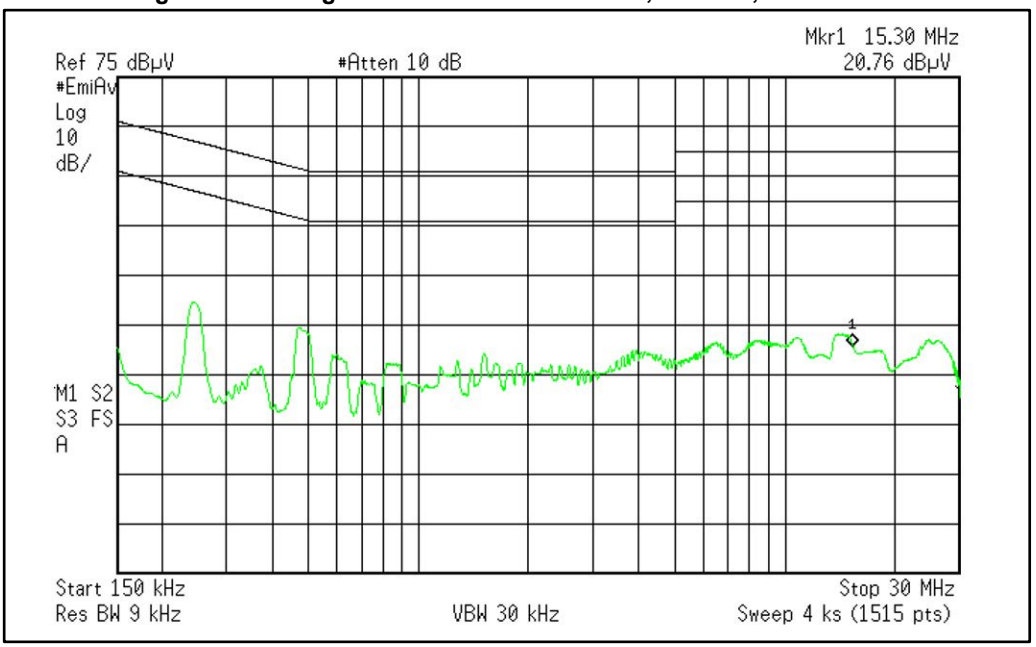


Figure 35: Average measurements at 230 V_{AC}, full load, T_{AMB} = 25°C



8 Immunity tests

The board was submitted to immunity tests according to IEC61000 and their results are classified according to the standard criteria:

- A: normal performance;
- B: temporary degradation or loss of function or performance, with automatic return to normal operation;
- C: temporary degradation or loss of function, with external intervention to re-cover normal operation
- D: degradation or loss of function, necessary substitution of damaged components to recover normal operation

8.1 ESD immunity test (IEC 61000-4-2)

The test was performed on a single test board. The input voltage was set to 230 V_{AC}, the output was loaded to full load and the proper operation was verified by connecting a current probe to the output.

The test conditions are:

- Contact discharge and air discharge methods
- Discharge circuit150 pF/330 Ω
- Polarity: positive / negative
- A network made up by two Y1 capacitors connected across the AC line connector according to the norm.

The test results are listed in the following tables.

Table 7: ESD contact discharge test results

Noise injection	ESD level	Polarity	Result	Criterion
L vs. PE	10 kV	Positive	PASS	A
L vs. PE	10 kV	Negative	PASS	A
N vs. PE	10 kV	Positive	PASS	A
N vs. PE	10 kV	Negative	PASS	A

Table 8: ESD contact discharge test results with PE connected on secondary GND

Noise injection	ESD level	Polarity	Result	Criterion
L vs. GND	8 kV	Positive	PASS	A
L vs. GND	8 kV	Negative	PASS	A
N vs. GND	8 kV	Positive	PASS	A
N vs. GND	8 kV	Negative	PASS	A

Table 9: ESD air discharge test results

Noise injection	ESD level	Polarity	Result	Criterion
Horizontal coupling plane	20 kV	Positive	PASS	A
Horizontal coupling plane	20 kV	Negative	PASS	A
Vertical coupling plane	20 kV	Positive	PASS	A
Vertical coupling plane	20 kV	Negative	PASS	A

8.2 Surge immunity test (IEC 61000-4-5)

The test was performed on a single test board. The input voltage was set to 230 V_{AC}, the output was loaded to full load and the proper operation was verified by connecting a current probe to the output.

The test conditions are:

- repetition rate: 30 seconds
- number of repetitions: 5 each
- applied to input lines vs. EARTH – common mode
- applied to input line (L vs. N) - differential mode
- a network made up by a varistor and two Y1 capacitors connected across the AC line connector according to the norm.

The test results are listed in the following tables.

Table 10: Common mode surge test results

Noise injection	Surge level	Polarity	Result	Criterion
L vs. PE	2 kV	Positive	PASS	A
N vs. PE	2 kV	Positive	PASS	A
L vs. PE	2 kV	Negative	PASS	A
N vs. PE	2 kV	Negative	PASS	A

Table 11: Differential mode surge test results

Noise injection	Surge level	Polarity	Result	Criterion
L vs. N	2 kV	Positive	PASS	A
L vs. N	2 kV	Negative	PASS	A

Performed tests show that the board withstands the lightning disturbances applied to input line in common mode and differential mode for each severity level.

According to the standard, the application can be classified as level 3.

8.3 Burst immunity test (IEC 61000-4-4)

The test was performed on a single test board. The input voltage was set to 230 V_{AC}, the output was loaded with 10% of the nominal load and the proper operation was verified by connecting a current probe to the output.

The test conditions are:

- polarity: positive/negative
- burst duration: 15 ms ± 20 % at 5 kHz
- burst period: 300 ms ± 20 %
- duration time: 1 minute
- applied to: AC lines through integrated capacitive coupling clamp.

The test results are listed in the following table.

Table 12: Burst test results

Noise injection	Burst level	Polarity	Result	Criterion
L	4 kV	Positive	PASS	A
N	4 kV	Positive	PASS	A
PE	4 kV	Positive	PASS	A
L / PE	4 kV	Positive	PASS	A
N / PE	4 kV	Positive	PASS	A
L / N	4 kV	Positive	PASS	B
L / N / PE	4 kV	Positive	PASS	A
L	4 kV	Negative	PASS	A
N	4 kV	Negative	PASS	A
PE	4 kV	Negative	PASS	A
L / PE	4 kV	Negative	PASS	A
N / PE	4 kV	Negative	PASS	A
L / N	4 kV	Negative	PASS	A
L / N / PE	4 kV	Negative	PASS	A

9 Board layout

Figure 36: SMSP board layout: complete

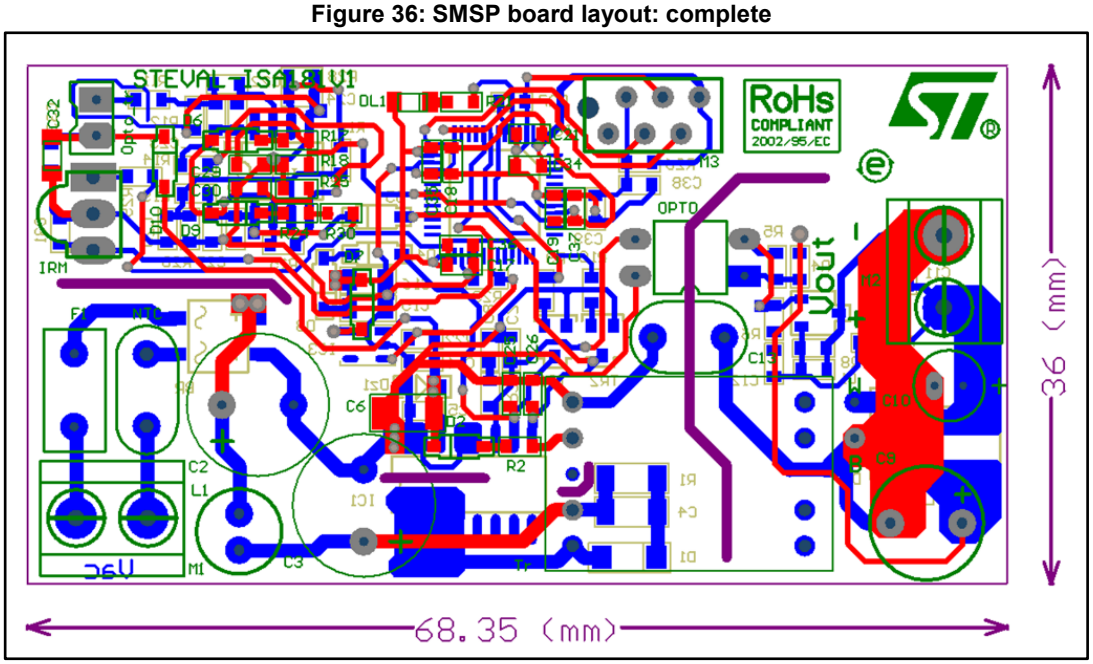


Figure 37: SMSP board layout: top layer + top overlay

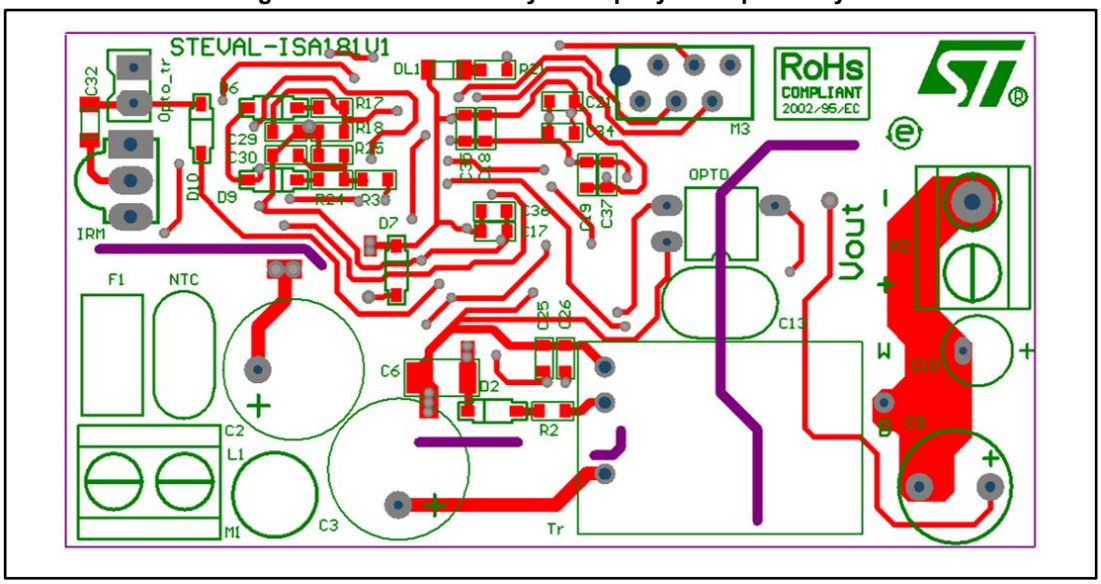


Figure 38: SMSP board layout: bottom layer + mirrored top overlay

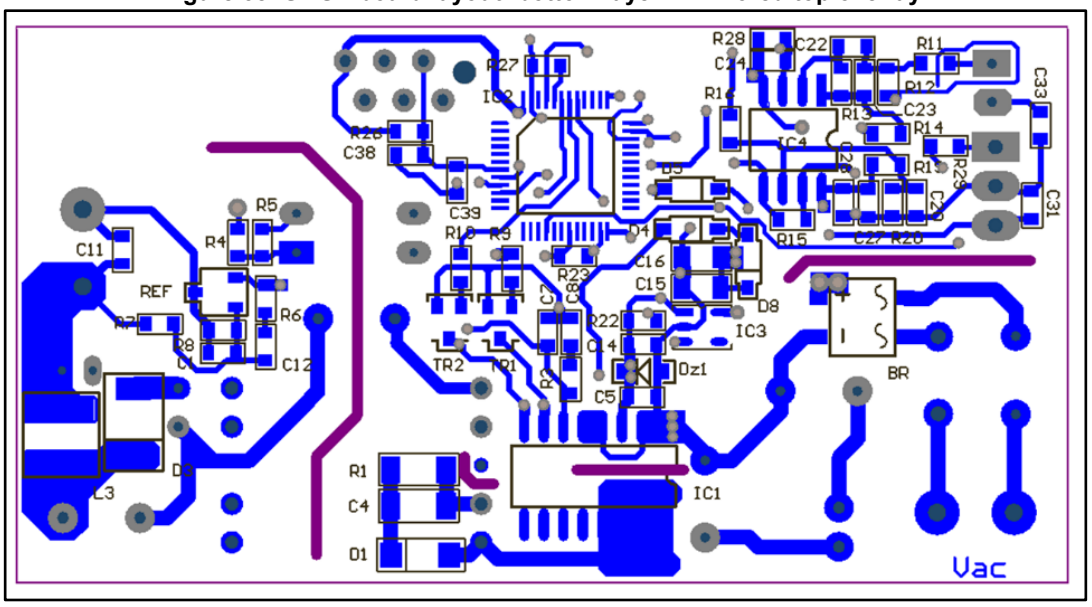


Figure 39: IR TX remote control board layout: complete

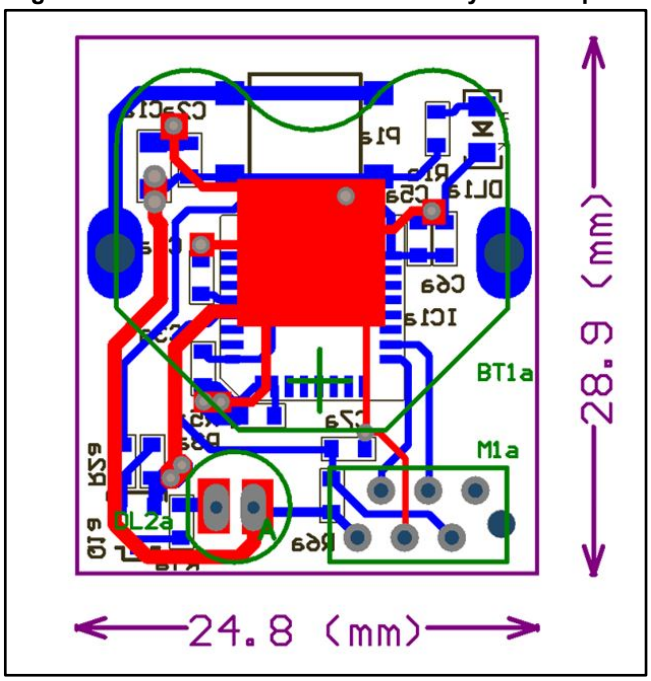


Figure 40: IR TX remote control board layout: top layer + top overlay

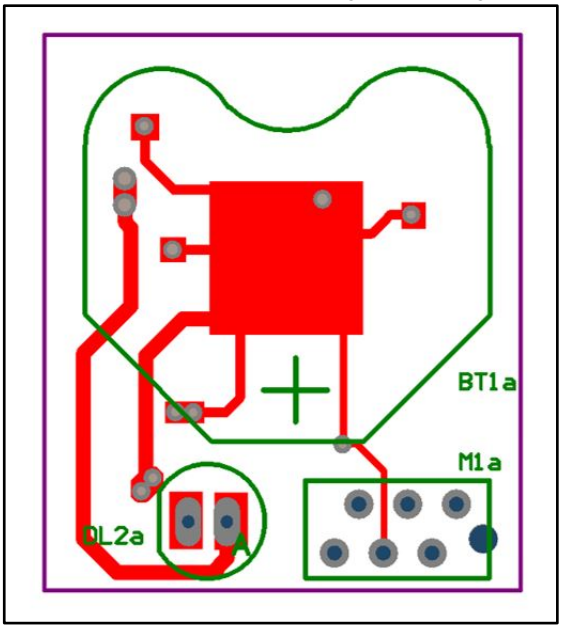
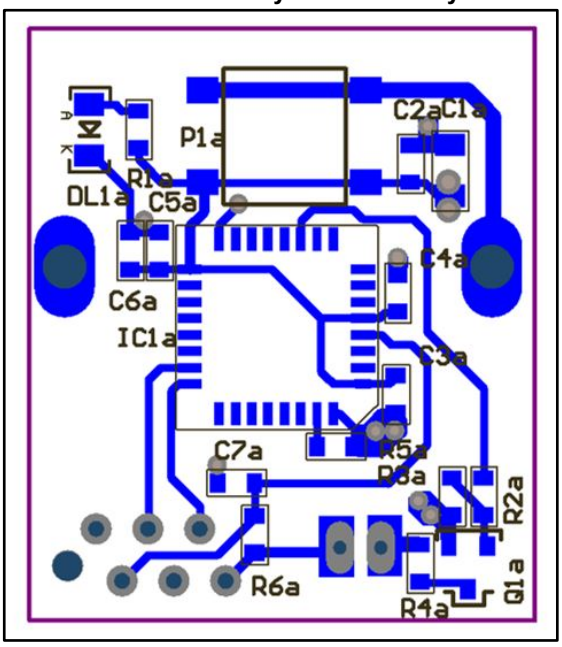


Figure 41: IR TX remote control board layout: bottom layer + mirrored top overlay



10 Conclusions

A 7.2 W single output remote controlled SMPS in flyback topology especially designed for air conditioning market using the VIPer0P has been described and characterized.

The key features are the possibility to be turned on/off by an IR remote controller, high conversion efficiency in the on state, extremely low power consumption in the zero power mode condition and excellent EMI/EMC performance using low cost input filter and passive component on VIPer0P- and STM32-sensitive pins.

All these features are realized by developing a small size PCB with a minimal bill of materials.

11 References

1. VIPer0P datasheet
2. Application note: Double outputs not isolated Flyback based on VIPer0P
3. Book: Microelectronics circuits. Authors: Adel S. Sedra, Kenneth C. Smith
4. Book: Basic circuit theory. Authors: Desoer Charles A., Kuh Ernest S.

12 Revision history

Table 13: Document revision history

Date	Version	Changes
25-Nov-2016	1	Initial release

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