



**RAYSTAR**

# 曜凌光電股份有限公司

住址: 42878 台中市大雅区科雅路 25 號 5F WEB: <http://www.Raystar-Optronics.com>  
5F., No.25, Keya Rd., Daya Dist., Taichung E-mail: sales@raystar-optronics.com  
City 428, Taiwan Tel:886-4-2565-0761 Fax :  
886-4-2565-0760

## RFC570B-EIW-DAN

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### SPECIFICATION

CUSTOMER:

APPROVED BY	
PCB VERSION	
DATE	

FOR CUSTOMER USE ONLY

SALES BY	APPROVED BY	CHECKED BY	PREPARED BY

ISSUED DATE:

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## 1. Revision History

DATE	VERSION	REVISED PAGE NO.	Note
2013/2/5	1		First issue

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## 2. General Specification

- Resolution: 320 x RGBx240
- Module dimension: 149.0 x 109.0 x 11.5 mm
- Active Area : 115.2 X 86.4 mm
- Dot pitch: 0.12 x 0.36 mm
- LCD type: TFT LCD Transmissive,
- View direction: 12 o'clock
- Gray Scale Inversion Direction: 6 o'clock
- Backlight Type: LED, Normally White
- Driver IC: SSD1963
- Interface: Digital 8080 family MPU

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### 3. Module Coding System

<b>R</b>	<b>F</b>	<b>C</b>	<b>57</b>	<b>0B</b>	<b>-</b>	<b>E</b>	<b>I</b>	<b>W</b>	<b>-</b>	<b>D</b>	<b>A</b>	<b>N</b>
1	2	3	4	5	-	6	7	8	-	9	10	11

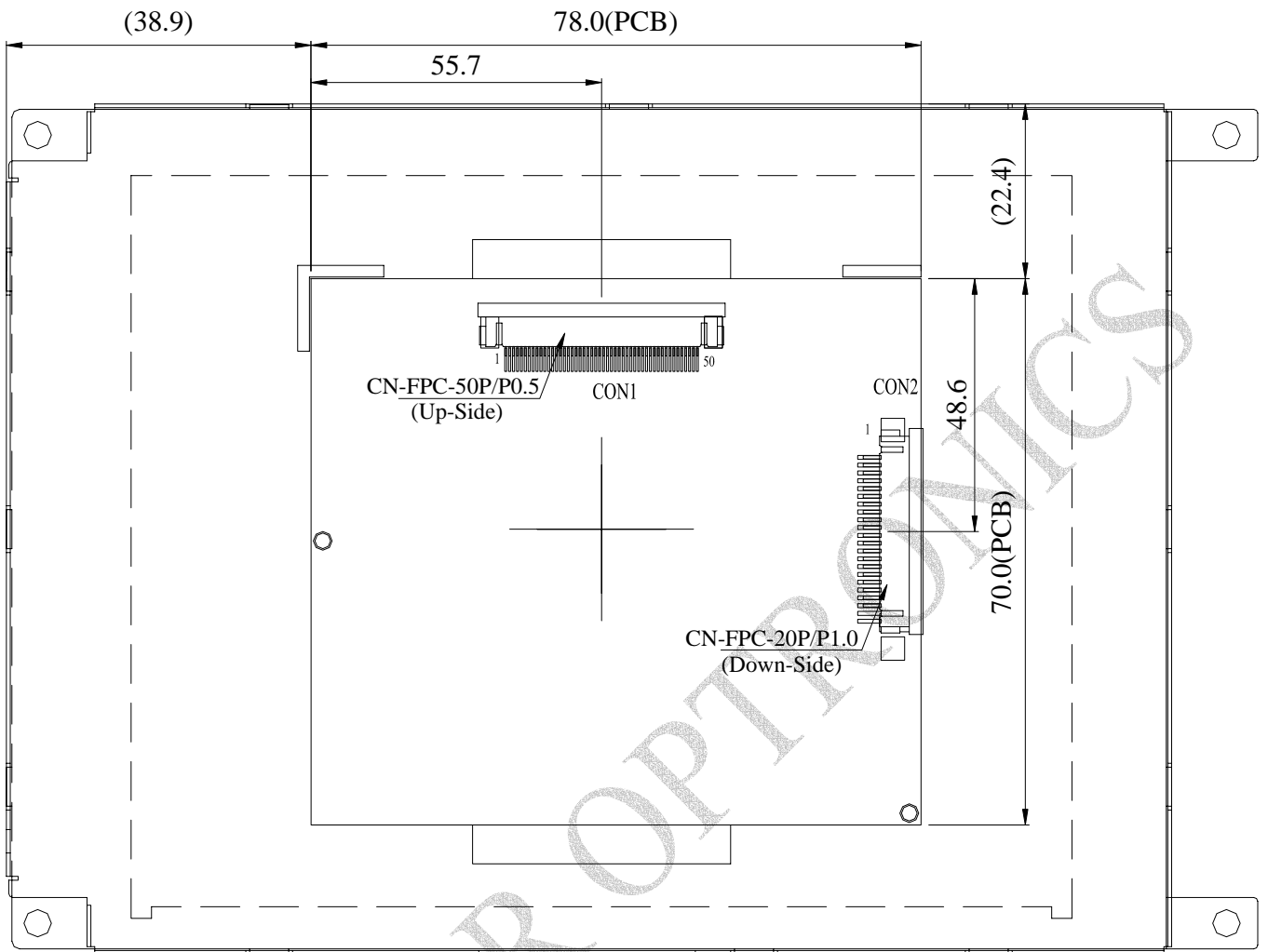
Item	Description		
1	R : Raystar Optronics Inc.		
2	Display Type : TFT Type		
3	Solution: A: 128x160 B:320x234 <b>C:320x240</b> D:480x234 G:640x480		
4	Display Size : 5.7" TFT		
5	Version Code.		
6	Model serials no.		
7	Polarizer Type, Temperature range, View direction	A : Reflective, N.T, 6:00	K : Transflective, W.T,12:00
		D : Reflective, N.T, 12:00	1 : Transflective, U.T,6:00
		G : Reflective, W. T, 6:00	4 : Transflective, U.T.12:00
		J : Reflective, W. T, 12:00	C : Transmissive, N.T,6:00
		0 : Reflective, U. T, 6:00	F : Transmissive, N.T,12:00
		3 : Reflective, U. T, 12:00	<b>I : Transmissive, W. T, 6:00</b>
		B : Transflective, N.T,6:00	L : Transmissive, W.T,12:00
		E : Transflective, N.T.12:00	2 : Transmissive, U. T, 6:00
		H : Transflective, W.T,6:00	5 : Transmissive, U.T,12:00
8	Backlight	N : Without backlight	Y : LED, Yellow Green
		P : EL, Blue green	A : LED, Amber
		T : EL, Green	<b>W : LED, White</b>
		D : EL, White	O : LED, Orange
		F : CCFL, White	G : LED, Green
9	Driver Method	<b>D: Digital</b> A: Analog	
10	Interface	N : without control board <b>A : 8Bit</b> B : 16Bit	
11	TS	<b>N : Without TS</b> S : resistive touch panel C : capacitive touch panel	

## 4. Interface Pin Function

### 4-1 Pins Connection To Control Board

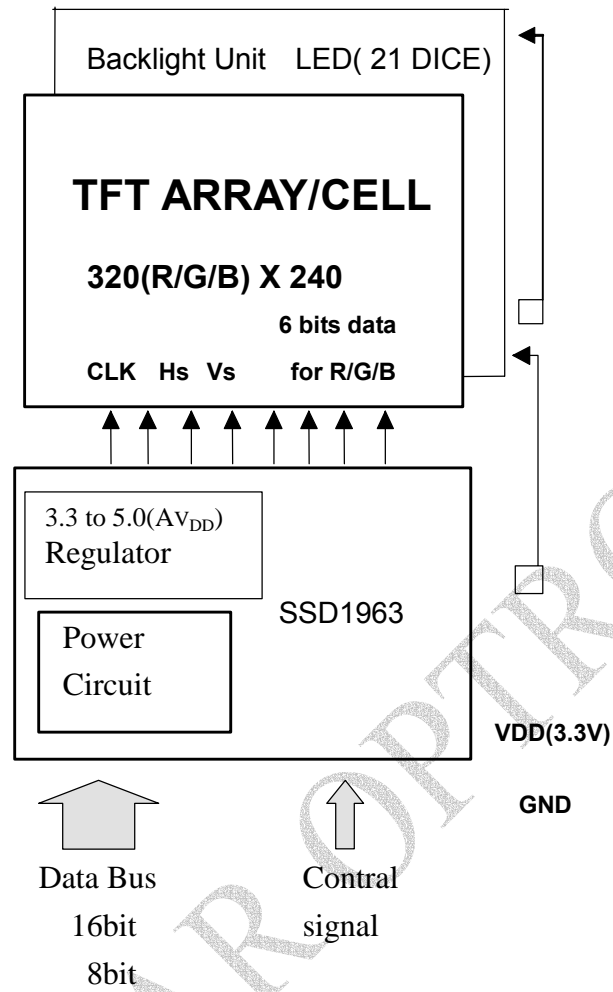
P/N	Symbol	8 B IT Function
1	GND	Ground
2	VCC	Power supply for Logic
3	NC	No connection
4	RS	Command/Data select(L: Command, H: Data)
5	WR	8080 family MPU interface : Write signal
6	RD	8080 family MPU interface: Read signal
7	DB0	Data bus
8	DB1	
9	DB2	
10	DB3	
11	DB4	
12	DB5	
13	DB6	
14	DB7	
15	CS	Chip select
16	RES	RESET
17	NC	No connection
18	RL	Scan direction
19	UD	Scan direction
20	NC	No connection







## 6. Block Diagram



## 7. Electrical Characteristics

Item	Symbol	Condition	Min	Typ	Max	Unit
Supply Voltage For Logic	VDD	V <sub>DD</sub> -GND	3.0	3.3	3.5	V
Input High Volt.	V <sub>IH</sub>	H Level	0.7 VDD	—	VDD	V
Input Low Volt.	V <sub>IL</sub>	L Level	0	—	0.3 VDD	V
Supply Current	I <sub>VDD</sub>	V <sub>DD</sub> =3.3V	—	121	—	mA

## 8. Electrical Absolute Ratings

Item	Symbol	Min	Typ	Max	Unit
Power Supply For Logic	V <sub>DD</sub> (digital-GND)	-0.3	—	3.5	V
Power Supply For Analog	AVDD (analog-GND)	-0.3	—	5.5	V
Input Voltage	V <sub>I</sub>	-0.3	—	VDD	V

## 9. DC Characteristics

**Conditions:**

Voltage referenced to VSS

VDDD, VDDPLL = 1.2V

VDDIO, VDDLCD = 3.3V

TA = 25°C

**DC Characteristics**

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
PSTY	Quiescent Power			300	500	uW
IIZ	Input leakage current		-1		1	uA
IOZ	Output leakage current		-1		1	uA
VOH	Output high voltage		0.7VDDIO			V
VOL	Output low voltage				0.3VDDIO	V
VIH	Input high voltage		0.7VDDIO		VDDIO+0.2	V
VIL	Input low voltage				0.3VDDIO	V

## 10. AC Characteristics

### Conditions:

Voltage referenced to VSS

VDDD, VDDPLL = 1.2V

VDDIO, VDDLCD = 3.3V

TA = 25°C

CL = 50pF (Bus/CPU Interface)

CL = 0pF (LCD Panel Interface)

### 10.1 Clock Timing

**Table 10-1: Clock Input Requirements for CLK (PLL-bypass)**

Symbol	Parameter	Min	Max	Units
FCLK	Input Clock Frequency (CLK)		110	MHz
TCLK	Input Clock period (CLK)	1/fCLK		ns

**Table 10-2: Clock Input Requirements for CLK**

Symbol	Parameter	Min	Max	Units
FCLK	Input Clock Frequency (CLK)	2.5	50	MHz
TCLK	Input Clock period (CLK)	1/fCLK		ns

**Table 10-3: Clock Input Requirements for crystal oscillator XTAL**

Symbol	Parameter	Min	Max	Units
FXTAL	Input Clock Frequency	2.5	10	MHz
TXTAL	Input Clock period	1/fXTAL		ns

## 10.2 MCU Interface Timing

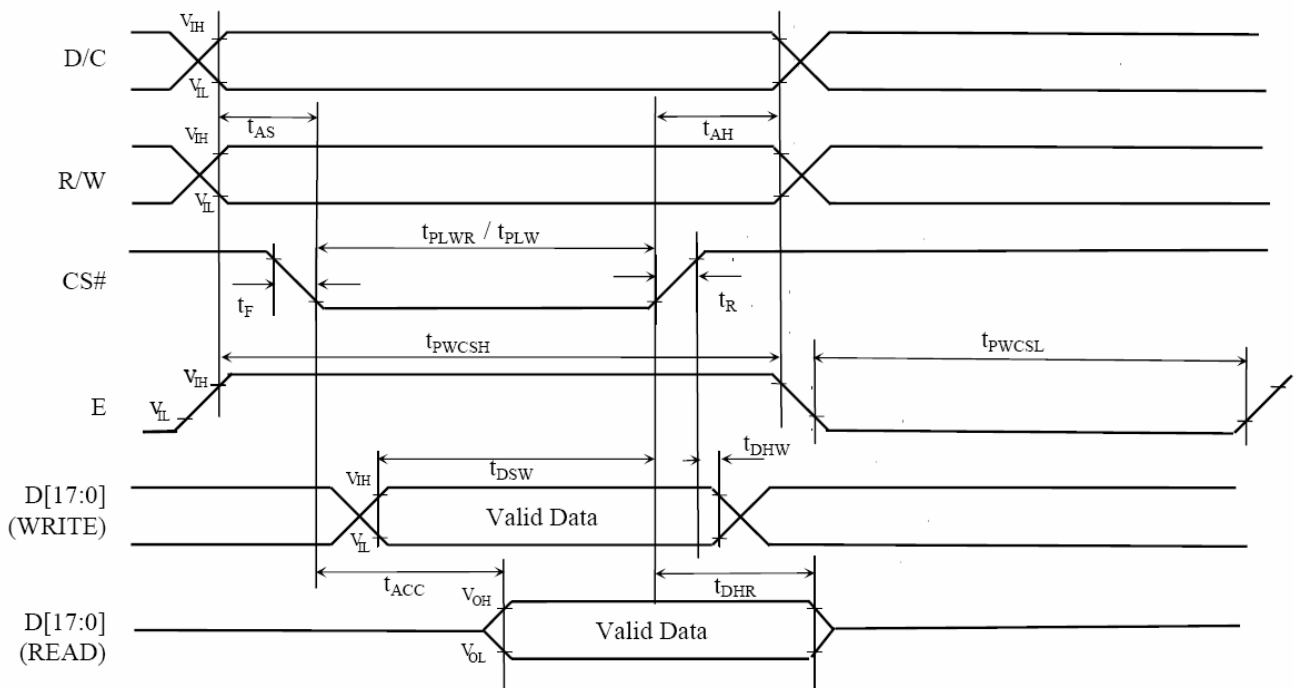
### 10.2.1 Parallel 6800-series Interface Timing

**Table 10-4: Parallel 6800-series Interface Timing Characteristics (Use CS# as clock)**

Symbol	Parameter	Min	Typ	Max	Unit
fMCLK	System Clock Frequency*	1	-	110	MHz
tMCLK	System Clock Period*	1/fMCLK	-	-	ns
tPWCSH	Control Pulse High Width	Write	13	1.5* tMCLK	ns
		Read	30	3.5* tMCLK	
tPWCSL	Control Pulse Low Width	Write (next write cycle)	13	1.5* tMCLK	ns
		Write (next read cycle)	80	9* tMCLK	
		Read	80	9* tMCLK	
tAS	Address Setup Time	2	-	-	ns
tAH	Address Hold Time	2	-	-	ns
tDSW	Data Setup Time	4	-	-	ns
tDHW	Data Hold Time	1	-	-	ns
tPLW	Write Low Time	14	-	-	ns
tPHW	Write High Time	14	-	-	ns
tPLWR	Read Low Time	38	-	-	ns
tACC	Data Access Time	32	-	-	ns
tDHR	Output Hold time	1	-	-	ns
tR	Rise Time	-	-	0.5	ns
tF	Fall Time	-	-	0.5	ns

\* System Clock denotes external input clock (PLL-bypass) or internal generated clock (PLL-enabled)

**Figure 10-1: Parallel 6800-series Interface Timing Diagram (Use CS# as Clock)**

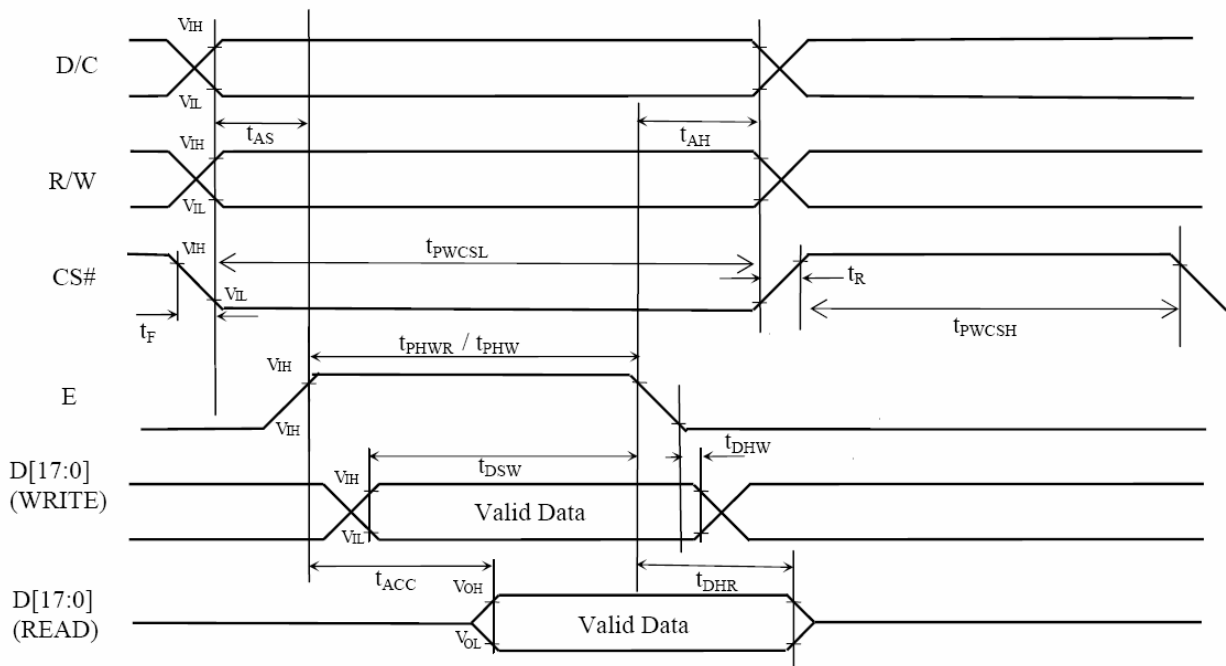


**Table 10-5: Parallel 6800-series Interface Timing Characteristics (Use E as clock)**

Symbol	Parameter	Min	Typ	Max	Unit	
fMCLK	System Clock Frequency*	1	-	110	MHz	
tMCLK	System Clock Period*	1/ fMCLK	-	-	ns	
tPWCSH	Control Pulse Low Width	Write (next write cycle)	13	1.5* tMCLK	-	ns
		Write (next read cycle)	80	9* tMCLK		
		Read	80	9* tMCLK		
tPWCSL	Control Pulse High Width	Write	13	1.5* tMCLK	-	ns
		Read	30	3.5* tMCLK		
tAS	Address Setup Time	2	-	-	ns	
tAH	Address Hold Time	2	-	-	ns	
tDSW	Data Setup Time	4	-	-	ns	
tDHW	Data Hold Time	1	-	-	ns	
tPLW	Write Low Time	14	-	-	ns	
tPHW	Write High Time	14	-	-	ns	
tPLWR	Read Low Time	38	-	-	ns	
tACC	Data Access Time	32	-	-	ns	
tDHR	Output Hold time	1	-	-	ns	
tR	Rise Time	-	-	0.5	ns	
tF	Fall Time	-	-	0.5	ns	

\* System Clock denotes external input clock (PLL-bypass) or internal generated clock (PLL-enabled)

**Figure10-2: Parallel 6800-series Interface Timing Diagram (Use E as Clock)**



### 10.2.2 Parallel 8080-series Interface Timing

**Table 10-6: Parallel 8080-series Interface**

Symbol	Parameter	Min	Typ	Max	Unit
fMCLK	System Clock Frequency*	1	-	110	MHz
tMCLK	System Clock Period*	1/ fMCLK	-	-	ns
tPWCSL	Control Pulse High Width	13	1.5* tMCLK	-	ns
tPWCSH	Control Pulse Low Width	30	3.5* tMCLK	-	ns
tAS	Address Setup Time	1	-	-	ns
tAH	Address Hold Time	2	-	-	ns
tDSW	Write Data Setup Time	4	-	-	ns
tDHW	Write Data Hold Time	1	-	-	ns
tPWLW	Write Low Time	12	-	-	ns
tDHR	Read Data Hold Time	1	-	-	ns
tACC	Access Time	32	-	-	ns
tPWLR	Read Low Time	36	-	-	ns
tR	Rise Time	-	-	0.5	ns
tF	Fall Time	-	-	0.5	ns
tCS	Chip select setup time	2	-	-	ns
tCSH	Chip select hold time to read signal	3	-	-	ns

\* System Clock denotes external input clock (PLL-bypass) or internal generated clock (PLL-enabled)

**Figure 10-3: Parallel 8080-series Interface Timing Diagram (Write Cycle)**

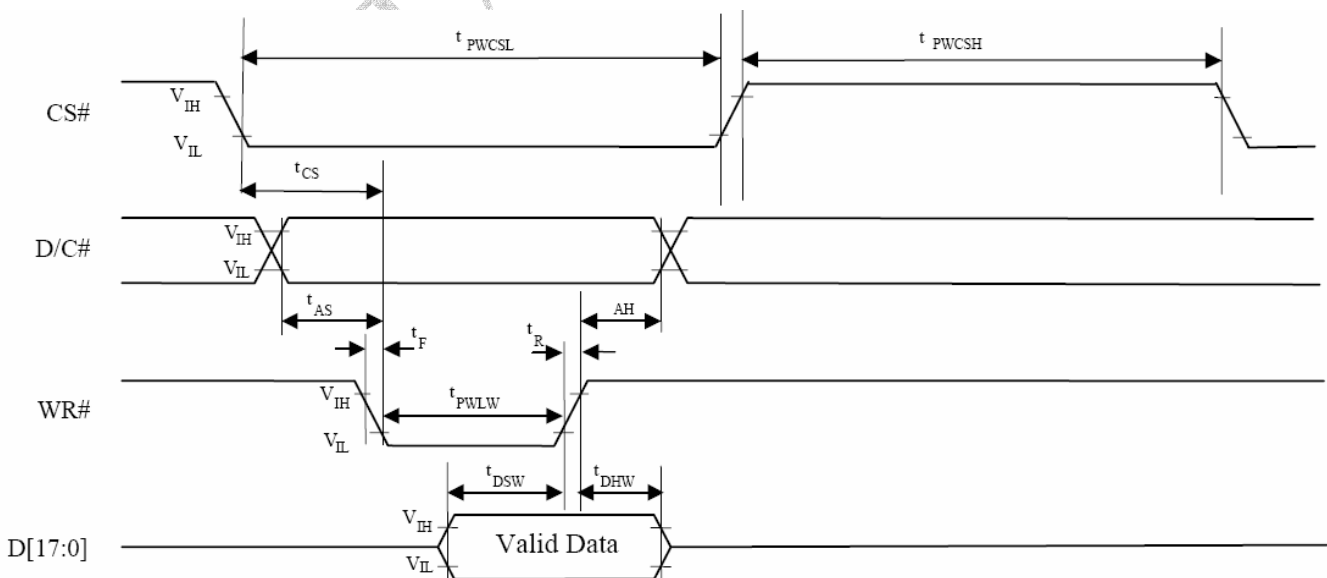
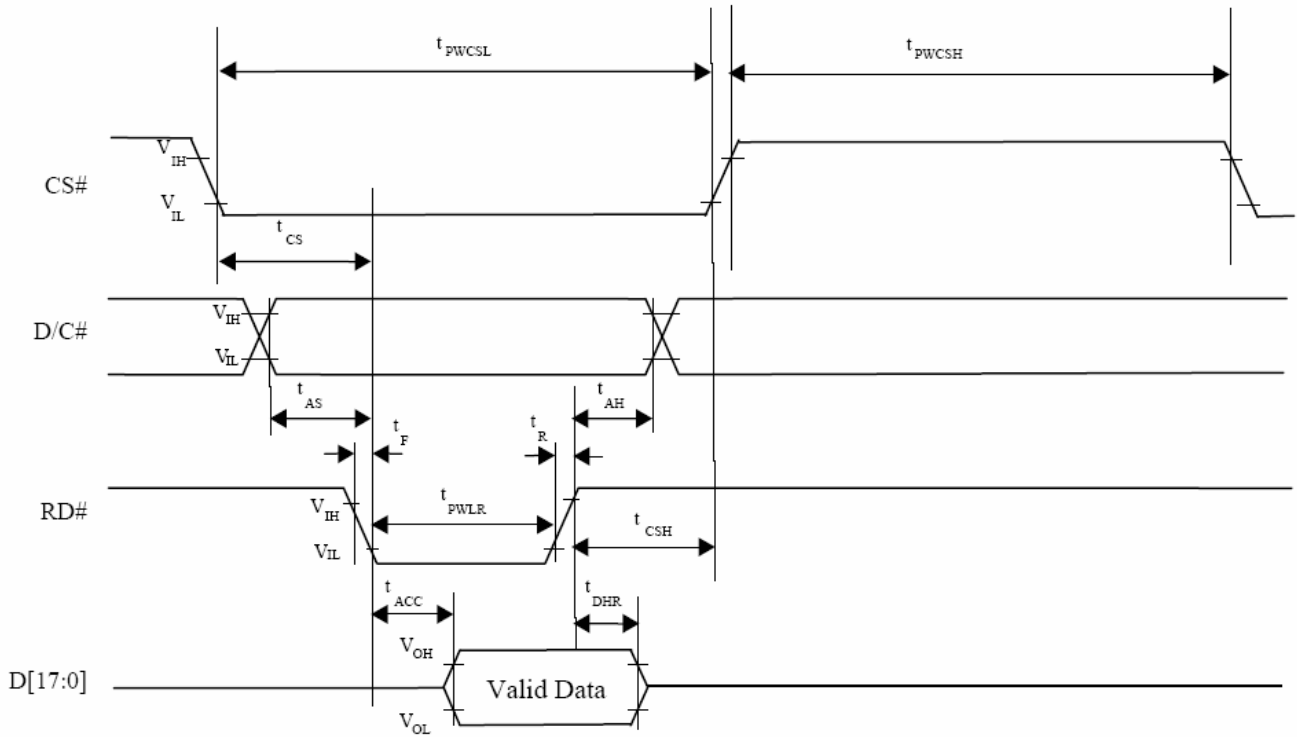


Figure 10-4: Parallel 8080-series Interface Timing Diagram (Read Cycle)



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# 11. Data transfer order Setting

## Pixel Data Format

Both 6800 and 8080 support 8-bit, 9-bit, 16-bit, 18-bit and 24-bit data bus. Depending on the width of the data bus, the display data are packed into the data bus in different ways.

Table 11-1: Pixel Data Format

Interface	Cycle	D[23]	D[22]	D[21]	D[20]	D[19]	D[18]	D[17]	D[16]	D[15]	D[14]	D[13]	D[12]	D[11]	D[10]	D[9]	D[8]	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]
24 bits	1st	R7	R6	R5	R4	R3	R2	R1	R0	G7	G6	G5	G4	G3	G2	G1	G0	B7	B6	B5	B4	B3	B2	B1	B0
18 bits	1st							R5	R4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B5	B4	B3	B2	B1	B0
16 bits (565 format)	1st									R5	R4	R3	R2	R1	G5	G4	G3	G2	G1	G0	B5	B4	B3	B2	B1
	1st									R7	R6	R5	R4	R3	R2	R1	R0	G7	G6	G5	G4	G3	G2	G1	G0
16 bits	2nd									B7	B6	B5	B4	B3	B2	B1	B0	R7	R6	R5	R4	R3	R2	R1	R0
	3rd									G7	G6	G5	G4	G3	G2	G1	G0	B7	B6	B5	B4	B3	B2	B1	B0
12 bits	1st													R7	R6	R5	R4	R3	R2	R1	R0	G7	G6	G5	G4
	2nd												G3	G2	G1	G0	B7	B6	B5	B4	B3	B2	B1	B0	
9 bits	1st																R5	R4	R3	R2	R1	R0	G5	G4	G3
	2nd															G2	G1	G0	B5	B4	B3	B2	B1	B0	
8 bits	1st																	R7	R6	R5	R4	R3	R2	R1	R0
	2nd																	G7	G6	G5	G4	G3	G2	G1	G0
	3rd																	B7	B6	B5	B4	B3	B2	B1	B0

# 12. Register Depiction

Please consult the spec of SSD1963 Version 1.2

## 13. OPTICAL CHARACTERISTIC

### 13-1 Optical Char. of LCD Panel

Parameter	Symbol	Values			Unit	Note
		Min.	Typ.	Max.		
Response Time	Tr+Tf	—	50	—	ms	Note 2,3
Contrast Ratio	C/R	—	250	—	—	*A)
$\theta$ (View Angle)	CR=10	12 O'Clock	—	40	—	Note 3,5
		6 O'Clock	—	60	—	
$\phi$ (View Angle)		9 O'Clock	—	60	—	
		3 O'Clock	—	60	—	
$\theta$ (View Angle)	CR=5	12 O'Clock	—	60	—	
		6 O'Clock	—	70	—	
$\phi$ (View Angle)		9 O'Clock	—	70	—	
		3 O'Clock	—	70	—	
Degree of Saturation	NTSC	—	50	—	%	

\*A) Contrast Ratio (CR) is define mathematically as :

$$\text{Contrast Ratio} = \frac{\text{Surface Luminance with all white pixels}}{\text{Surface Luminance with all balck pixels}}$$

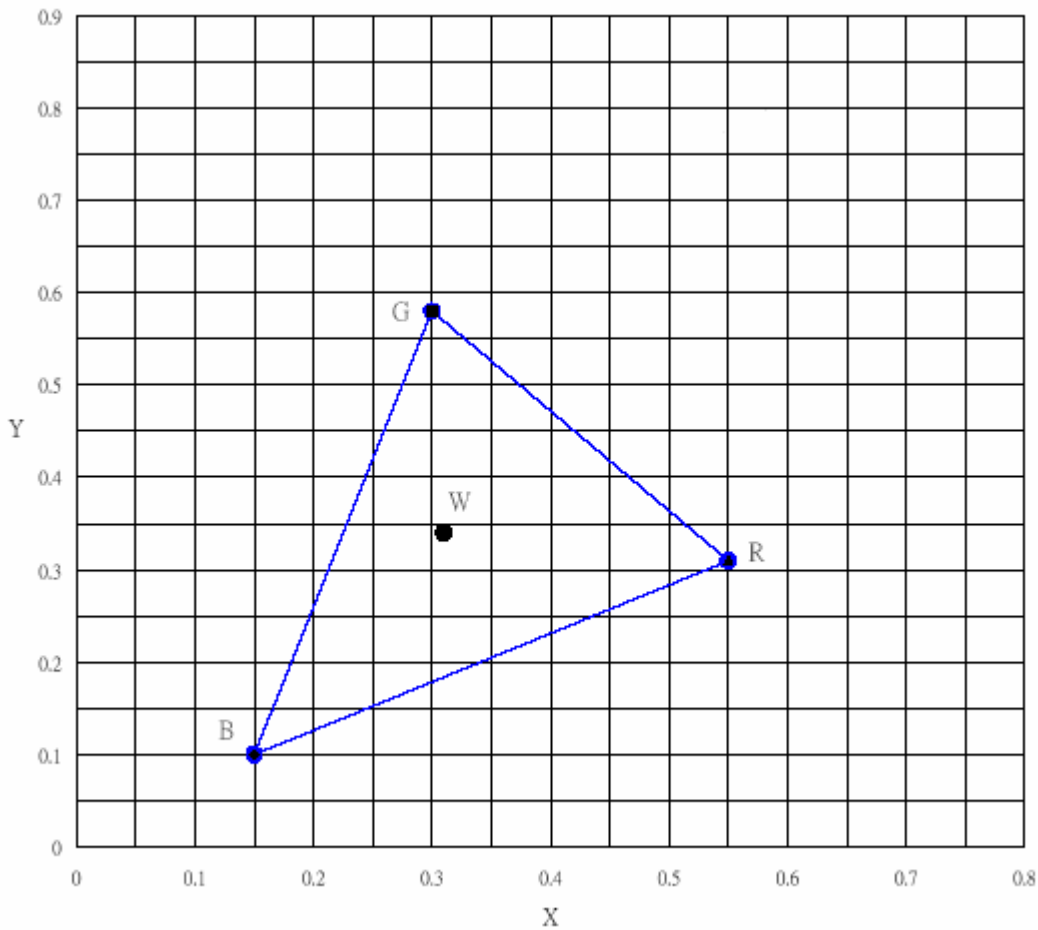
13-2 Color of CIE Coordinate

ITEM		SYMBOL	CONDITION	VALUE			NOTE
				MIN.	TYP.	MAX.	
Color of CIE Coordinate	Red	x	$\varphi=0^\circ, \theta=0^\circ$	0.5	0.55	0.6	Note※
		y		0.26	0.31	0.36	
	Green	x	$\varphi=0^\circ, \theta=0^\circ$	0.25	0.3	0.35	
		y		0.53	0.58	0.63	
	Blue	x	$\varphi=0^\circ, \theta=0^\circ$	0.1	0.15	0.2	
		y		0.05	0.1	0.15	
	White	x	$\varphi=0^\circ, \theta=0^\circ$	0.26	0.31	0.36	
		y		0.29	0.34	0.39	

Note※ Measuring at position 3 on Fig.1 CIE chromaticity diagram.

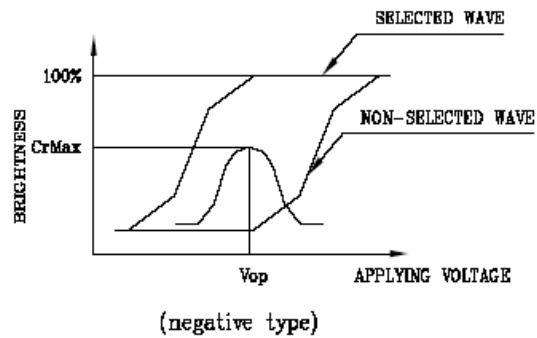
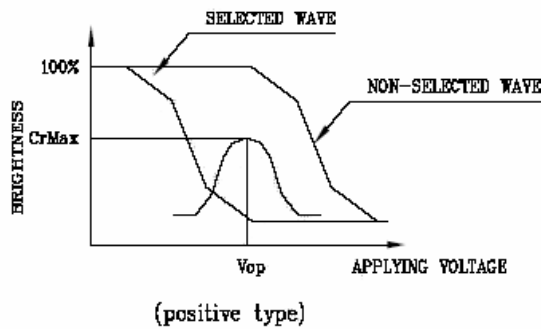
Base on Nan Ya Backlight (CIE X=0.29 ±0.02 , Y=0.29 ±0.02)

Fig.1



(NOTE 1)

Definition of Operation Voltage(Vop)

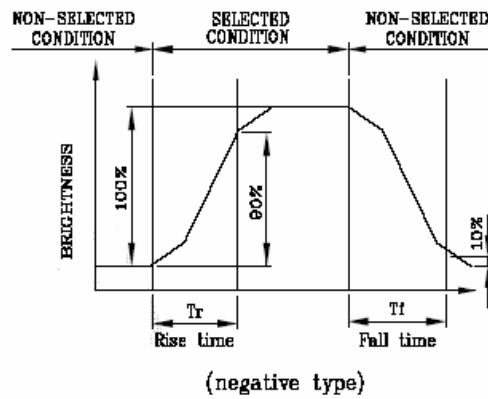
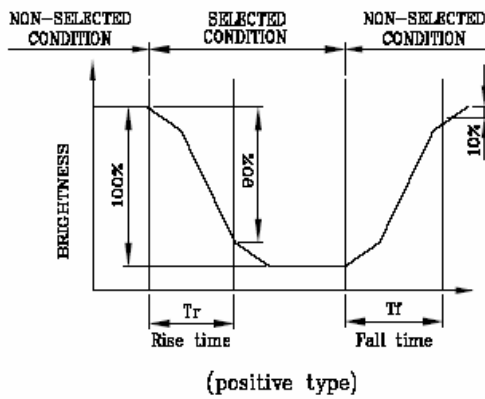


\*Conditions

Viewing Angle : 0  
 Frame Frequency : 70Hz  
 Applying Waveform : 1/N duty 1/a bias

(NOTE 2)

Definition of Response Time(Tr,Tf)

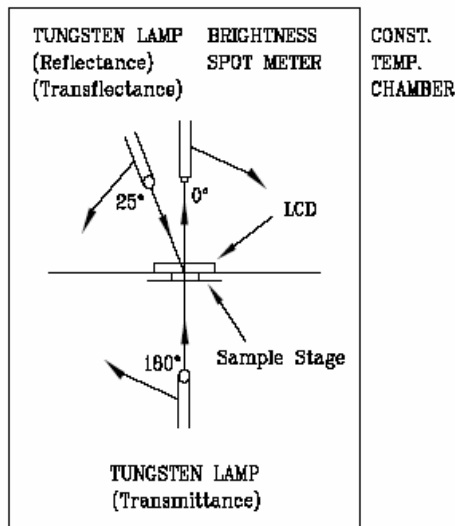


\*Conditions

Operating Voltage : Vop  
 Viewing Angle (θ,θ) : (0,0)  
 Frame Frequency : 70Hz  
 Applying Waveform : 1/N duty 1/a bias

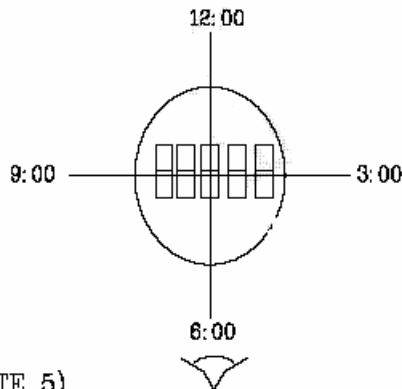
(NOTE 3)

Description of Measuring Equipment and Driving Waveforms



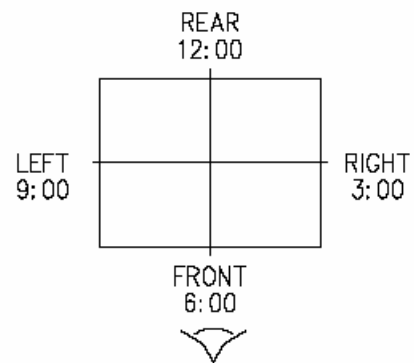
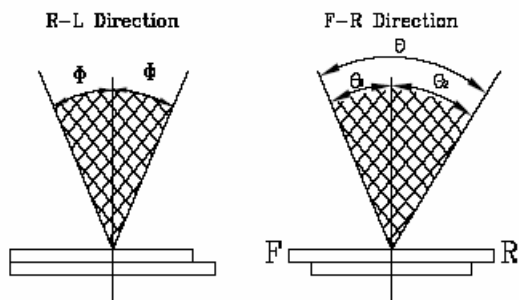
(NOTE 4)

Definition of Viewing Direction



(NOTE 5)

Definition of Viewing Angle



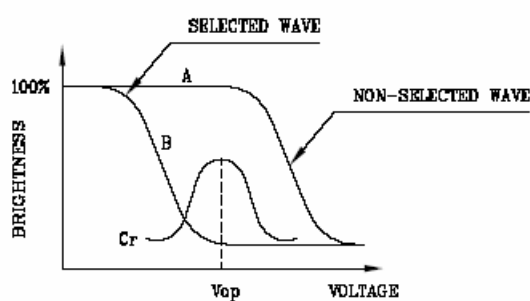
$$\Theta = \Theta_1 + \Theta_2$$

\*Conditions

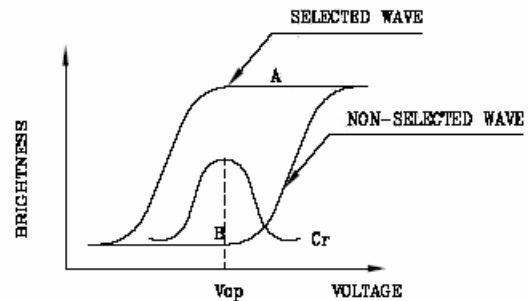
- Operating Voltage :  $V_{op}$
- Frame Frequency : 70Hz
- Applying Waveform : 1/N duty 1/a bias
- Contrast Ratio : larger than 2

(NOTE 6)

Definition of Contrast Ratio (Cr)



(positive type)



(negative type)

$$\text{Contrast Ratio : } Cr = A/B$$

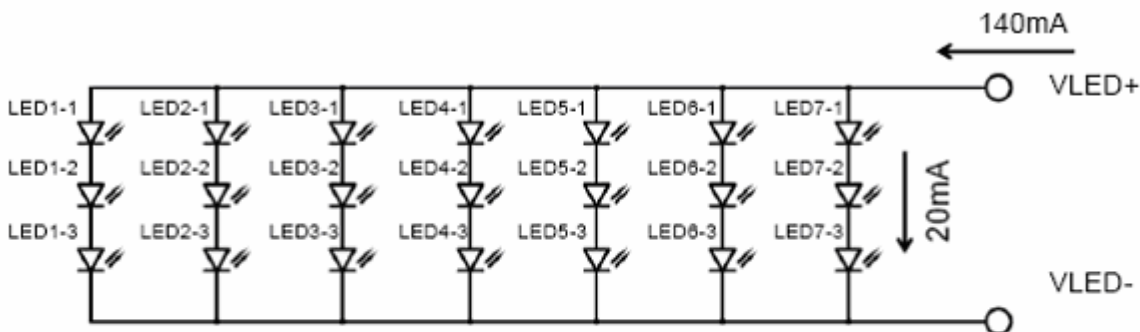
\*Conditions

- Viewing Angle : 0
- Frame Frequency : 70Hz

## 14. LED driving conditions

Parameter	Symbol	Min.	Typ.	Max.	Unit	Remark
LED Current	$I_{LED}$	----	140	----	mA	Note1
LED voltage	$V_{LED}$	9.0	----	10.5	V	Note6
LED life Time	-	----	50K	----	-	Note 2,3.5
Luminous Intensity	IV	300	----	----	CD/M <sup>2</sup>	Note 4

Note 1: There are 7 Groups LED shown as below, =9.9 V(Min)



Note 2 :  $T_a = 25^{\circ}C$  ,

Note 3 : Brightness to be decreased to 50% of the initial value.

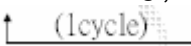
Note 4: The luminous is measured through LCD panel.

Note5: 50K hours is only an estimate for reference.

Note6: The LED of B/L is drive by current only ; driving voltage is only for reference .

## 15. Reliability Test

### WIDE TEMPERATURE RELIABILITY TEST

NO	ITEM	CONDITION			STANDARD	NOTE
1	High Temp. Storage	80°C	240 Hrs		Appearance without defect	
2	Low Temp. Storage	-30°C	240 Hrs		Appearance without defect	
3	High Temp. & High Humi. Storage	60 °C 90%RH	240 Hrs		Appearance without defect	
4	High Temp. Operating Display	70°C	240 Hrs		Appearance without defect	
5	Low Temp. Operating Display	-20°C	240 Hrs		Appearance without defect	
6	Thermal Shock	-20 °C, 30min. → 70°C, 30min. <div style="text-align: center;">   (1cycle)         </div>			Appearance without defect	10 cycles

# Inspection Provision

## 1. Purpose

The RAYSTAR inspection provision provides outgoing inspection provision and its expected quality level based on our outgoing inspection of RAYSTAR LCD produces.

## 2. Applicable Scope

The RAYSTAR inspection provision is applicable to the arrangement in regard to outgoing inspection and quality assurance after outgoing.

## 3. Technical Terms

### 3-1 RAYSTAR Technical Terms



## 4. Outgoing Inspection

### 4-1 Inspection Method

MIL-STD-105E Level II Regular inspection

### 4-2 Inspection Standard

	Item	AQL(%)	Remarks
Major Defect	Dots	0.4	Faults which substantially lower the practicality and the initial purpose difficult to achieve
	Solder appearance		
	Cracks		

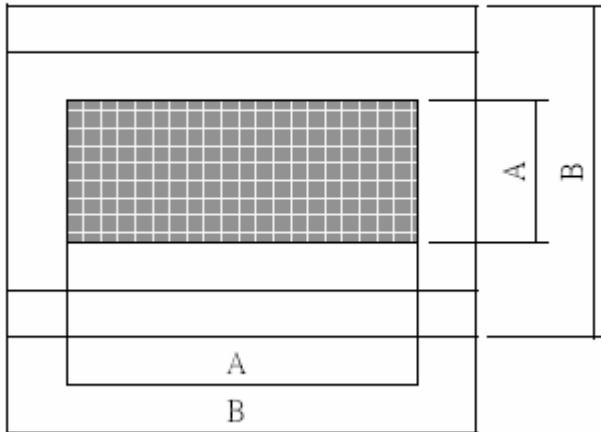
	Dimensions	External from Dimensions	AQL	Remarks
Minor Defect	Inside the glass	Black spots	0.65	Faults which appear to pose almost no obstacle to the practicality, effective use, and operation
	Polarizing plate	Scratches, foreign Matter, air bubbles, and peeling		
	Dots	Pinhole, deformation		
	Color tone	Color unevenness		
	Solder appearance	Cold solder Solder projections		



4-3 Inspection Provisions

\*Viewing Area Definition

Fig. 1



A : Zone Viewing Area  
 B : Zone Glass Plate Outline

\*Inspection place to be 500 to 1000 lux illuminance uniformly without glaring.  
 The distance between luminous source(daylight fluorescent lamp and cool white fluorescent lamp)  
 and sample to be 30 cm to 50 cm.

\*Test and measurement are performed under the following conditions, unless otherwise specified.

Temperature  $20 \pm 15^{\circ}\text{C}$   
 Humidity  $65 \pm 20\% \text{R.H.}$   
 Pressure 860~1060hPa(mmbar)

In case of doubtful judgment, it is performed under the following conditions.

Temperature  $20 \pm 2^{\circ}\text{C}$   
 Humidity  $65 \pm 5\% \text{R.H.}$   
 Pressure 860~1060hPa(mmbar)

5.Specification for quality check

5-1-1 Electrical characteristics :

NO.	Item	Criterion
1	Non operational	Fail
2	Miss operating	Fail
3	Contrast irregular	Fail
4	Response time	Within Specified value

5-1-2 Components soldering :

Should be no defective soldering such as shorting, loose terminal cold solder, peeling of printed circuit board pattern, improper mounting position, etc.

5-2 Inspection Standard for TFT panel

5-2-1 The environmental condition of inspection :

The environmental condition and visual inspection shall be conducted as below.

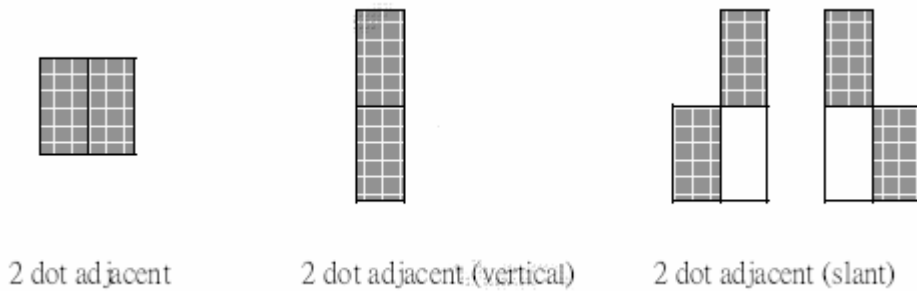
- (1) Ambient temperature :  $25\pm 5^{\circ}\text{C}$
- (2) Humidity : 25~75% RH
- (3) External appearance inspection shall be conducted by using a single 20W fluorescent lamp or equivalent illumination.
- (4) Visual inspection on the operation condition for cosmetic shall be conducted at the distance 30cm or more between the LCD panels and eyes of inspector. The viewing angle shall be 90 degree to the front surface of display panel.
- (5) Ambient Illumination : 300~500 Lux for external appearance inspection.
- (6) Ambient Illumination : 100~200 Lux for light on inspection.

5-2-2 Inspection Criteria

(1) Definition of dot defect induced from the panel inside

- a) The definition of dot : The size of a defective dot over 1/2 of whole dot is regarded as one defective dot
- b) Bright dot : Dots appear bright and unchanged in size in which LCD panel is displaying under black pattern.
- c) Dark dot : Dots appear dark and unchanged in size in which LCD panel is displaying under pure red, green, blue pattern.
- d) 2 dot adjacent = 1 pair = 2 dots

Picture :

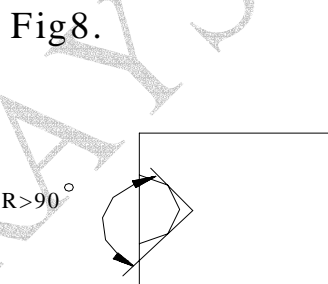
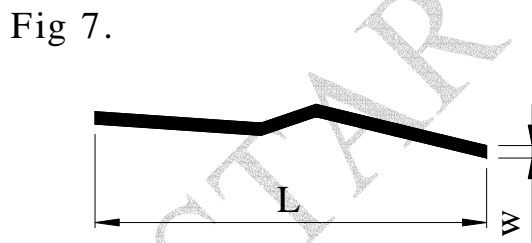
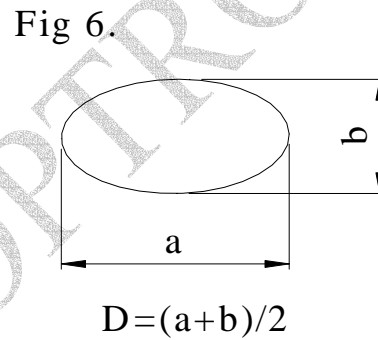
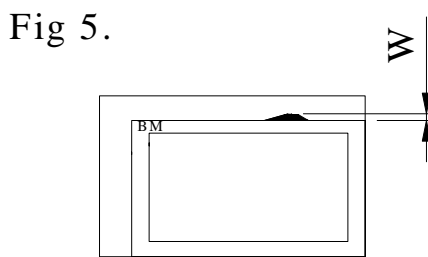
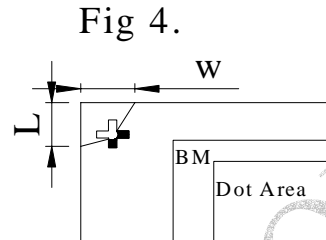
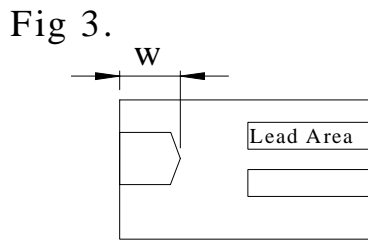
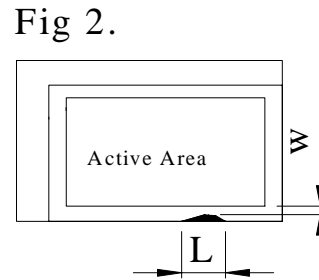
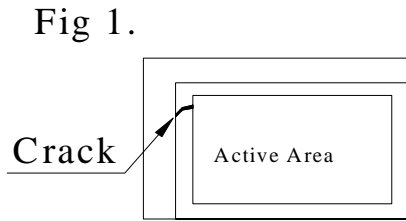


(2) Display Inspection

NO.	Item		Acceptable Count	
1	Dot defect	Bright Dot	Random	$N \leq 2$
			2 dots adjacent	$N \leq 0$
		Dark Dot	Random	$N \leq 3$
			2 dots adjacent	$N \leq 1$
	Total bright and dark dot			$N \leq 4$
Functional failure (V-line/ H-line/Cross line etc.)			Not allowable	
	Mura	It's OK if mura is slight visible through 6% ND filter. (Judged by limit sample if it is necessary)		
2	Newton ring (touch panel)	Orbicular of interference fringes is not allowed in the optimum contrast within the active area under viewing angle.		

(3) Appearance inspection

NO.	Item	Standards
1	Panel Crack	Not allow. It is shown in Fig.1.
2	Broken CF Non -lead Side of TFT	The broken in the area of $W > 2\text{mm}$ is ignored, L is ignored. It is shown in Fig.2.
3	Broken Lead Side of TFT	FPC lead, electrical line or alignment mark can't be damaged. It is shown in Fig.3.
4	Broken Corner of TFT at Lead Side	FPC lead. electrical line or alignment mark can't be damaged. It is shown in Fig.4.
5	Burr of TFT / CF Edge	The distance of burr from the edge of TFT / CF, $W \leq 0.3\text{mm}$ . It is shown in Fig.5.
6	Foreign Black / White/Bright Spot	(1) $0.15 < D \leq 0.5 \text{ mm}$ , $N \leq 4$ ; (2) $D \leq 0.15\text{mm}$ , Ignore. It is shown in Fig.6.
7	Foreign Black / White/Bright Line	(1) $0.05 < W \leq 0.1 \text{ mm}$ , $0.3 < L \leq 2 \text{ mm}$ , $N \leq 4$ .
		(2) $W \leq 0.05\text{mm}$ and $L \leq 0.3\text{mm}$ Ignore. It is shown in Fig.7.
8	Color irregular	Not remarkable color irregular.



Notes

1.W:Width

2.Length

3.D:Average Diameter

4.N:Count

5.All the anhle of the broken must be larger than  $90^\circ$ ~.It is shown in Fig.8.( $R > 90^\circ$ ~)

NOTICE:

- SAFETY

1. If the LCD panel breaks, be careful not to get the liquid crystal to touch your skin.
2. If the liquid crystal touches your skin or clothes, please wash it off immediately by using soap and water.

- HANDLING

1. Avoid static electricity which can damage the CMOS LSI.
2. Do not remove the panel or frame from the module.
3. The polarizing plate of the display is very fragile. So, please handle it very carefully.
4. Do not wipe the polarizing plate with a dry cloth, as it may easily scratch the surface of plate.
5. Do not use ketonics solvent & Aromatic solvent. Use a soft cloth soaked with a cleaning naphtha solvent.

- STORAGE

1. Store the panel or module in a dark place where the temperature is  $25\pm 5^{\circ}\text{C}$  and the humidity is below 65% RH.
2. Do not place the module near organics solvents or corrosive gases.
3. Do not crush, shake, or jolt the module.

- TERMS OF WARRANT

1. Acceptance inspection period

The period is within one month after the arrival of contracted commodity at the buyer's factory site.

2. Applicable warrant period

The period is within twelve months since the date of shipping out under normal using and storage conditions.

**LCM Sample Estimate Feedback Sheet**

Module Number : \_\_\_\_\_

**1 、 Panel Specification :**

1. Panel Type :	<input type="checkbox"/> Pass	<input type="checkbox"/> NG , _____
2. View Direction :	<input type="checkbox"/> Pass	<input type="checkbox"/> NG , _____
3. Numbers of Dots :	<input type="checkbox"/> Pass	<input type="checkbox"/> NG , _____
4. View Area :	<input type="checkbox"/> Pass	<input type="checkbox"/> NG , _____
5. Active Area :	<input type="checkbox"/> Pass	<input type="checkbox"/> NG , _____
6. Operating Temperature :	<input type="checkbox"/> Pass	<input type="checkbox"/> NG , _____
7. Storage Temperature :	<input type="checkbox"/> Pass	<input type="checkbox"/> NG , _____
8. Others :	_____	

**2 、 Mechanical Specification :**

1. PCB Size :	<input type="checkbox"/> Pass	<input type="checkbox"/> NG , _____
2. Frame Size :	<input type="checkbox"/> Pass	<input type="checkbox"/> NG , _____
3. Material of Frame :	<input type="checkbox"/> Pass	<input type="checkbox"/> NG , _____
4. Connector Position :	<input type="checkbox"/> Pass	<input type="checkbox"/> NG , _____
5. Fix Hole Position :	<input type="checkbox"/> Pass	<input type="checkbox"/> NG , _____
6. Backlight Position :	<input type="checkbox"/> Pass	<input type="checkbox"/> NG , _____
7. Thickness of PCB :	<input type="checkbox"/> Pass	<input type="checkbox"/> NG , _____
8. Height of Frame to PCB :	<input type="checkbox"/> Pass	<input type="checkbox"/> NG , _____
9. Height of Module :	<input type="checkbox"/> Pass	<input type="checkbox"/> NG , _____
10. Others :	<input type="checkbox"/> Pass	<input type="checkbox"/> NG , _____

**3 、 Relative Hole Size :**

1. Pitch of Connector :	<input type="checkbox"/> Pass	<input type="checkbox"/> NG , _____
2. Hole size of Connector :	<input type="checkbox"/> Pass	<input type="checkbox"/> NG , _____
3. Mounting Hole size :	<input type="checkbox"/> Pass	<input type="checkbox"/> NG , _____
4. Mounting Hole Type :	<input type="checkbox"/> Pass	<input type="checkbox"/> NG , _____
5. Others :	<input type="checkbox"/> Pass	<input type="checkbox"/> NG , _____

**4 、 Backlight Specification :**

1. B/L Type :	<input type="checkbox"/> Pass	<input type="checkbox"/> NG , _____
2. B/L Color :	<input type="checkbox"/> Pass	<input type="checkbox"/> NG , _____
3. B/L Driving Voltage (Reference for LED Type) :	<input type="checkbox"/> Pass	<input type="checkbox"/> NG , _____
4. B/L Driving Current :	<input type="checkbox"/> Pass	<input type="checkbox"/> NG , _____
5. Brightness of B/L :	<input type="checkbox"/> Pass	<input type="checkbox"/> NG , _____
6. B/L Solder Method :	<input type="checkbox"/> Pass	<input type="checkbox"/> NG , _____
7. Others :	<input type="checkbox"/> Pass	<input type="checkbox"/> NG , _____

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<b>Module Number :</b> _____		
<b>5 、 <u>Electronic Characteristics of Module</u> :</b>		
1.Input Voltage :	<input type="checkbox"/> Pass	<input type="checkbox"/> NG , _____
2.Supply Current :	<input type="checkbox"/> Pass	<input type="checkbox"/> NG , _____
3.Driving Voltage for LCD :	<input type="checkbox"/> Pass	<input type="checkbox"/> NG , _____
4.Contrast for LCD :	<input type="checkbox"/> Pass	<input type="checkbox"/> NG , _____
5.B/L Driving Method :	<input type="checkbox"/> Pass	<input type="checkbox"/> NG , _____
6.Negative Voltage Output :	<input type="checkbox"/> Pass	<input type="checkbox"/> NG , _____
7.Interface Function :	<input type="checkbox"/> Pass	<input type="checkbox"/> NG , _____
8.LCD Uniformity :	<input type="checkbox"/> Pass	<input type="checkbox"/> NG , _____
9.ESD test :	<input type="checkbox"/> Pass	<input type="checkbox"/> NG , _____
10.Others :	<input type="checkbox"/> Pass	<input type="checkbox"/> NG , _____
<b>6 、 <u>Summary</u> :</b>		
<p style="text-align: right;">Sales signature : _____</p> <p style="text-align: right;">Customer Signature : _____      <b>Date :</b>    /    /</p>		