

**DISPLAY Elektronik GmbH**

**DATA SHEET**

**LCD MODULE**

**DEM 240128A ADX-PW-N**

*Product Specification*

*Version : 1*

17.06.2017

# GENERAL SPECIFICATION

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MODULE NO. :

**DEM 240128A ADX-PW-N**

CUSTOMER P/N:

Version NO.	Change Description	Date
0	Original Version	15.06.2017
1	Change the LCD to Transmissive negative and change the OP./ST. Temperature	17.06.2017

PREPARED BY: GJJ

DATE: 17.06.2017

APPROVED BY: MH

DATE: 17.06.2017

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**1. FUNCTIONS & FEATURES**

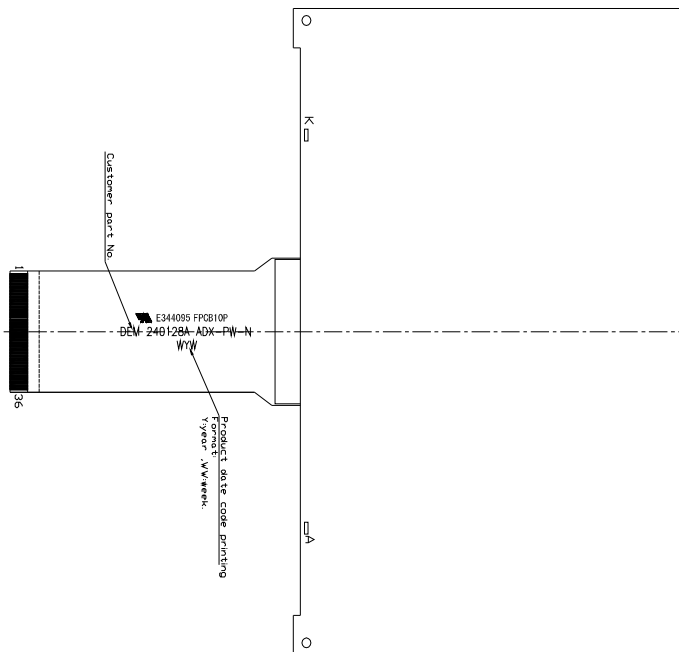
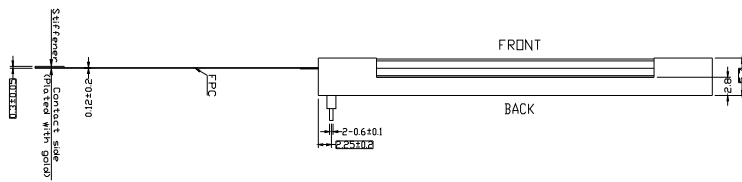
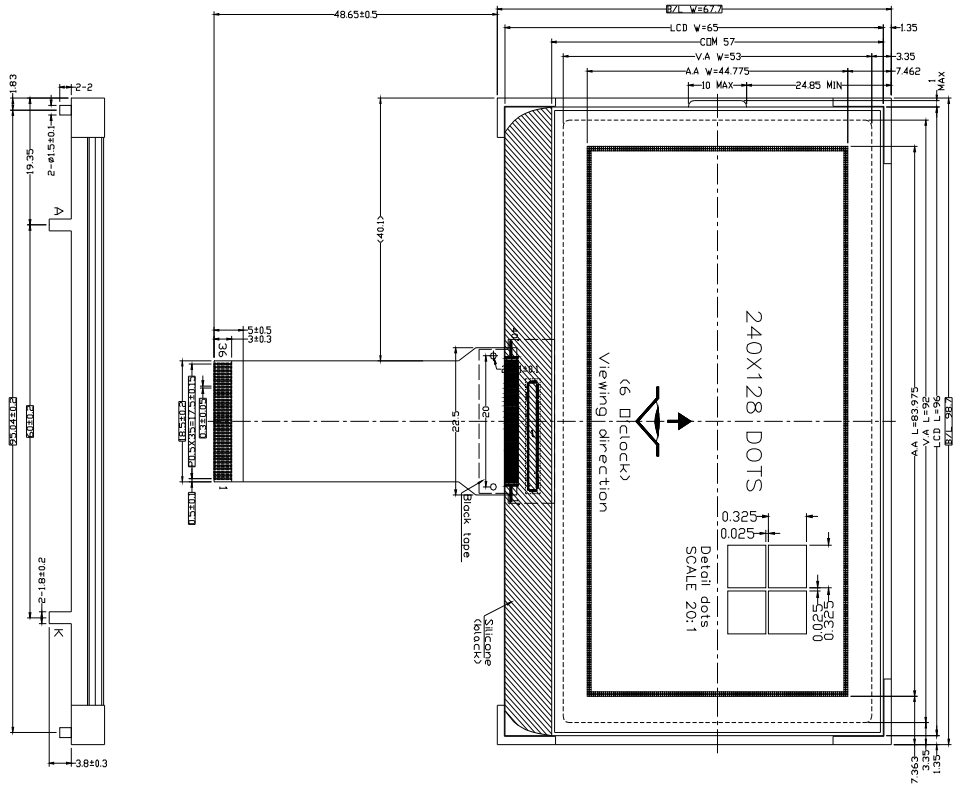
<b>MODULE NAME</b>	<b>LCD Type</b>	<b>Remark</b>
DEM 240128A ADX-PW-N	ASTN Transmissive Negative Mode	

- Viewing Direction : 6 O'clock
- Driving Scheme : 1/144Duty Cycle, 1/12 Bias
- Power Supply Voltage : 3.0 Volt (typ.)
- LCD Operation Voltage : 14.5 Volt (typ.)
- Driver IC : ST7529-G (Sitronix)
- Display Format : 240 x 128 Dots
- RoHS Compliant

**2. MECHANICAL SPECIFICATIONS**

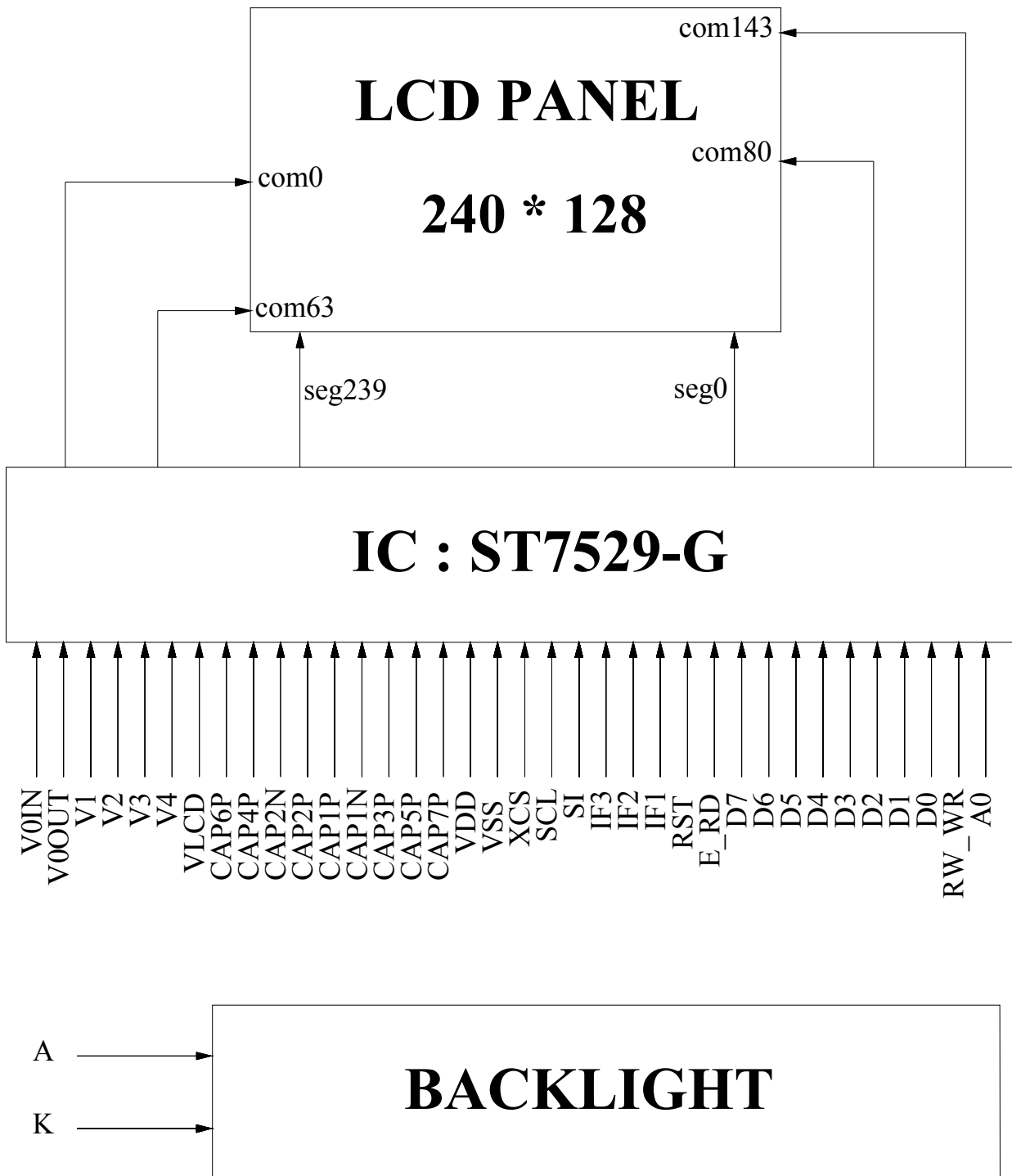
- Module Size(Without FPC) : 98.70 x 67.70 x 5.70 mm
- View Area : 92.00 x 53.00 mm
- Active Area : 83.975 x 44.775 mm
- Dot Size : 0.325 x 0.325 mm
- Dot Pitch : 0.35 x 0.35 mm

3. EXTERNAL DIMENSIONS (Unit: mm)



- Remarks:
1. Unmarked tolerance is  $\pm 0.3$
  2. All materials comply with RoHS
  3. .....critical dimension.

4. BLOCK DIAGRAM



## 5. PIN ASSIGNMENT

Pin No.	Name	Description												
1	A0	Register select input pin – A0 = "H": D0 to D7 or SI are display data – A0 = "L": D0 to D7 or SI are control data												
2	RW_WR	Read / Write execution control pin												
		<table border="1"> <thead> <tr> <th>MPU type</th> <th>RW_WR</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>6800-series</td> <td>RW</td> <td>Read / Write control input pin RW = "H" : read RW = "L" : write</td> </tr> <tr> <td>8080-series</td> <td>/WR</td> <td>Write enable clock input pin The data on D0 to D7 are latched at the rising edge of the /WR signal.</td> </tr> </tbody> </table>	MPU type	RW_WR	Description	6800-series	RW	Read / Write control input pin RW = "H" : read RW = "L" : write	8080-series	/WR	Write enable clock input pin The data on D0 to D7 are latched at the rising edge of the /WR signal.			
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8080-series	/WR	Write enable clock input pin The data on D0 to D7 are latched at the rising edge of the /WR signal.												
3	D0	They connect to the standard 8-bit MPU bus When the following interface is selected and the XCS pin is high, the following pins become high impedance, which should be fixed to VDD or VSS. Serial interface: D7-D0 are in the state of high impedance												
4	D1													
5	D2													
6	D3													
7	D4													
8	D5													
9	D6													
10	D7													
11	E_RD	Read / Write execution control pin												
		<table border="1"> <thead> <tr> <th>MPU Type</th> <th>E_RD</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>6800-series</td> <td>E</td> <td>Read / Write control input pin – RW = "H": When E is "H", D0 to D7 are in an output status. – RW = "L": The data on D0 to D7 are latched at the falling edge of the E signal.</td> </tr> <tr> <td>8080-series</td> <td>/RD</td> <td>Read enable clock input pin When /RD is "L", D0 to D7 are in an output status.</td> </tr> </tbody> </table>	MPU Type	E_RD	Description	6800-series	E	Read / Write control input pin – RW = "H": When E is "H", D0 to D7 are in an output status. – RW = "L": The data on D0 to D7 are latched at the falling edge of the E signal.	8080-series	/RD	Read enable clock input pin When /RD is "L", D0 to D7 are in an output status.			
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8080-series	/RD	Read enable clock input pin When /RD is "L", D0 to D7 are in an output status.												
12	RST	Reset input pin When RST is "L", initialization is executed.												
13	IF1	Parallel / Serial data input select input												
14	IF2	<table border="1"> <thead> <tr> <th>IF1</th> <th>IF2</th> <th>IF3</th> <th>MPU interface type</th> </tr> </thead> <tbody> <tr> <td>H</td> <td>H</td> <td>L</td> <td>80 series 8-bit parallel</td> </tr> <tr> <td>L</td> <td>H</td> <td>H</td> <td>68 series 8-bit parallel</td> </tr> </tbody> </table>	IF1	IF2	IF3	MPU interface type	H	H	L	80 series 8-bit parallel	L	H	H	68 series 8-bit parallel
		IF1	IF2	IF3	MPU interface type									
H	H	L	80 series 8-bit parallel											
L	H	H	68 series 8-bit parallel											
15	IF3	<table border="1"> <tbody> <tr> <td>L</td> <td>L</td> <td>H</td> <td>9-bit serial (3 line)</td> </tr> <tr> <td>L</td> <td>L</td> <td>L</td> <td>8-bit serial (4 line)</td> </tr> </tbody> </table>	L	L	H	9-bit serial (3 line)	L	L	L	8-bit serial (4 line)				
		L	L	H	9-bit serial (3 line)									
L	L	L	8-bit serial (4 line)											
16	SI	This pin is used to input serial data when the serial interface is selected. (3 line and 4 line)												
17	SCL	This pin is used to input serial clock when the serial interface is selected. The data is latched at the rising edge. (3 line and 4 line)												
18	XCS	Chip select input pins Data/instruction I/O is enabled only when XCS is "L". When chip select is non-active, D0 to D7 may be high impedance.												
19	VSS	Ground												
20	VDD	Power supply												

21	CAP7P	DC/DC Voltage Converter										
22	CAP5P											
23	CAP3P											
24	CAP1N											
25	CAP1P											
26	CAP2P											
27	CAP2N											
28	CAP4P											
29	CAP6P											
30	VLCD	LCD power supply voltage										
31	V4	<p>LCD driver supply voltages                      V0In &amp; V0out should be connected together in FPC area.                      Voltages should have the following relationship:  <math>V0 \geq V1 \geq V2 \geq V3 \geq V4 \geq VSS</math>                      When the internal power circuit is active, these voltages are generated as the following table according to the state of LCD bias.</p> <table border="1"> <thead> <tr> <th>LCD bias</th> <th>V1</th> <th>V2</th> <th>V3</th> <th>V4</th> </tr> </thead> <tbody> <tr> <td>1/N bias</td> <td><math>(N-1) / N \times V0</math></td> <td><math>(N-2) / N \times V0</math></td> <td><math>(2/N) \times V0</math></td> <td><math>(1/N) \times V0</math></td> </tr> </tbody> </table>	LCD bias	V1	V2	V3	V4	1/N bias	$(N-1) / N \times V0$	$(N-2) / N \times V0$	$(2/N) \times V0$	$(1/N) \times V0$
LCD bias	V1		V2	V3	V4							
1/N bias	$(N-1) / N \times V0$		$(N-2) / N \times V0$	$(2/N) \times V0$	$(1/N) \times V0$							
32	V3											
33	V2											
34	V1											
35	V0OUT											
36	V0IN											

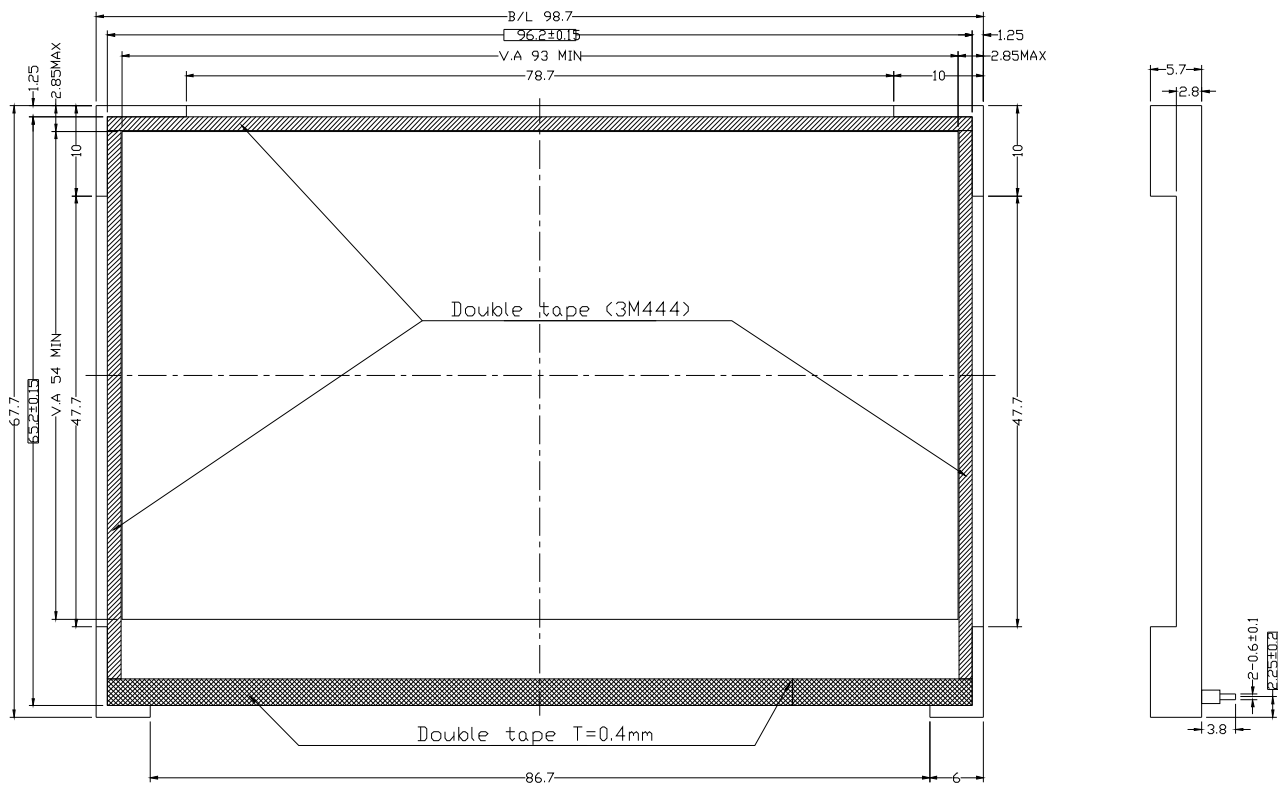
NOTE: N = 5 to 14



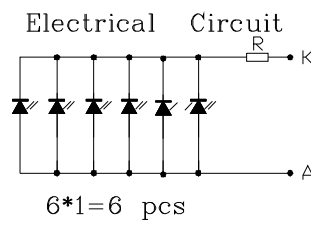
6. BACKLIGHT DRAWING

Electrical/Optical Specifications

Item	Symbol	Min.	Typ.	Max.	Unit	Condition
Forward Voltage	Vf	--	3.1	--	V	--
Forward Current	If	--	90	120	mA	Vf = 3.1 V
Power Dissipation	Pd	--	--	0.372	W	Vf = 3.1 V
Reverse Voltage	Vr	--	--	5	V	--
Reverse Current	Ir	--	--	0.1	mA	Vr = 5 V Each chip
Luminous Intensity	Lv	400	--	--	cd/m <sup>2</sup>	Vf = 3.1 V
Luminous Uniformity	ΔLv	70	--	--	%	Vf = 3.1 V
Color Chromaticity	X	0.26	--	0.33	--	Vf = 3.1 V
	Y	0.26	--	0.33	--	



- Remarks:
1. Unmarked tolerance is ±0.3
  2. All materials comply with RoHs
  3. [ ] ...:critical dimension.
  4. Backlight color: white
  5. LED life time 50000H



**7. ABSOLUTE MAXIMUM RATINGS**

Parameter	Symbol	Min	Max	Unit
Power Supply Voltage	VDD,VDD1	-0.5	+5.0	V
Power Supply Voltage	VDD2,VDD3, VDD4,VDD5	-0.5	+5.0	V
Power Supply Voltage(VDD Standard)	VLCDIN, VLCDOUT	-0.5	+22	V
Power Supply Voltage(VDD Standard)	V0,V1,V2,V3, V4	-0.3	VLCDIN	V
Input Voltage	VIN	-0.5	VDD+0.5	V
Output Voltage	VO	-0.5	VDD+0.5	V
Operating Temperature	Topr	-30	+80	□
Storage Temperature	Tstr	-40	+90	□

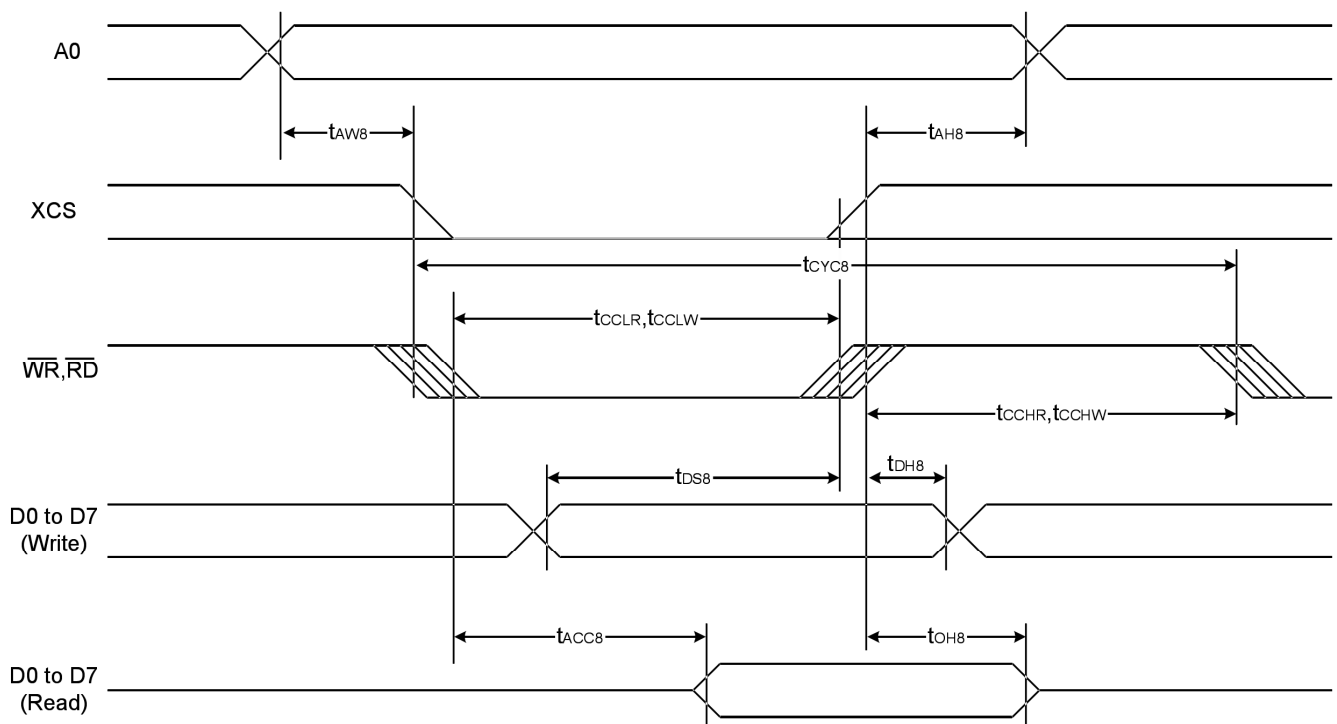
**8. DC CHARACTERISTICS**

Item	Symbol	Standard Value			Test Condition	Unit
		Min.	Typ.	Max.		
Power supply Voltage	VDD	2.7	3.0	3.3		V
Operating Voltage	Vop	14.2	14.5	14.8		
Current Consumption	IDD	---	1.7	2.55	Test character pattern	mA

9. AC ELECTRICAL CHARACTERISTICS

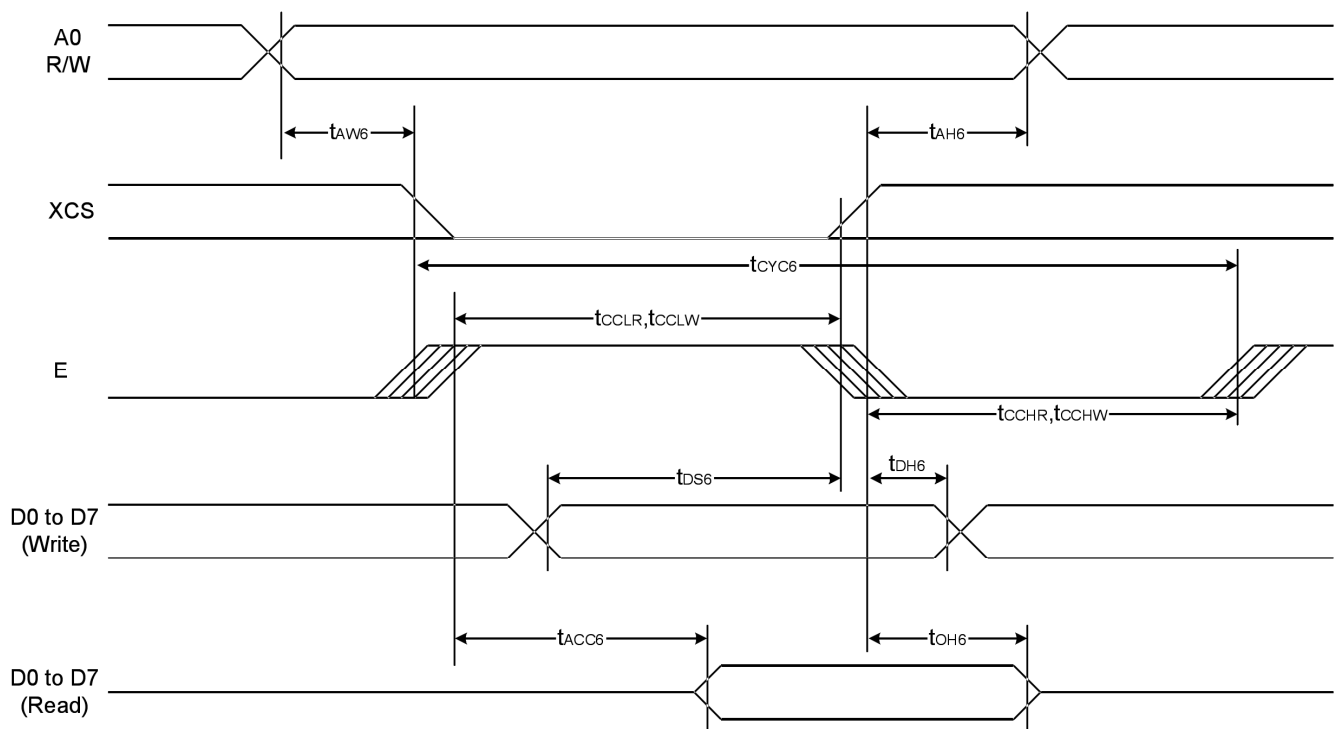
9.1 System bus READ/WRITE characteristics for the 8080 series MPU

Item	Signal	Symbol	Condition	Rating		Units
				Min.	Max.	
Address hold time	A0	$t_{AH8}$		20	—	ns
Address setup time		$t_{AW8}$		20	—	
System cycle time		$t_{CYC8}$		200	—	
Enable L pulse width (WRITE)	WR	$t_{CCLW}$		100	—	
Enable H pulse width (WRITE)		$t_{CCHW}$		100	—	
Enable L pulse width (READ)	RD	$t_{CCLR}$		100	—	
Enable H pulse width (READ)		$t_{CCHR}$		100	—	
WRITE Data setup time	D0 to D7	$t_{DS8}$		150	—	
WRITE Address hold time		$t_{DH8}$		20	—	
READ access time		$t_{ACC8}$	CL = 100 pF	—	40	
READ Output disable time		$t_{OH8}$	CL = 100 pF	—	30	



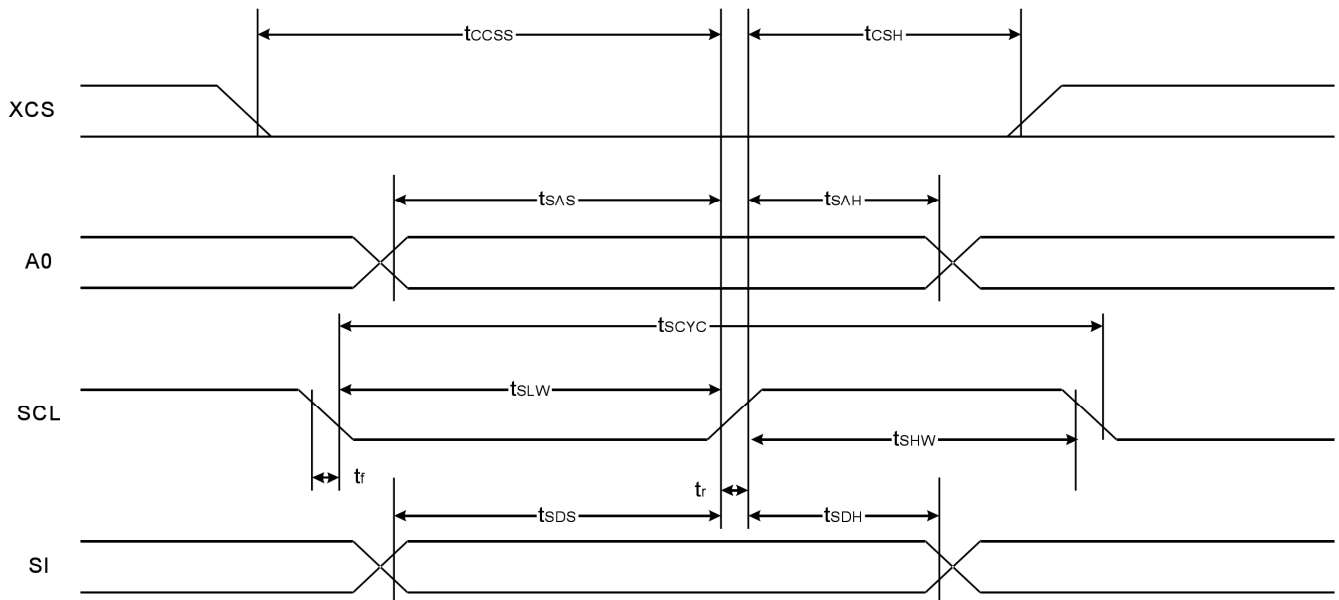
9.2 System bus READ/WRITE characteristics for the 6800 series MPU

Item	Signal	Symbol	Condition	Rating		Units
				Min.	Max.	
Address hold time	A0	$t_{AH6}$		20	—	ns
Address setup time		$t_{AW6}$		20	—	
System cycle time		$t_{CYC6}$		200	—	
Enable L pulse width (WRITE)	WR	$t_{EWLW}$		100	—	
Enable H pulse width (WRITE)		$t_{EWHW}$		100	—	
Enable L pulse width (READ)	RD	$t_{EWLR}$		100	—	
Enable H pulse width (READ)		$t_{EWHR}$		100	—	
WRITE Data setup time	D0 to D7	$t_{DS6}$		150	—	
WRITE Address hold time		$t_{DH6}$		20	—	
READ access time		$t_{ACC6}$	CL = 100 pF	—	40	
READ Output disable time		$t_{OH6}$	CL = 100 pF	—	30	



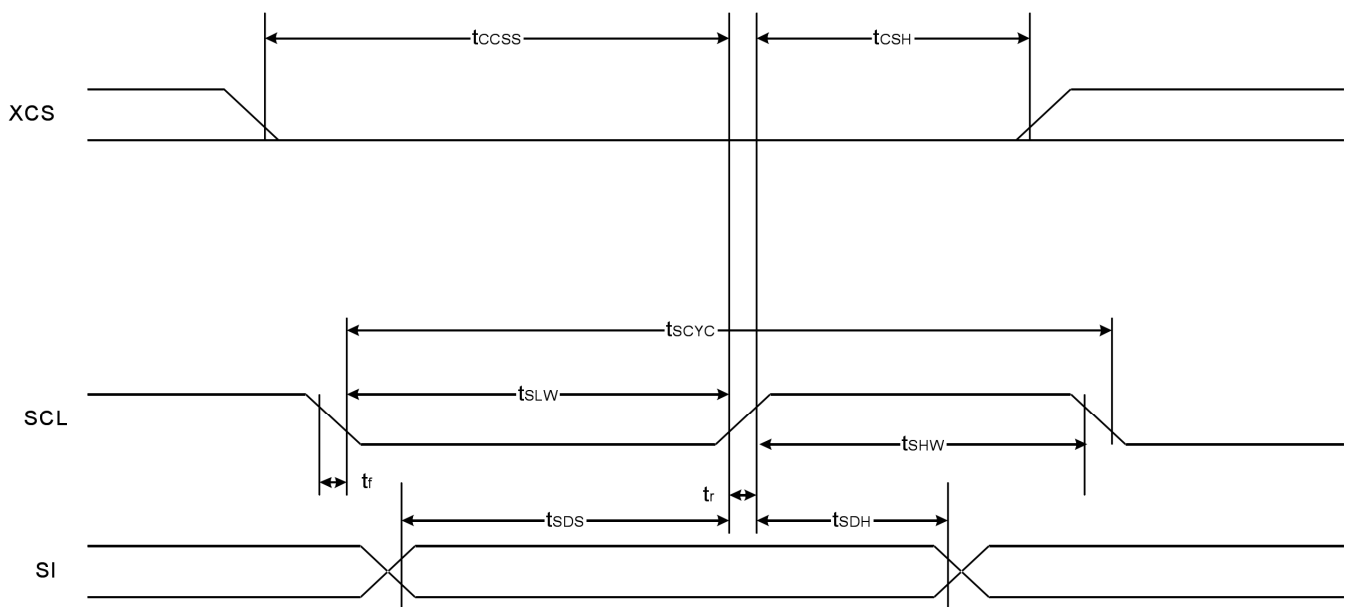
9.3 The Serial Interface (4-Line interface)

Item	Signal	Symbol	Condition	Rating		Units
				Min.	Max.	
Serial Clock Period	SCL	t <sub>SCYC</sub>	—	100	—	ns
SCL “H” pulse width		t <sub>SHW</sub>	—	50	—	
SCL “L” pulse width		t <sub>SLW</sub>	—	50	—	
Address setup time	A0	t <sub>SAS</sub>	—	40	—	
Address hold time		t <sub>SAH</sub>	—	30	—	
Data setup time	SI	t <sub>SDS</sub>	—	30	—	
Data hold time		t <sub>SDH</sub>	—	30	—	
CS-SCL time	XCS	t <sub>CSS</sub>	—	20	—	
CS-SCL time		t <sub>CSH</sub>	—	50	—	



**9.4 The Serial Interface (3-Line interface)**

Item	Signal	Symbol	Condition	Rating		Units
				Min.	Max.	
Serial Clock Period	SCL	t <sub>SCYC</sub>	—	100	—	ns
SCL “H” pulse width		t <sub>SHW</sub>	—	50	—	
SCL “L” pulse width		t <sub>SLW</sub>	—	50	—	
Data setup time	SI	t <sub>SDS</sub>	—	30	—	
Data hold time		t <sub>SDH</sub>	—	30	—	
CS-SCL time	XCS	t <sub>CSS</sub>	—	20	—	
CS-SCL time		t <sub>CSH</sub>	—	50	—	



## 10. COMMAND TABLE

Ext=0 or Ext=1

Index	Command	A0	RD	WR	D7	D6	D5	D4	D3	D2	D1	D0	Function	Hex	Parameter
1	Ext In	0	1	0	0	0	1	1	0	0	0	0	Ext=0 Set	30	None
2	Ext Out	0	1	0	0	0	1	1	0	0	0	1	Ext=1 Set	31	None

Ext=0

Index	Command	A0	RD	WR	D7	D6	D5	D4	D3	D2	D1	D0	Function	Hex	Parameter
1	DISON	0	1	0	1	0	1	0	1	1	1	1	Display On	AF	None
2	DISOFF	0	1	0	1	0	1	0	1	1	1	0	Display Off	AE	None
3	DISNOR	0	1	0	1	0	1	0	0	1	1	0	Normal Display	A6	None
4	DISINV	0	1	0	1	0	1	0	0	1	1	1	Inverse Display	A7	None
5	COMSCN	0	1	0	1	0	1	1	1	0	1	1	COM Scan Direction	BB	1 byte
6	DISCTRL	0	1	0	1	1	0	0	1	0	1	0	Display Control	CA	3 bytes
7	SLPIN	0	1	0	1	0	0	1	0	1	0	1	Sleep In	95	None
8	SLPOUT	0	1	0	1	0	0	1	0	1	0	0	Sleep Out	94	None
9	LASET	0	1	0	0	1	1	1	0	1	0	1	Line Address Set	75	2 bytes
10	CASET	0	1	0	0	0	0	1	0	1	0	1	Column Address Set	15	2 bytes
11	DATSDR	0	1	0	1	0	1	1	1	1	0	0	Data Scan Direction	BC	3 bytes
12	RAMWR	0	1	0	0	1	0	1	1	1	0	0	Writing to Memory	5C	Data
13	RAMRD	0	1	0	0	1	0	1	1	1	0	1	Reading from Memory	5D	Data
14	PTLIN	0	1	0	1	0	1	0	1	0	0	0	Partial display in	A8	2 bytes
15	PTLOUT	0	1	0	1	0	1	0	1	0	0	1	Partial display out	A9	None
16	RMWIN	0	1	0	1	1	1	0	0	0	0	0	Read and Modify Write	E0	None
17	RMWOUT	0	1	0	1	1	1	0	1	1	1	0	RMW end	EE	None
18	ASCSET	0	1	0	1	0	1	0	1	0	1	0	Area Scroll Set	AA	4 bytes
19	SCSTART	0	1	0	1	0	1	0	1	0	1	1	Scroll Start Set	AB	1 byte
20	OSCON	0	1	0	1	1	0	1	0	0	0	1	Internal OSC on	D1	None
21	OSCOFF	0	1	0	1	1	0	1	0	0	1	0	Internal OSC off	D2	None
22	PWRCTRL	0	1	0	0	0	1	0	0	0	0	0	Power Control	20	1 byte
23	VOLCTRL	0	1	0	1	0	0	0	0	0	0	1	EC control	81	2 bytes
24	VOLUP	0	1	0	1	1	0	1	0	1	1	0	EC increase 1	D6	None
25	VOLDOWN	0	1	0	1	1	0	1	0	1	1	1	EC decrease 1	D7	None
26	RESERVED	0	1	0	1	0	0	0	0	0	1	0	Not Use	82	0
27	EPSRRD1	0	1	0	0	1	1	1	1	1	0	0	READ Register1	7C	None

28	EPSRRD2	0	1	0	0	1	1	1	1	1	0	1	READ Register2	7D	None
29	NOP	0	1	0	0	0	1	0	0	1	0	1	NOP Instruction	25	None
30	STREAD	0	0	1	Read Data							Status Read			
31	EPINT	0	1	0	0	0	0	0	0	1	1	1	Initial code(1)	07	1 byte

**Ext=1**

<i>Index</i>	<i>Command</i>	<i>A0</i>	<i>RD</i>	<i>WR</i>	<i>D7</i>	<i>D6</i>	<i>D5</i>	<i>D4</i>	<i>D3</i>	<i>D2</i>	<i>D1</i>	<i>D0</i>	<i>Function</i>	<i>Hex</i>	<i>Parameter</i>
1	Gray 1 Set	0	1	0	0	0	1	0	0	0	0	0	FRAME 1 Gray PWM Set	20	16 bytes
2	Gray 2 Set	0	1	0	0	0	1	0	0	0	0	1	FRAME 2 Gray PWM Set	21	16 bytes
3	Wt. Set	0	1	0	0	0	1	0	0	0	1	0	Weight Set	22	3 bytes
4	ANASET	0	1	0	0	0	1	1	0	0	1	0	Analog Circuit Set	32	3 bytes
5	DITHOFF	0	1	0	0	0	1	1	0	1	0	0	Dithering Circuit Off	34	None
6	DITHON	0	1	0	0	0	1	1	0	1	0	1	Dithering Circuit On	35	None
7	EPCTIN	0	1	0	1	1	0	0	1	1	0	1	Control EEPROM	CD	1 byte
8	EPCOUT	0	1	0	1	1	0	0	1	1	0	0	Cancel EEPROM	CC	None
9	EPMWR	0	1	0	1	1	1	1	1	1	0	0	Write to EEPROM	FC	None
10	EPMRD	0	1	0	1	1	1	1	1	1	0	1	Read from EEPROM	FD	None



**11. ACCEPT QUALITY LEVEL (AQL)**

11.1 AQL Standard Value: Critical Defect =0.1, Major Defect=0.65; Minor Defect =2.5.

11.2 Inspection Plan: MIL-STD-105E, Normal Inspection Level II, Single Sampling Plan

**12. RELIABILITY TEST**

Operating life time: 50000 hours (at room temperature without direct irradiation of sunlight)

Reliability characteristics shall meet following requirements.

<b>Test Item</b>	<b>Test Condition</b>
High temperature storage	+90□ x 96hrs
Low temperature storage	-40□ x 96hrs
High temperature operation	+80□ x 96hrs
Low temperature operation	-30□ x 96hrs
High temperature, High humidity	+60□ x 95%RH x 96hrs
Thermal shock	-30□ x 30min → +25□ x 10s → +80□ x 30min 5Cycles
Vibration test	Frequency x Swing x Time 40Hz x 4mm x 4hrs
Drop test	Drop height x No. of drops 1.0m x 6drops

**13. QUALITY DESCRIPTION**

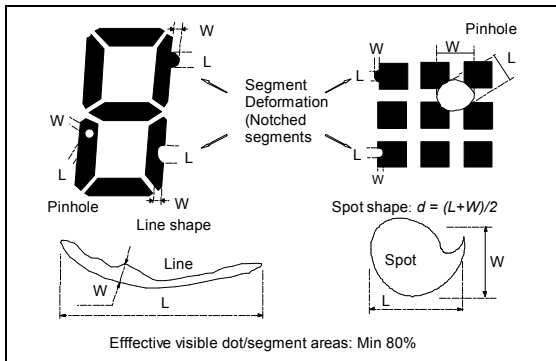
**DEFECT SPECIFICATION:**

a: Table for Cosmetic defects

(Note: nc = not counted).

Sizes and number of defects

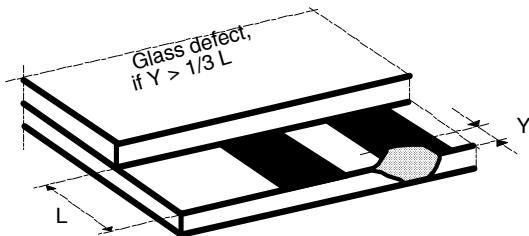
(Max. Qty)



Examples/ Shapes

b: Glass defects

b1: Glass defects at contact ledge



b2: Glass chipping in other areas shall not be in conflict with the product's function.

Defect Type	Max. defect size [ $\mu\text{m}$ ] d or L W	Max. Quantity.
Black or White Spots	$d \leq 100$	nc
	$100 < d \leq 200$	3
Black or White Lines	-- $W \leq 10$	nc
	$L \leq 3000$ $W \leq 30$	2
	$L \leq 2000$ $W \leq 50$	2
Pinhole	$d \leq 100$	nc
	$100 < d \leq 200$	1/segment
(Total defects)		(5)
Segment Deformation	$W \leq 100$	nc
Bubble (e.g. under pola)	$d \leq 150$	nc
	$200 < d \leq 400$	2

**14. LCD MODULES HANDLING PRECAUTIONS**

- The display panel is made of glass. Do not subject it to a mechanical shock by dropping it from a high place, etc.
- If the display panel is damaged and the liquid crystal substance inside it leaks out, do not get any in your mouth. If the substance come into contact with your skin or clothes promptly wash it off using soap and water.
- Do not apply excessive force to the display surface or the adjoining areas since this may cause the color tone to vary.
- The polarizer covering the display surface of the LCD module is soft and easily scratched. Handle this polarize carefully.
- To prevent destruction of the elements by static electricity, be careful to maintain an optimum work environment.

-Be sure to ground the body when handling the LCD module.

-Tools required for assembly, such as soldering irons, must be properly grounded.

-To reduce the amount of static electricity generated, do not conduct assembly and other work under dry conditions.

-The LCD module is coated with a film to protect the display surface. Exercise care when peeling off this protective film since static electricity may be generated.

- **Storage precautions**

When storing the LCD modules, avoid exposure to direct sunlight or to the light of fluorescent lamps. Keep the modules in bags designed to prevent static electricity charging under low temperature / normal humidity conditions (avoid high temperature / high humidity and low temperatures below 0□). Whenever possible, the LCD modules should be stored in the same conditions in which they were shipped from our company.

**15. OTHERS**

- Liquid crystals solidify at low temperature (below the storage temperature range) leading to defective orientation of liquid crystal or the generation of air bubbles (black or white). Air bubbles may also be generated if the module is subjected to a strong shock at a low temperature.
- If the LCD modules have been operating for a long time showing the same display patterns may remain on the screen as ghost images and a slight contrast irregularity may also appear. Abnormal operating status can be resumed to be normal condition by suspending use for some time. It should be noted that this phenomena does not adversely affect performance reliability.
- To minimize the performance degradation of the LCD modules resulting from caused by static electricity, etc. exercise care to avoid holding the following sections when handling the modules :
  - Exposed area of the printed circuit board
  - Terminal electrode sections