

**DISPLAY Elektronik GmbH**

**DATA SHEET**

**LCD MODULE**

**DEM 240064B ADX-PW-N**

*Product Specification*

*Version: 1*

**17.06.2017**

# GENERAL SPECIFICATION

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MODULE NO. :

## DEM 240064B ADX-PW-N

CUSTOMER P/N:

VERSION NO.	CHANGE DESCRIPTION	DATE
0	Original Version	15.06.2017
1	Change the LCD to Transmissive negative and change the OP./ST. Temperature	17.06.2017

PREPARED BY: GJJ

DATE: 17.06.2017

APPROVED BY: MH

DATE: 17.06.2017

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**1. FUNCTIONS & FEATURES**

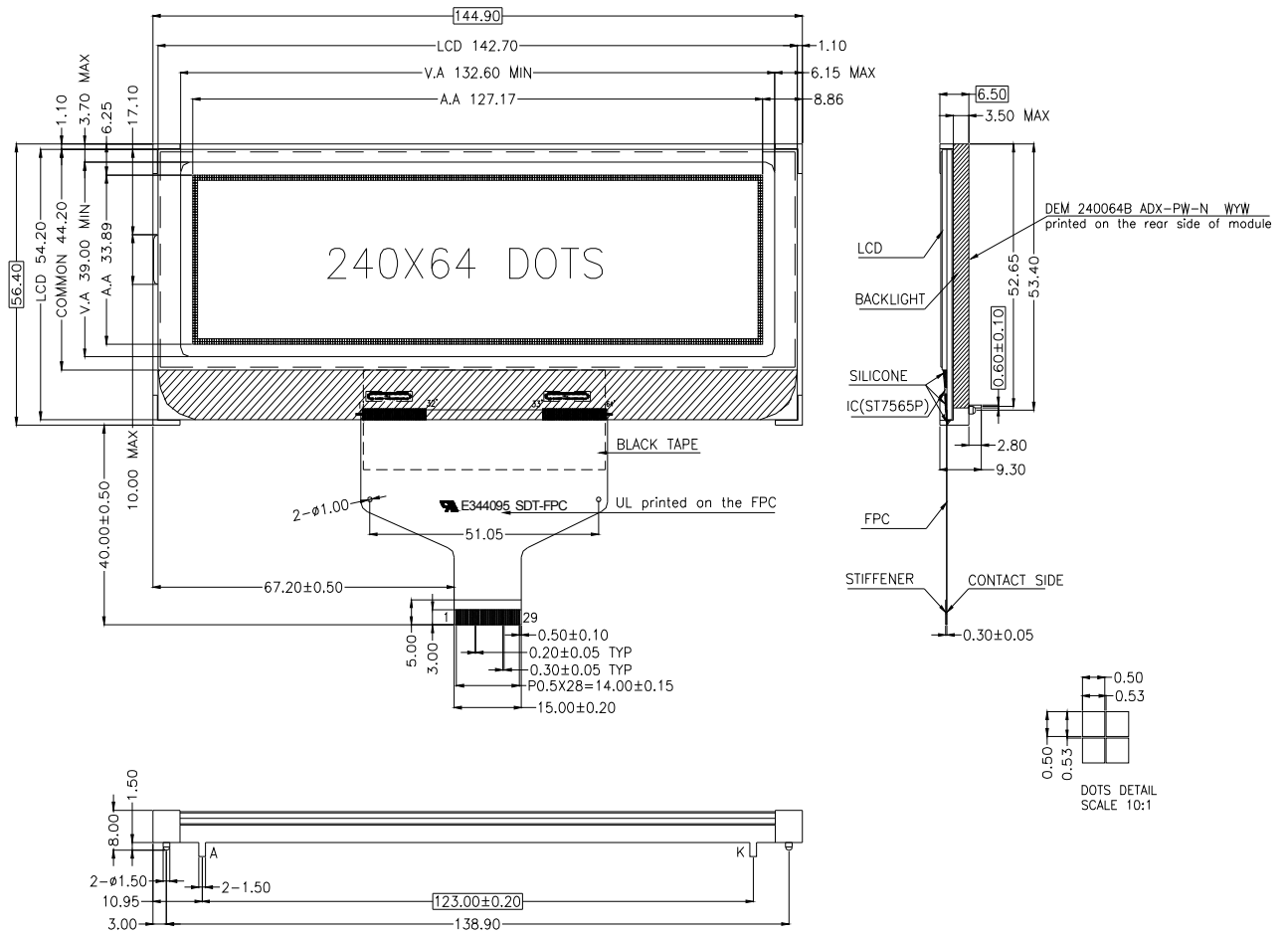
<b>MODULE NAME</b>	<b>LCD TYPE</b>	<b>Remark</b>
DEM 240064B ADX-PW-N	ASTN Transmissive Negative Mode	---

- Viewing Direction : 6 O'clock
- Driving Scheme : 1/65Duty Cycle, 1/9 Bias
- Power Supply Voltage : 3.3 Volt (typ.)
- LCD Operation Voltage : 11.0 Volt (typ.)
- Display Format : 240 x 64 Dots
- Operating Temperature : -30°C to +80°C
- Storage Temperature : -40°C to +90°C
- RoHS Conformed

**2. MECHANICAL SPECIFICATIONS**

- Module Size : 144.90 x 56.40 x 6.50 mm
- View Area Size : 132.60 x 39.00 mm
- Dot Size : 0.50 x 0.50 mm
- Dot Gap : 0.03 mm

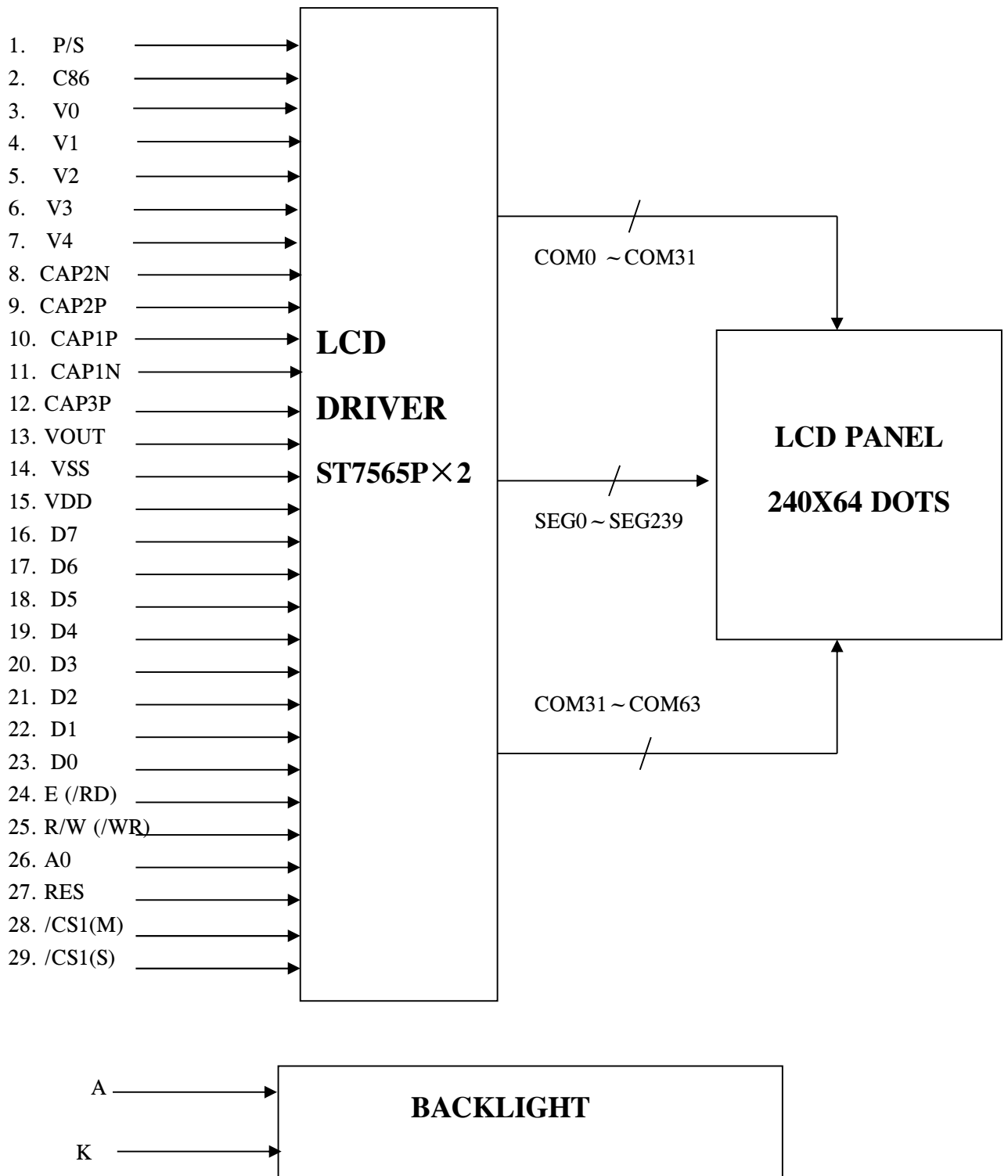
**3. EXTERNAL DIMENSIONS**



**Remarks:**

- 1. Unmarked tolerance is ±0.3,
- 2. The material comply with RoHS,

**4. BLOCK DIAGRAM**



5. PIN ASSIGNMENT

Pin No.	Name	Description																														
1	P/S	<p>This is the parallel data input/serial data input switch terminal.                      P/S = "H": Parallel data input.                      P/S = "L": Serial data input.                      The following applies depending on the P/S status:</p> <table border="1"> <thead> <tr> <th>P/S</th> <th>DATA/Command</th> <th>Data</th> <th>Read/Write</th> <th>4-line SPI Clock</th> </tr> </thead> <tbody> <tr> <td>H</td> <td>D/C(A0)</td> <td>D0 to D7</td> <td>/RD,/WR</td> <td>×</td> </tr> <tr> <td>L</td> <td>D/C(A0)</td> <td>SI(D7)</td> <td>Write only</td> <td>SCL(D6)</td> </tr> </tbody> </table> <p>When P/S = "L", D0 to D5 fixed "H".                      /RD (E) and /WR (R/W) are fixed to either "H" or "L".                      With serial data input, It is impossible read data from RAM .</p>	P/S	DATA/Command	Data	Read/Write	4-line SPI Clock	H	D/C(A0)	D0 to D7	/RD,/WR	×	L	D/C(A0)	SI(D7)	Write only	SCL(D6)															
P/S	DATA/Command	Data	Read/Write	4-line SPI Clock																												
H	D/C(A0)	D0 to D7	/RD,/WR	×																												
L	D/C(A0)	SI(D7)	Write only	SCL(D6)																												
2	C86	<p>This is the MPU interface switch terminal.                      C86 = "H": 6800 Series MPU interface.                      C86 = "L": 8080 MPU interface.</p>																														
3	V0	<p>This is a multi-level power supply for the liquid crystal drive. The voltage Supply applied is determined by the liquid crystal cell, and is changed through the use of a resistive voltage divided or through changing the impedance using an op. amp. Voltage levels are determined based on Vss, and must maintain the relative magnitudes shown below.  <math>V0 \cong V1 \cong V2 \cong V3 \cong V4 \cong V_{ss}</math>                      When the power supply turns ON, the internal power supply circuits produce the V1 to V4 voltages shown below. The voltage settings are selected using the LCD bias set command.</p>																														
4	V1																															
5	V2																															
6	V3																															
7	V4	<table border="1"> <thead> <tr> <th></th> <th>1/65 DUTY</th> <th>1/49 DUTY</th> <th>1/33 DUTY</th> <th>1/55 DUTY</th> <th>1/53 DUTY</th> </tr> </thead> <tbody> <tr> <td>V1</td> <td>8/9*V0,6/7*V0</td> <td>7/8*V0,5/6*V0</td> <td>5/6*V0,4/5*V0</td> <td>7/8*V0,5/6*V0</td> <td>7/8*V0,5/6*V0</td> </tr> <tr> <td>V2</td> <td>7/9*V0,5/7*V0</td> <td>6/8*V0,4/6*V0</td> <td>4/6*V0,3/5*V0</td> <td>6/8*V0,4/6*V0</td> <td>6/8*V0,4/6*V0</td> </tr> <tr> <td>V3</td> <td>2/9*V0,2/7*V0</td> <td>2/8*V0,2/6*V0</td> <td>2/6*V0,2/5*V0</td> <td>2/8*V0,2/6*V0</td> <td>2/8*V0,2/6*V0</td> </tr> <tr> <td>V4</td> <td>1/9*V0,1/7*V0</td> <td>1/8*V0,1/6*V0</td> <td>1/6*V0,1/5*V0</td> <td>1/8*V0,1/6*V0</td> <td>1/8*V0,1/6*V0</td> </tr> </tbody> </table>		1/65 DUTY	1/49 DUTY	1/33 DUTY	1/55 DUTY	1/53 DUTY	V1	8/9*V0,6/7*V0	7/8*V0,5/6*V0	5/6*V0,4/5*V0	7/8*V0,5/6*V0	7/8*V0,5/6*V0	V2	7/9*V0,5/7*V0	6/8*V0,4/6*V0	4/6*V0,3/5*V0	6/8*V0,4/6*V0	6/8*V0,4/6*V0	V3	2/9*V0,2/7*V0	2/8*V0,2/6*V0	2/6*V0,2/5*V0	2/8*V0,2/6*V0	2/8*V0,2/6*V0	V4	1/9*V0,1/7*V0	1/8*V0,1/6*V0	1/6*V0,1/5*V0	1/8*V0,1/6*V0	1/8*V0,1/6*V0
	1/65 DUTY	1/49 DUTY	1/33 DUTY	1/55 DUTY	1/53 DUTY																											
V1	8/9*V0,6/7*V0	7/8*V0,5/6*V0	5/6*V0,4/5*V0	7/8*V0,5/6*V0	7/8*V0,5/6*V0																											
V2	7/9*V0,5/7*V0	6/8*V0,4/6*V0	4/6*V0,3/5*V0	6/8*V0,4/6*V0	6/8*V0,4/6*V0																											
V3	2/9*V0,2/7*V0	2/8*V0,2/6*V0	2/6*V0,2/5*V0	2/8*V0,2/6*V0	2/8*V0,2/6*V0																											
V4	1/9*V0,1/7*V0	1/8*V0,1/6*V0	1/6*V0,1/5*V0	1/8*V0,1/6*V0	1/8*V0,1/6*V0																											
8	CAP2N	DC/DC voltage converter. Connects a capacitor between this terminal and CAP2P terminal.																														
9	CAP2P	DC/DC voltage converter. Connects a capacitor between this terminal and CAP2N terminal.																														
10	CAP1P	DC/DC voltage converter. Connect a capacitor between this terminal and CAP1N terminal.																														
11	CAP1N	DC/DC voltage converter. Connects a capacitor between this terminal and CAP1P terminal.																														
12	CAP3P	DC/DC voltage converter. Connects a capacitor between this terminal and CAP1N terminal.																														
13	VOUT	DC/DC voltage converter. Connects a capacitor between this terminal and VSS or VDD.																														
14	VSS	0V pin connected to the system ground (GND)																														
15	VDD	Power supply for logic (+3.3V)																														
16	D7	<p>This is an 8-bit bi-directional data bus that connects to an 8-bit or 16-bit standard MPU data bus.                      When the serial interface is selected (P/S = "L") :                      D7 : serial data input (SI) ; D6 : the serial clock input (SCL).                      D0 to D5 are set to high impedance.                      When the chip select is not active, D0 to D7 are set to high impedance.</p>																														
17	D6																															
18	D5																															
19	D4																															
20	D3																															
21	D2																															
22	D1																															
23	D0																															

24	E(/RD)	<ul style="list-style-type: none"> <li>• When connected to an 8080 MPU, this is active LOW.</li> <li>(E) This pin is connected to the /RD signal of the 8080 MPU, and the ST7565P series data bus is in an output status when this signal is “L”.</li> <li>• When connected to a 6800 Series MPU, this is active HIGH.</li> </ul> <p>This is the 6800 Series MPU enable clock input terminal.</p>
25	R/W(/WR)	<ul style="list-style-type: none"> <li>• When connected to an 8080 MPU, this is active LOW.</li> <li>(R/W) This terminal connects to the 8080 MPU /WR signal. The signals on the data bus are latched at the rising edge of the /WR signal.</li> <li>• When connected to a 6800 Series MPU:</li> </ul> <p>This is the read/write control signal input terminal.  When R/W = “H”: Read.  When R/W = “L”: Write.</p>
26	A0	<p>This is connect to the least significant bit of the normal MPU address bus, and it determines whether the data bits are data or a command.</p> <p>A0 = “H”: Indicates that D0 to D7 are display data.  A0 = “L”: Indicates that D0 to D7 are control data.</p>
27	/RES	<p>When /RES is set to “L,” the settings are initialized.  The reset operation is performed by the /RES signal level.</p>
28	/CS1(M)	<p>This is the chip select signal. When /CS1 = “L” and CS2 = “H,” then the chip select becomes active, and data/command I/O is enabled.</p>
29	/CS1(S)	

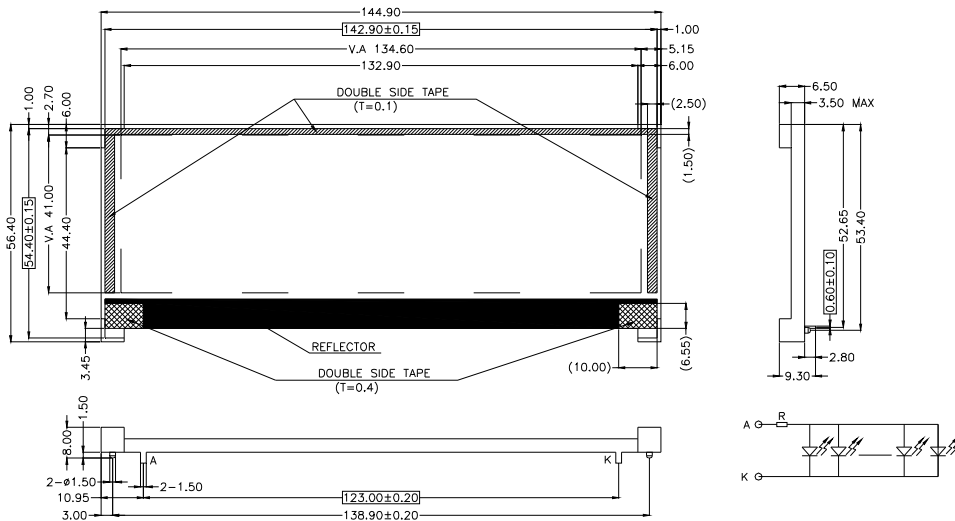


**6. BACKLIGHT ELECTRONIC/OPTICAL SPECIFICATIONS**

Electronic/Optical Specifications:

	SYMBOL	MIN.	TYP.	MAX.	UNIT	CONDITIONS
Forward Voltage	$V_f$	3.0	3.2	3.4	V	$I_f = 120 \text{ mA}$
Forward Current	$I_f$		120	160	mA	
Power Dissipation	$P_d$			0.544	W	$I_f = 120 \text{ mA}$
Reverse Voltage	$V_R$			5	V	
Reverse Current	$I_R$			0.8	mA	$V_r = 5.0 \text{ V}$
Luminous Intensity	$I_v$	150	200	TBD	cd/m <sup>2</sup>	$I_f = 120 \text{ mA}$
Luminous Uniformity		70			%	$I_f = 120 \text{ mA}$
Color Chromaticity	X	0.26		0.33		$I_f = 20 \text{ mA}$ $T_a = 25^\circ \text{ C}$ Each chip
	Y	0.26		0.33		

	SYMBOL	RATINGS
Operating Temperature	Topr	-30° C to +80° C
	Tsty	-40° C to +90° C



Remarks:  
 1.Unmarked tolerance is ±0.2.  
 2.The material comply with RoHS.  
 3.COLOR:WHITE  
 4.NO.OF SMT LED:8PCS  
 5.Lifetime 5000hours(LED Brightness ≥ 50% TYP Value of Specification)

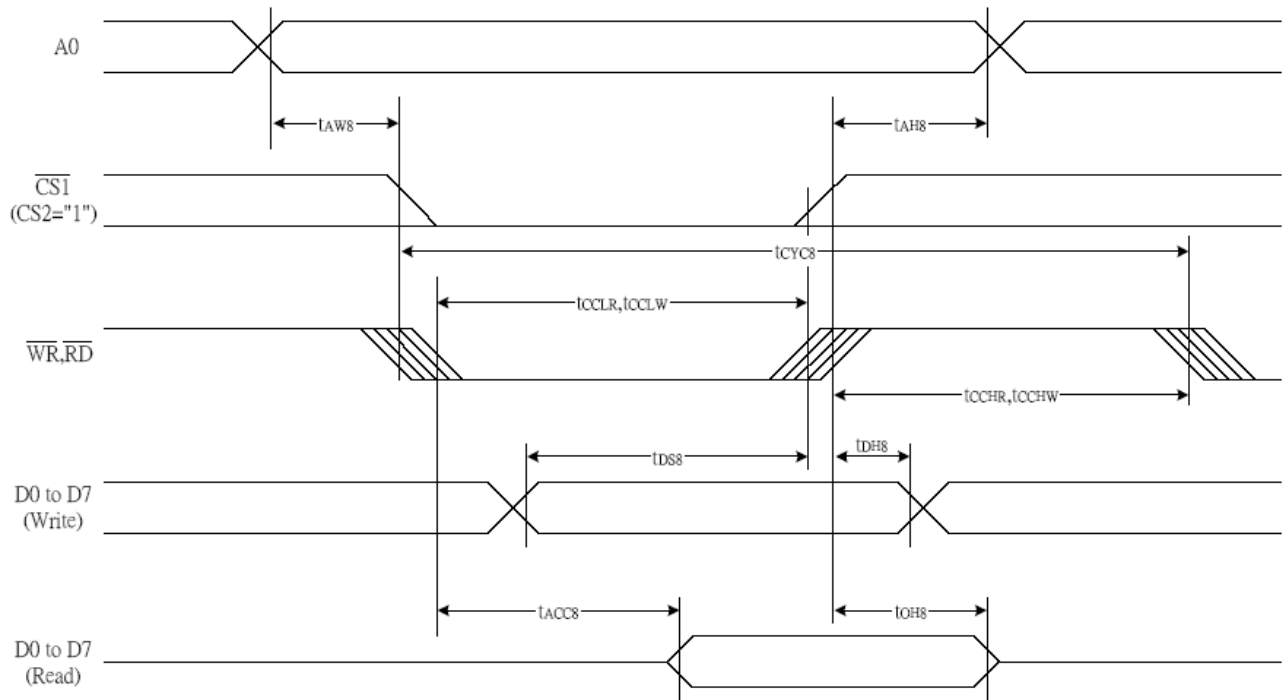
**7. DC CHARACTERISTICS**

( $V_{DD} = 3.3 \text{ V}$ ,  $T_a = 25^\circ \text{ C}$ )

ITEM	symbol	STANDARD VALUE			TEST CONDITION	UNIT
		MIN	TYP	MAX		
Operating Voltage (1)	$V_{DD}$	3.0	3.3	3.6		V
Operating Voltage (2)	$V_{LCD}$	10.5	11.0	11.5		
Current Consumption	$I_{DD}$	---	TBD	---	$V_{DD} = 3.3 \text{ V} \pm 0.3 \text{ V}$ $V_{LCD} = 11.0 \text{ V}$	mA

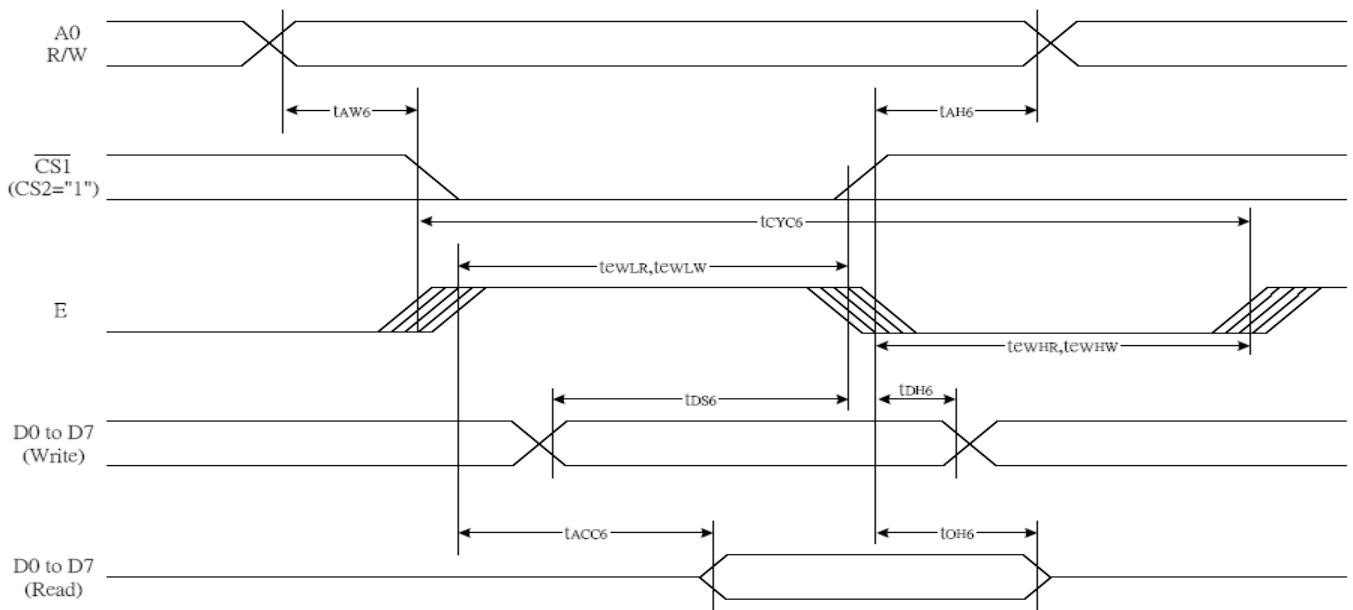
8. AC ELECTRICAL CHARACTERISTICS

8.2 System bus Read/Write characteristics for the 8080 series MPU



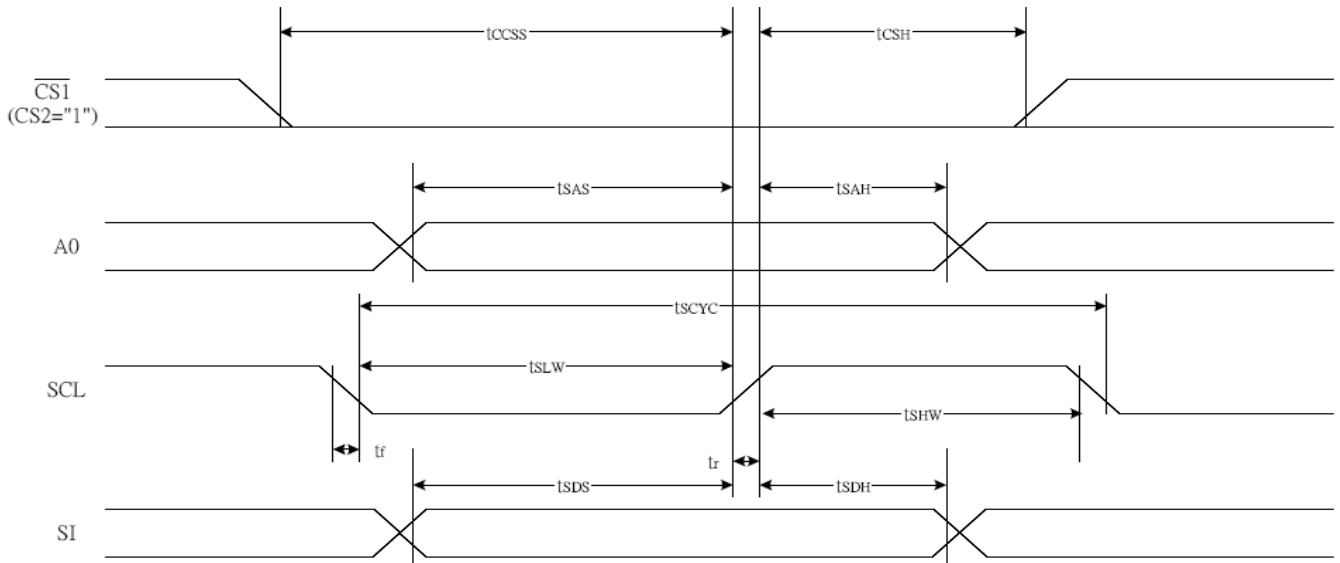
Item	Signal	Symbol	Condition	Rating		Units
				Min.	Max.	
Address hold time	A0	tAH8		0	—	Ns
Address setup time		tAW8		0	—	
System cycle time		tCYC8		240	—	
Enable L pulse width (WRITE)	WR	tCCLW		80	—	
Enable H pulse width (WRITE)		tCCHW		80	—	
Enable L pulse width (READ)	RD	tCCLR		140	—	
Enable H pulse width (READ)		tCCHR		80	—	
WRITE Data setup time	D0 to D7	tDS8		40	—	
WRITE Address hold time		tDH8		0	—	
READ access time		tACC8	CL = 100 pF	—	70	
READ Output disable time		tOH8	CL = 100 pF	5	50	

**8.2. System bus READ/WRITE characteristic for the 6800 series MPU**



Item	Signal	Symbol	Condition	Rating		Units
				Min.	Max.	
Address hold time	A0	tAH6		0	—	ns
Address setup time		tAW6		0	—	
System cycle time		tCYC6		240	—	
Enable L pulse width (WRITE)	WR	tEWLW		80	—	
Enable H pulse width (WRITE)		tEWHW		80	—	
Enable L pulse width (READ)	RD	tEWLR		80	—	
Enable H pulse width (READ)		tEWHR		140	—	
WRITE Data setup time	D0 to D7	tDS6		40	—	
WRITE Address hold time		tDH6		0	—	
READ access time		tACC6	CL = 100 pF	—	70	
READ Output disable time		tOH6	CL = 100 pF	5	50	

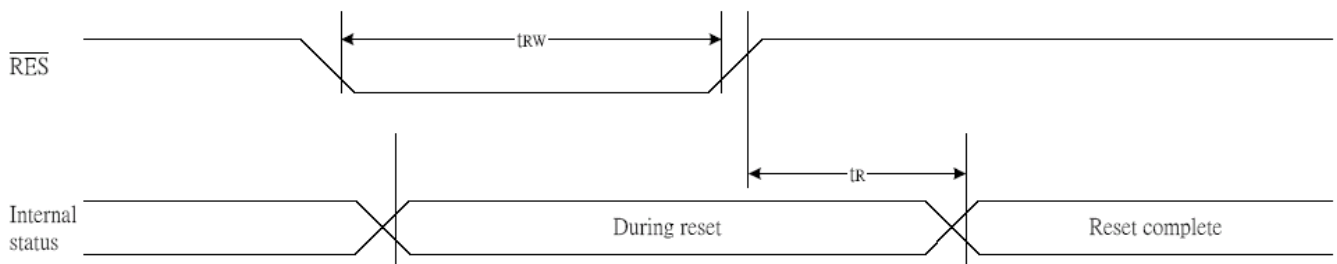
8.3. Serial Interface



Item	Signal	Symbol	Condition	Rating		Units
				Min.	Max.	
Serial Clock Period	SCL	$T_{\text{scyc}}$		50	—	ns
SCL "H" pulse width		$T_{\text{shw}}$		25	—	
SCL "L" pulse width		$T_{\text{slw}}$		25	—	
Address setup time	A0	$T_{\text{sas}}$		20	—	
Address hold time		$T_{\text{sah}}$		10	—	
Data setup time	SI	$T_{\text{sds}}$		20	—	
Data hold time		$T_{\text{sdh}}$		10	—	
CS-SCL time	CS	$T_{\text{css}}$		20	—	
CS-SCL time		$T_{\text{csh}}$		40	—	

8.4 Reset Timing

0



Item	Signal	Symbol	Condition	Rating			Units
				Min.	Typ.	Max.	
Reset time		$t_{\text{R}}$		—	—	1.0	us
Reset "L" pulse width	$\overline{\text{RES}}$	$t_{\text{RW}}$		1.0	—	—	us

**9. ABSOLUTE MAXIMUM RATINGS**

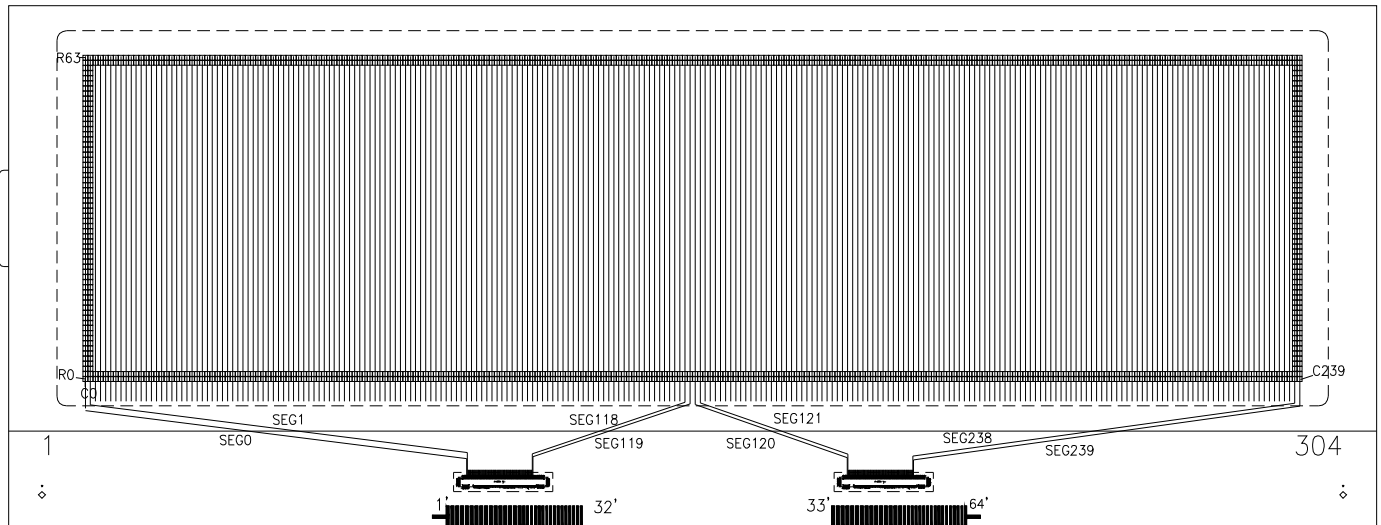
Parameter	Symbol	Conditions	Unit
Power Supply Voltage	V <sub>DD</sub>	0.3 ~ 3.6	V
Power supply voltage (V <sub>DD</sub> standard)	V <sub>DD2</sub>	0.3 ~ 3.6	V
Power supply voltage (V <sub>DD</sub> standard)	V <sub>0</sub> , V <sub>OUT</sub>	0.3 ~ 14.5	V
Power supply voltage (V <sub>DD</sub> standard)	V <sub>1</sub> , V <sub>2</sub> , V <sub>3</sub> , V <sub>4</sub>	V <sub>0</sub> to 0.3	V

## 10. COMMAND TABLE

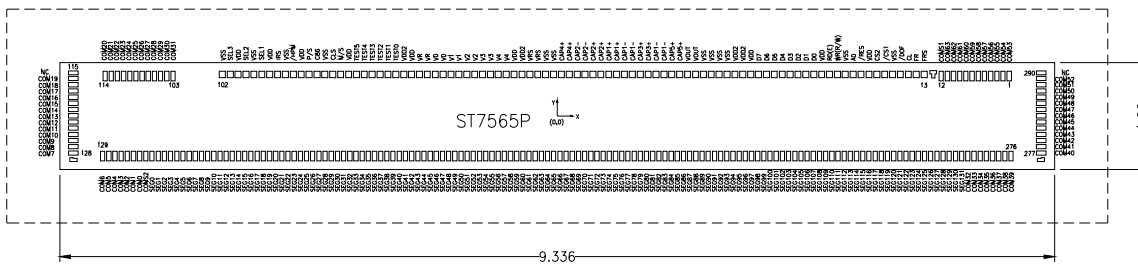
Command	Table of ST7565P Commands										Function	
	Command Code			Command Code								(Note) *: disabled data
	A0	/RD	/WR	D7	D6	D5	D4	D3	D2	D1	D0	
(1) Display ON/OFF	0	1	0	1	0	1	0	1	1	1	0	LCD display ON/OFF 0: OFF, 1: ON
(2) Display start line set	0	1	0	0	1	Display start address					0	Sets the display RAM display start line address
(3) Page address set	0	1	0	1	0	1	1	Page address				Sets the display RAM page address
(4) Column address set upper bit	0	1	0	0	0	0	1	Most significant column address				Sets the most significant 4 bits of the display RAM column address. Sets the least significant 4 bits of the display RAM column address.
Column address set lower bit	0	1	0	0	0	0	0	Least significant column address				
(5) Status read	0	0	1	Status				0	0	0	0	Reads the status data
(6) Display data write	1	1	0	Write data							Writes to the display RAM	
(7) Display data read	1	0	1	Read data							Reads from the display RAM	
(8) ADC select	0	1	0	1	0	1	0	0	0	0	0	Sets the display RAM address SEG output correspondence 0: normal, 1: reverse
(9) Display normal/reverse	0	1	0	1	0	1	0	0	1	1	0	Sets the LCD display normal/reverse 0: normal, 1: reverse
(10) Display all points ON/OFF	0	1	0	1	0	1	0	0	1	0	0	Display all points 0: normal display 1: all points ON
(11) LCD bias set	0	1	0	1	0	1	0	0	0	1	0	Sets the LCD drive voltage bias ratio 0: 1/9 bias, 1: 1/7 bias (ST7565P)
(12) Read/modify/write	0	1	0	1	1	1	0	0	0	0	0	Column address increment At write: +1 At read: 0
(13) End	0	1	0	1	1	1	0	1	1	1	0	Clear read/modify/write
(14) Reset	0	1	0	1	1	1	0	0	0	1	0	Internal reset
(15) Common output mode select	0	1	0	1	1	0	0	0	*	*	*	Select COM output scan direction 0: normal direction 1: reverse direction
(16) Power control set	0	1	0	0	0	1	0	1	Operating mode		Select internal power supply operating mode	
(17) V <sub>0</sub> voltage regulator internal resistor ratio set	0	1	0	0	0	1	0	0	Resistor ratio		Select internal resistor ratio(R <sub>b</sub> /R <sub>a</sub> ) mode	
(18) Electronic volume mode set	0	1	0	1	0	0	0	0	0	0	1	Set the V <sub>0</sub> output voltage electronic volume register
Electronic volume register set				0	0	Electronic volume value						
(19) Static indicator ON/OFF	0	1	0	1	0	1	0	1	1	0	0	0: OFF, 1: ON Set the flashing mode
Static indicator register set				0	0	0	0	0	0	0	0	
(20) Booster ratio set	0	1	0	1	1	1	1	1	0	0	0	select booster ratio 00: 2x,3x,4x 01: 5x 11: 6x
(21) Power saver												Display OFF and display all points ON compound command
(22) NOP	0	1	0	1	1	1	0	0	0	1	1	Command for non-operation
(23) Test	0	1	0	1	1	1	1	*	*	*	*	Command for IC test. Do not use this command



13. SEGMENT LAYOUT



14. IC PAD CONFIGURATION



Left

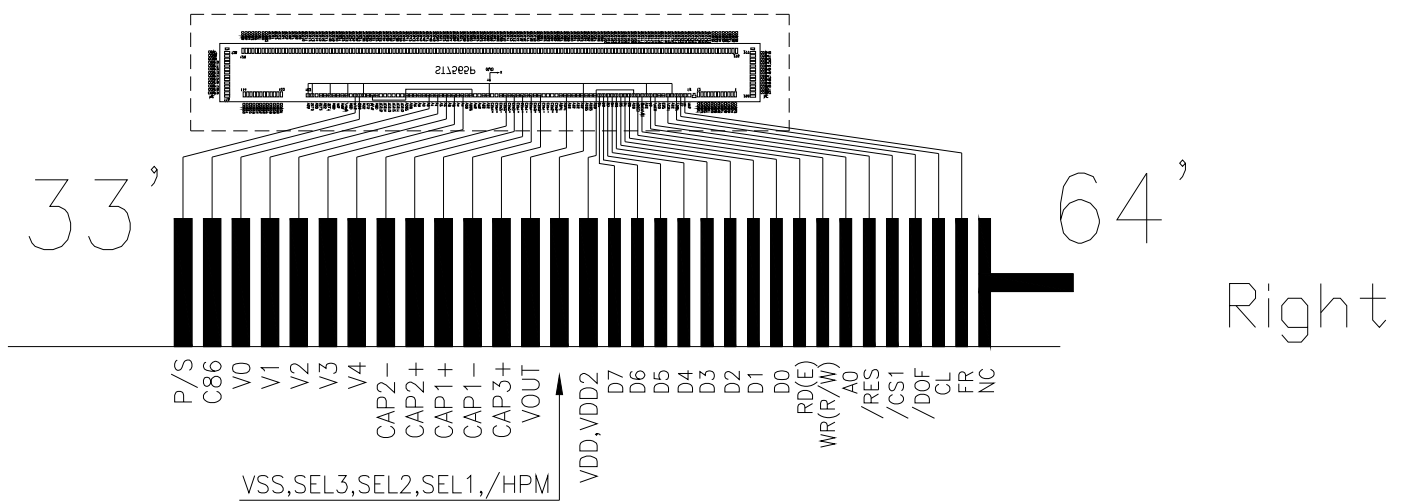
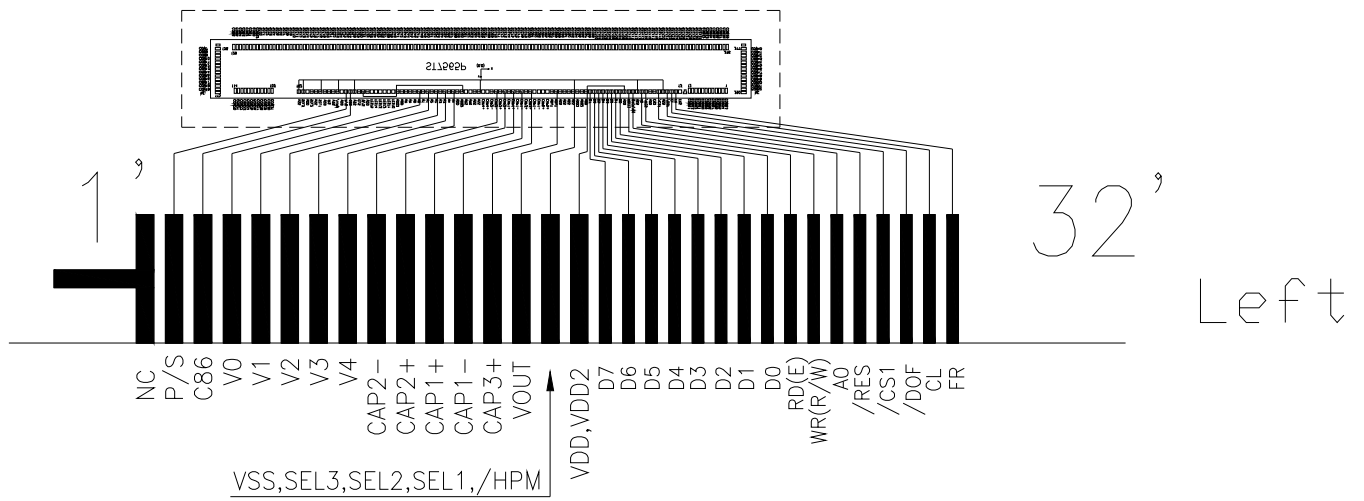
PAD NO.	CONFIGURATION	PAD NO.	CONFIGURATION
1'	NC	17'	D7
2'	P/S	18'	D6
3'	C86	19'	D5
4'	V0	20'	D4
5'	V1	21'	D3
6'	V2	22'	D2
7'	V3	23'	D1
8'	V4	24'	D0
9'	CAP2-	25'	RD(E)
10'	CAP2+	26'	WR(R/W)
11'	CAP1+	27'	A0
12'	CAP1-	28'	/RES
13'	CAP3+	29'	/CS1
14'	VOUT	30'	/DOF
	VSS,SEL3,SEL2,	31'	CL
	SEL1,/HPM	32'	FR
15'	VDD,VDD2		
16'			

Right

PAD NO.	CONFIGURATION	PAD NO.	CONFIGURATION
33'	P/S	53'	D2
34'	C86	54'	D1
35'	V0	55'	D0
36'	V1	56'	RD(E)
37'	V2	57'	WR(R/W)
38'	V3	58'	A0
39'	V4	59'	/RES
40'	CAP2-	60'	/CS1
41'	CAP2+	61'	/DOF
42'	CAP1+	62'	CL
43'	CAP1-	63'	FR
44'	CAP3+	64'	NC
45'	VOUT		
	VSS,SEL3,SEL2,		
46'	SEL1,/HPM		
47'	VDD,VDD2		
48'	D7		
49'	D6		
50'	D5		
51'	D4		
52'	D3		



15. IC LAYOUT DRAWING



**16. MODULE ACCEPT QUALITY LEVEL (AQL)**

16.1 AQL Standard Value: Fatal Defect =0.1, Major Defect=0.65; Minor Defect =2.5.

16.2 Curtailed Inspection Scheme

Type	Batch Qty	inspection Qty	AQL value	pass	Reject
module product	350PCS < 1000PCS	125pcs	0.1	0	1
			0.65	2	3
			2.5	7	8
	200PCS < 350PCS	80pcs	0.1	0	1
			0.65	1	2
			2.5	5	6
	<200PCS	32pcs	0.1	0	1
			0.65	0	1
			2.5	4	5
Module sample	<200PCS	All inspected	/	/	The sample will be reject when the fateful defect > 2pcs or main defect > 5pcs.
	>200PCS	125pcs			

- Notes:** 1). Batch QTY is the production amount that Production department ship to QA department.  
 2). All of product will be inspected if the batch QTY less than inspected QTY.  
 3). Each batch fixed to be 500pcs.

**17. RELIABILITY TEST**

Operating life time: Longer than 50000 hours (at room temperature without direct irradiation of sunlight)

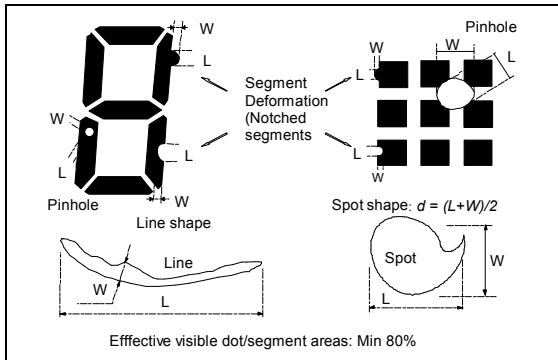
Reliability characteristics shall meet following requirements.

TEMPERATURE TESTS	NORMAL GRADE
High temperature storage	+ 90□ *96hrs
Low temperature storage	-40□* 96hrs
High temperature operation	+ 80□ *96hrs
Low temperature operation	-30□ *96hrs
High temperature, High humidity	+ 70□* 95 %RH *96hrs
Thermal shock	-30□ *30min. ← 10s ↓ 5Cycles + 80□ * 30min. →
Vibration test	Frequency *Swing * Time 40Hz * 4mm * 4hrs
Drop test	Drop height*Times 1.0m * 6times

**18. QUALITY DESCRIPTION**

**DEFECT SPECIFICATION:**

a: Table for Cosmetic defects  
 (Note: nc = not counted).  
 Sizes and number of defects  
 (Max. Qty)

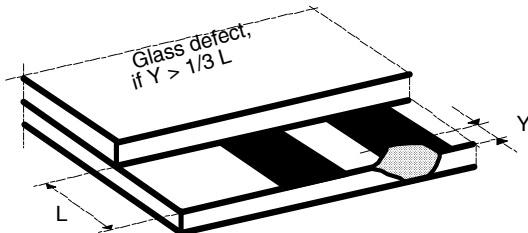


Defect Type	Max. defect size [ $\mu\text{m}$ ] d or L	Max. Quantity
Black or White Spots	$d \leq 150$	nc
	$150 < d \leq 300$	3
Black or White Lines	$W \leq 10$	nc
	$L \leq 3000$ $W \leq 30$	2
	$L \leq 2000$ $W \leq 50$	2
Pinhole	$d \leq 150$	nc
	$150 < d \leq 300$	1/segment
(Total defects)		(5)
Segment Deformation	$W \leq 100$	nc
Bubble (e.g. under pola)	$d \leq 150$	nc
	$200 < d \leq 400$	2

Examples/ Shapes

b: Glass defects

b1: Glass defects at contact ledge



b2: Glass chipping in other areas shall not be in conflict with the product's function.

**19. LCD MODULES HANDLING PRECAUTIONS**

- The display panel is made of glass. Do not subject it to a mechanical shock by dropping it from a high place, etc.
- If the display panel is damaged and the liquid crystal substance inside it leaks out, do not get any in your mouth. If the substance come into contact with your skin or clothes promptly wash it off using soap and water.
- Do not apply excessive force to the display surface or the adjoining areas since this may cause the color tone to vary.
- The polarizer covering the display surface of the LCD module is soft and easily scratched. Handle this polarize carefully.
- To prevent destruction of the elements by static electricity, be careful to maintain an optimum work environment.
  - Be sure to ground the body when handling the LCD module.
  - Tools required for assembly, such as soldering irons, must be properly grounded.
  - To reduce the amount of static electricity generated, do not conduct assembly and other work under dry conditions.
  - The LCD module is coated with a film to protect the display surface. Exercise care when peeling off this protective film since static electricity may be generated.
- Storage precautions  
When storing the LCD modules, avoid exposure to direct sunlight or to the light of fluorescent lamps. Keep the modules in bags designed to prevent static electricity charging under low temperature / normal humidity conditions (avoid high temperature / high humidity and low temperatures below 0°C). Whenever possible, the LCD modules should be stored in the same conditions in which they were shipped from our company.

**20. OTHERS**

- Liquid crystals solidify at low temperature (below the storage temperature range) leading to defective orientation of liquid crystal or the generation of air bubbles (black or white). Air bubbles may also be generated if the module is subjected to a strong shock at a low temperature.
- If the LCD modules have been operating for a long time showing the same display patterns may remain on the screen as ghost images and a slight contrast irregularity may also appear. Abnormal operating status can be resumed to be normal condition by suspending use for some time. It should be noted that this phenomena does not adversely affect performance reliability.
- To minimize the performance degradation of the LCD modules resulting from caused by static electricity, etc. exercise care to avoid holding the following sections when handling the modules :
  - Exposed area of the printed circuit board
  - Terminal electrode sections