DISPLAY Elektronik GmbH

DATA SHEET

LCD MODULE

DEM 128064S FGH-PW

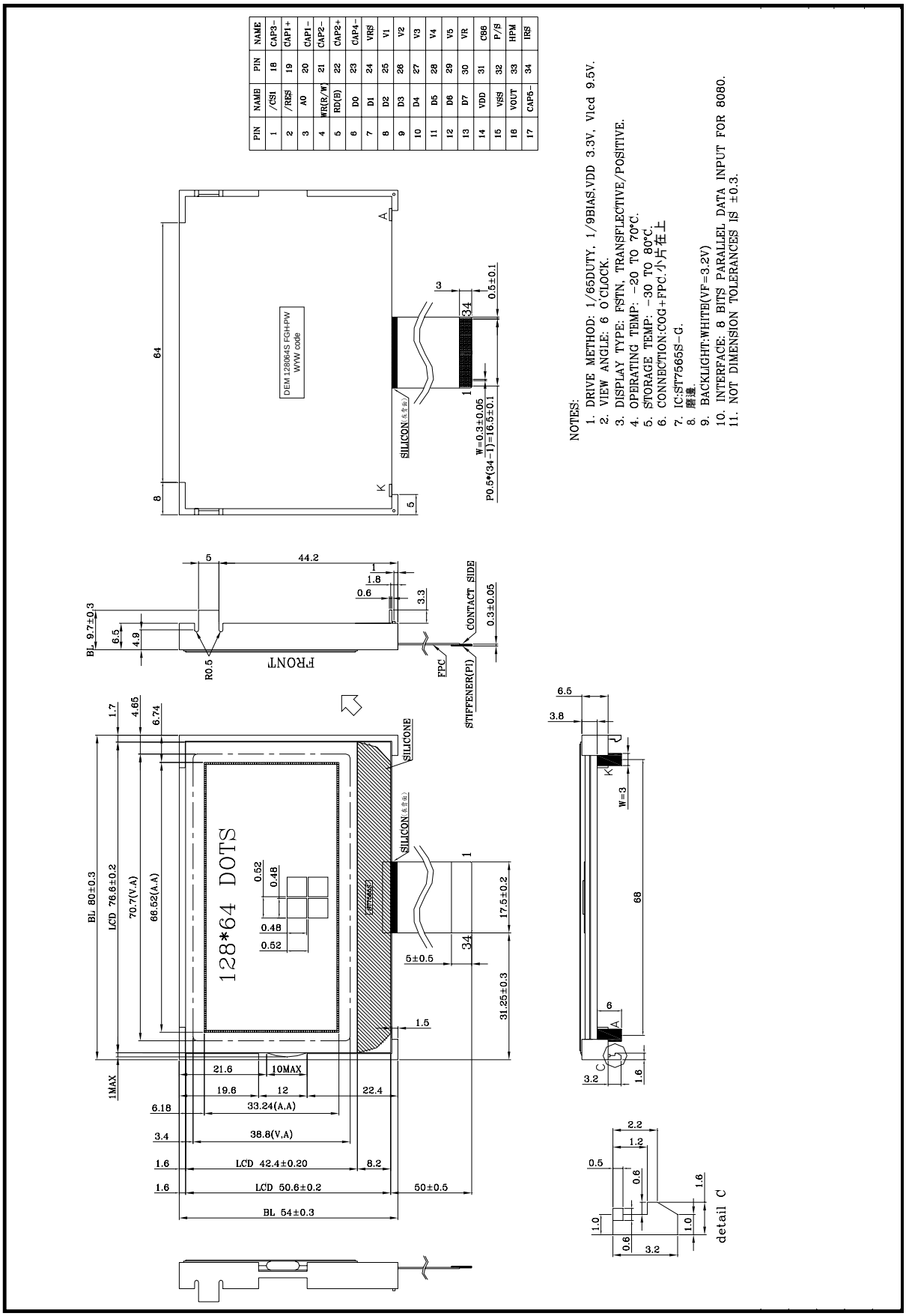
Product Specification **Version: 1**

22.02.2013

Revision Record

DATE	VER.	DESRIPTION	NOTE
07.02.2013	0	Specification released	-
22.02.2013	1	Revise Optical Characteristics	-

LCM Dimension



CONTENTS

1. PRODUCT SPECIFICATIONS

1.1 General

- 128 x 64 dot matrix LCD
- FSTN, Positive Mode
- Transflective, Wide Temperature Range
- 6 o'clock
- Backlight: Edge LED (White)
- Multiplexing Driving : 1/65duty, 1/9bias
- Controller IC: ST7565S-G (Sitronix)

1.2 Mechanical Characteristics

Item	Characteristic
Dot configuration	128 x 64
Dot dimensions(mm)	0.48 x 0.48
Dot spacing (mm)	0.52 x 0.52
Module dimensions (Horizontal × Vertical × Thickness, mm)	80.00 x 54.00 x 9.70 max.
Viewing area (Horizontal × Vertical, mm)	70.70 x 38.80
Active area (Horizontal × Vertical, mm)	66.52 x 33.24
Backlight outline dimension	80.00 x 54.00 x 9.70

1.3 Absolute Maximum Ratings (Without LED Backlight)

Characteristic	Symbol	Unit	Value
Operating Voltage (logic)	**V_{DD}**	**V**	**-0.3 to +5.0**
Input Voltage	**V_{IN}**	**V**	**-0.3 to V_{DD}+0.3**

Note 1: Referenced to V_{SS}=0V

1.4 Electrical Characteristics (Without LED Backlight)

Characteristic	Symbol	Condition	Min.	Typ.	Max.	Unit
Operating Voltage(logic)	**V_{DD}-V_{SS}**	**--**	**3.0**	**3.3**	**3.6**	**V**
Input Voltage	**V_{IH}**	**--**	**0.8V_{DD}**	**--**	**V_{DD}**	**V**
	V_{IL}	**--**	**V_{SS}**	**--**	**0.2V_{DD}**	
Output Voltage	**V_{OH}**	**I_{OH}=-0.1mA**	**0.8V_{DD}**	**--**	**V_{DD}**	**V**
	V_{HL}	**I_{OL}=0.1mA**	**V_{SS}**	**--**	**0.2V_{DD}**	
Current Consumption	**I_{DD}**	**V_{IN}=V_{DD}**	**--**	**0.05**	**1**	**mA**

1.5 Optical Characteristics Absolute Maximum Ratings

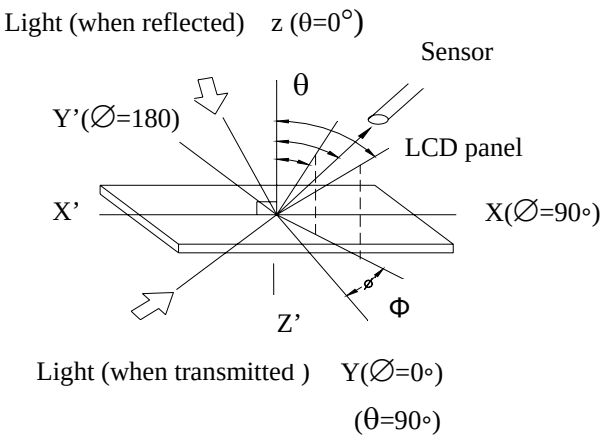
Item	Symbol	Rating	Unit
Operating temperature range	**Top**	**-20~70**	**°C**
Storage temperature range	**Tst**	**-30~80**	**°C**

1.6 Optical Characteristics

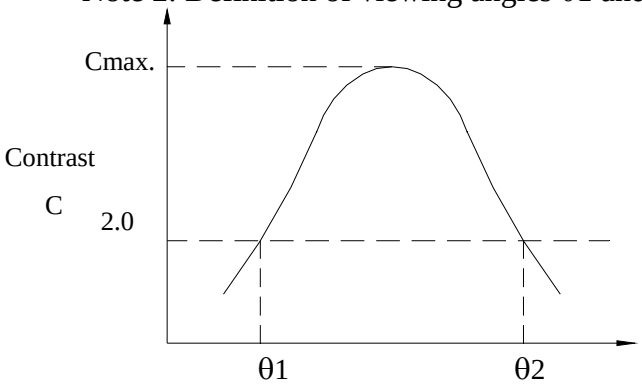
1/65 duty, 1/9bias, Vlcd=9.5V, Ta=25

Item	Symbol	Conditions	Min.	Typ.	Max	Reference
Driving voltage	Vlcd=VDD-VO		9.2	9.5	9.8	V
	Vlcd	-20°C	9.5	9.8	10.1	V
		+25°C	9.2	9.5	9.8	V
		+70°C	8.9	9.2	9.5	V
Viewing angle	θ	C≥2.0,∅=0°C	30°	-		Notes 1 & 2
Contrast	C	θ=5°, ∅=0°	3.0	--	-	Note 3
Response time(rise)	ton	θ=5°, ∅=0°	-		198ms	Note 4
Response time(fall)	toff	θ=5°, ∅=0°	-	-	176ms	Note 4

Note 1: Definition of angles θ and ∅



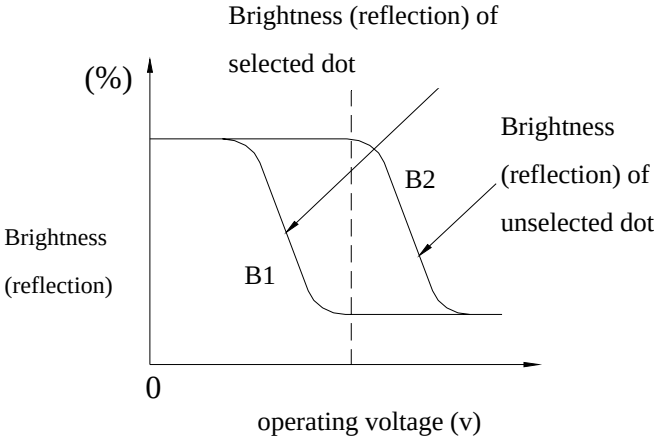
Note 2: Definition of viewing angles θ1 and ∅2



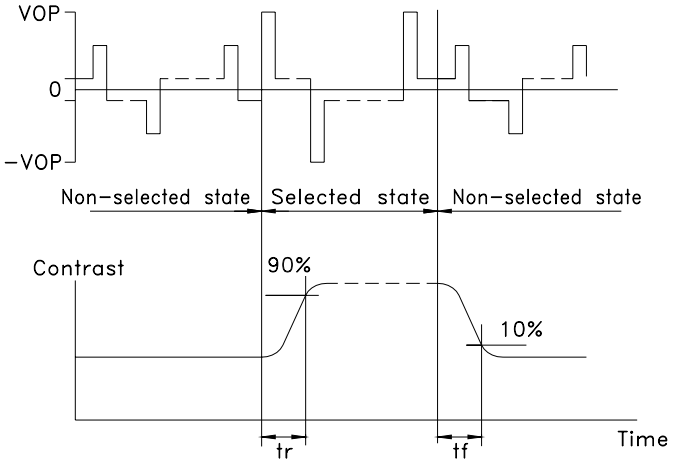
Note : Optimum viewing angle with the naked eye and viewing angle θ at Cmax. Above are not always the same

Note 3: Definition of contrast C

$$C = \frac{\text{Brightness (reflection) of unselected dot (B2)}}{\text{Brightness (reflection) of selected dot (B1)}}$$



Note 4: Definition of response time



Note: Measured with a transmissive LCD panel which is displayed 1 cm^2

V_{OPR} : Operating voltage f_{FRM} : Frame frequency

t_{ON} : Response time (rise) t_{OFF} : Response time (fall)

1.7 LED Backlight Characteristics

1.7.1 Electrical / Optical Specifications

Ta = 25°C

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Forward voltage	V_f	If=80mA, White	3.0	3.2	3.4	V
LED *****Luminous Intensity	I_V	If=80mA, White	400	450	--	Cd/m2
Chromaticity Coordinate	x	If=80mA, White	0.26	0.29	0.32	
	y		0.27	0.30	0.33	
Reverse Current	$\mathbf{I_R}$	VR=5V, White	--	--	80	uA

Note: * Measured at the bare LED Backlight Unit.

2.7.2 LED Maximum Operating Range

Item	Symbol	White	Unit
Power Dissipation	P_{AD}	340	mW
Forward Current	I_F	100	mA
Reverse Voltage	V_R	5	V

2. RELIABILITY

2.1 Reliability

Test item	Test condition	Evaluation and assessment
Operation at high temperature and humidity	40 °C±2 °C 90%RH for 500hours	No abnormalities in functions* and appearance**
Operation at high temperature	60 °C±2 °C for 500 hours	No abnormalities in functions* and appearance**
Heat shock	-20± ~ +60 °C Left for 1 hour at each temperature, transition time 5 min, repeated 10times	No abnormalities in functions* and appearance**
Low temperature	-20±2 °C for 500 hours	No abnormalities in functions* and appearance**
Vibration	Sweep for 1 min at 10 Hz, 55Hz, 10Hz, amplitude 1.5mm 2 hrs each in the X,Y and Z directions	No abnormalities in functions* and appearance**
Drop shock	Dropped onto a board from a height of 10cm	No abnormalities in functions* and appearance**

* Dissipation current, contrast and display functions

** Polarizing filter deterioration, other appearance defects

2.2 Liquid crystal panel service life

100,000 hours minimum at 25 °C±10 °C

2.3 definition of panel service life

- Contrast becomes 30% of initial value
- Current consumption becomes three times higher than initial value
- Remarkable alignment deterioration occurs in LCD cell layer
- Unusual operation occurs in display functions

3. OPERATING INSTRUCTIONS

3.1 Input Signal Function

Pin No	Symbol	I/O	Function
1	/CS1	I	This is the chip select signal. When CS1 = “L” and CS2 = “H,” then the chip select becomes active, and data/command I/O is enabled.
2	/RES	I	When RES is set to “L,” the settings are initialized. The reset operation is performed by the RES signal level.
3	A0	I	This is connect to the least significant bit of the normal MPU address bus, and it determines whether the data bits are data or a command. A0 = “H”: Indicates that D0 to D7 are display data. A0 = “L”: Indicates that D0 to D7 are control data.
4	WR(R/W)	I	• When connected to an 8080 MPU, this is active LOW. (R/W) This terminal connects to the 8080 MPU WR signal. The signals on the data bus are latched at the rising edge of the WR signal. • When connected to a 6800 Series MPU: This is the read/write control signal input terminal. When R/W = “H”: Read. When R/W = “L”: Write.
5	RD(E)	I	• When connected to an 8080 MPU, this is active LOW. (E) This pin is connected to the RD signal of the 8080 MPU, and the ST7565S series data bus is in an output status when this signal is “L”. • When connected to a 6800 Series MPU, this is active HIGH. This is the 6800 Series MPU enable clock input terminal.
6~13	D0 to D5 D6 (SCL) D7 (SI)	I/O	This is an 8-bit bi-directional data bus that connects to an 8-bit or 16-bit standard MPU data bus. When the serial interface is selected (P/S = “L”) : D0 to D5 are set to high impedance. D6 : the serial clock input (SCL) ; D7 : serial data input (SI) . When the chip select is not active, D0 to D7 are set to high impedance.
14	VDD	PS	Shared with the MPU power supply terminal Vcc.
15	VSS	PS	This is a 0V terminal connected to the system GND.
16	VOUT	O	DC/DC voltage converter. Connect a capacitor between this terminal and VSS.
17	CAP5-	O	DC/DC voltage converter. Connect a capacitor between this terminal and the CAP1+ terminal.
18	CAP3-	O	DC/DC voltage converter. Connect a capacitor between this terminal and the CAP1+ terminal.
19	CAP1+	O	DC/DC voltage converter. Connect a capacitor between this terminal and the CAP1- terminal.
20	CAP1-	O	DC/DC voltage converter. Connect a capacitor between this terminal and the CAP1+ terminal.
21	CAP2-	O	DC/DC voltage converter. Connect a capacitor between this terminal

<table>
<tr><td></td><td></td><td></td><td>and the CAP2+ terminal.</td></tr>
<tr><td>22</td><td>CAP2+</td><td>O</td><td>DC/DC voltage converter. Connect a capacitor between this terminal and the CAP2- terminal.</td></tr>
<tr><td>23</td><td>CAP4-</td><td>O</td><td>DC/DC voltage converter. Connect a capacitor between this terminal and the CAP2+ terminal.</td></tr>
<tr><td>24</td><td>VRS</td><td>PS</td><td>This is the internal-output VREG power supply for the LCD power supply
voltage regulator.</td></tr>
<tr><td>25~29</td><td>V1,V2,
V3,V4, V5</td><td>PS</td><td>This is a multi-level power supply for the liquid crystal drive. The voltage Supply applied is determined by the liquid crystal cell, and is changed through the use of a resistive voltage divided or through changing the impedance using an op.amp. Voltage levels are determined based on VDD, and must maintain the
relative magnitudes shown below.

VDD (= V0) ≧V1 ≧V2 ≧V3 ≧V4 ≧V5</td></tr>
<tr><td>30</td><td>VR</td><td>I</td><td>Output voltage regulator terminal. Provides the voltage between VDD and
V5 through a resistive voltage divider.
IRS = “L” : the V5 voltage regulator internal resistors are not used .
IRS = “H” : the V5 voltage regulator internal resistors are used .</td></tr>
<tr><td>31</td><td>C86</td><td>I</td><td>This is the MPU interface switch terminal.
C86 = “H”: 6800 Series MPU interface. C86 = “L”: 8080 MPU interface.</td></tr>
<tr><td>32</td><td>P/S</td><td>I</td><td>This is the parallel data input/serial data input switch terminal.
P/S = “H”: Parallel data input. P/S = “L”: Serial data input.
The following applies depending on the P/S status:
<table>
<tr><th>P/S</th><th>Data/Comman</th><th>Data</th><th>Read/Write</th><th>Serial Clock</th></tr>
<tr><td>“H”</td><td>A0</td><td>D0 to D7</td><td>RD, WR</td><td>X</td></tr>
<tr><td>“L”</td><td>A0</td><td>SI (D7)</td><td>Write only</td><td>SCL (D6)</td></tr>
</table>
When P/S = “L”, D0 to D5 may be “H”, “L” or Open.
RD (E) and WR (R/W) are fixed to either “H” or “L”.
With serial data input, It is impossible read data from RAM .</td></tr>
<tr><td>33</td><td>/HPM</td><td>I</td><td>This is the power control terminal for the power supply circuit for liquid crystal drive. /HPM = “H”: Normal mode /HPM = “L”: High power mode</td></tr>
<tr><td>34</td><td>IRS</td><td>I</td><td>This terminal selects the resistors for the V5 voltage level adjustment.
IRS = “H”: Use the internal resistors
IRS = “L”: Do not use the internal resistors. The V5 voltage level is regulated by an external resistive voltage divider attached to the VR terminal</td></tr>
</table>

Table 1

P/S	/CS1	CS2	A0	/RD	/WR	C86	D7	D6	D5~D0
H: Parallel Input	/CS1	CS2	A0	/RD	/WR	C86	D7	D6	D5~D0
L: Serial Input	/CS1	CS2	A0	—	—	—	SI	SCL	(HZ)

"—" indicates fixed to either "H" or to "L"

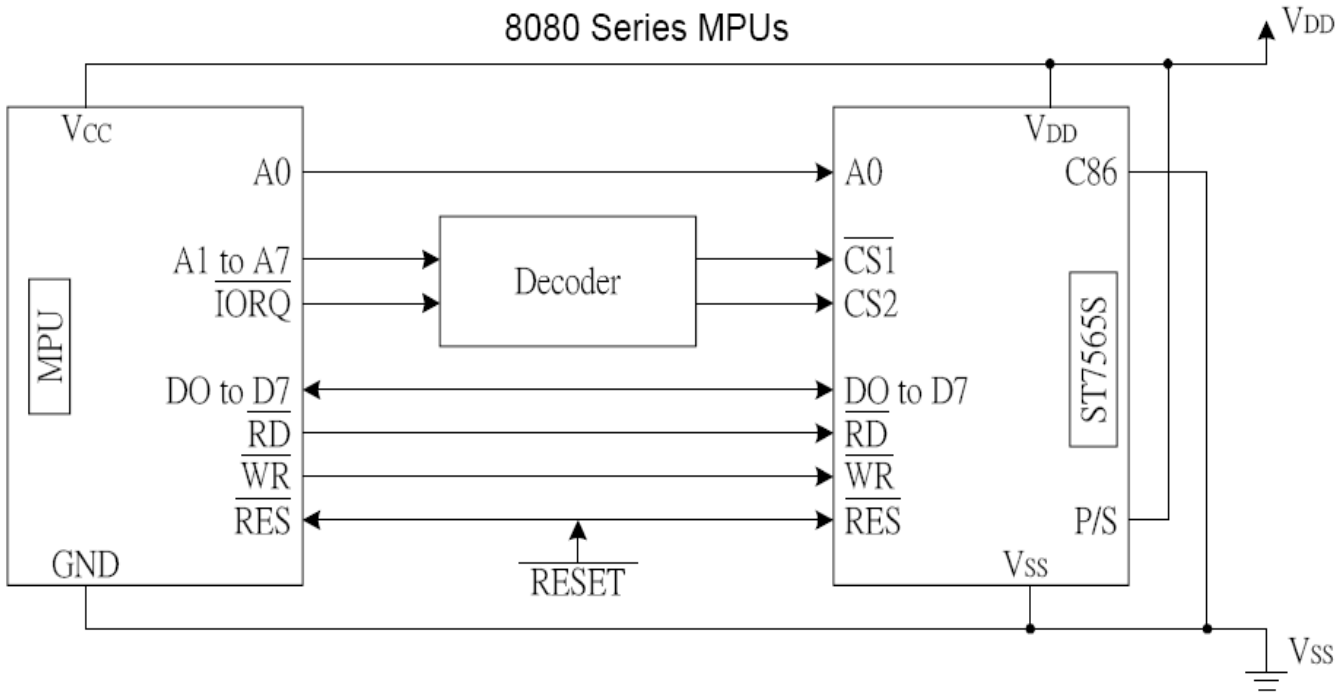
Table 2

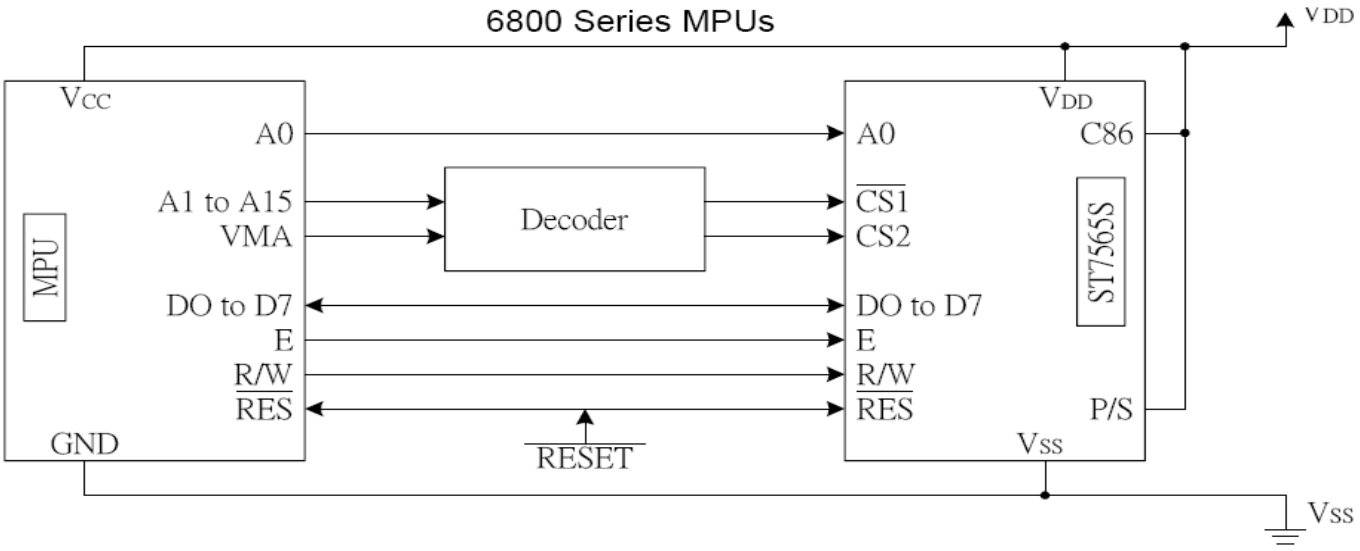
C86 (P/S=H)	/CS1	CS2	A0	E(/RD)	R/W(/WR)	D7~D0
H: 6800 Series	/CS1	CS2	A0	E	R/W	D7~D0
L: 8080 Series	/CS1	CS2	A0	/RD	/WR	D7~D0

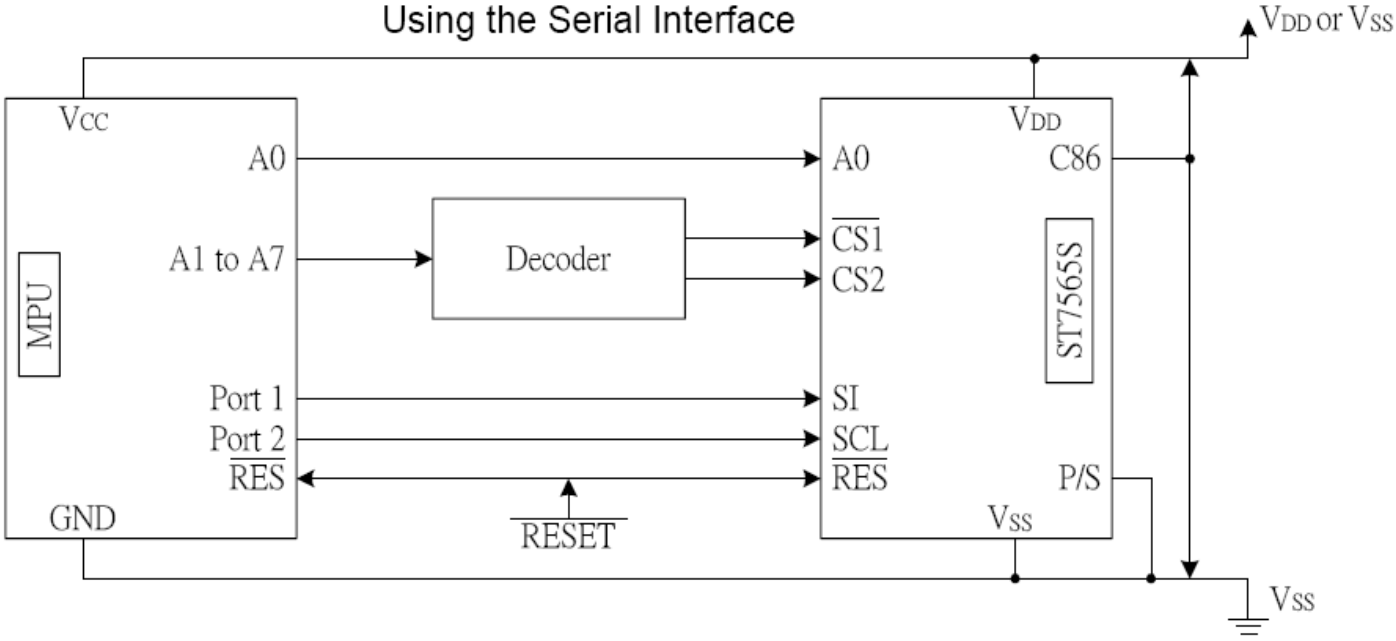
Table 3

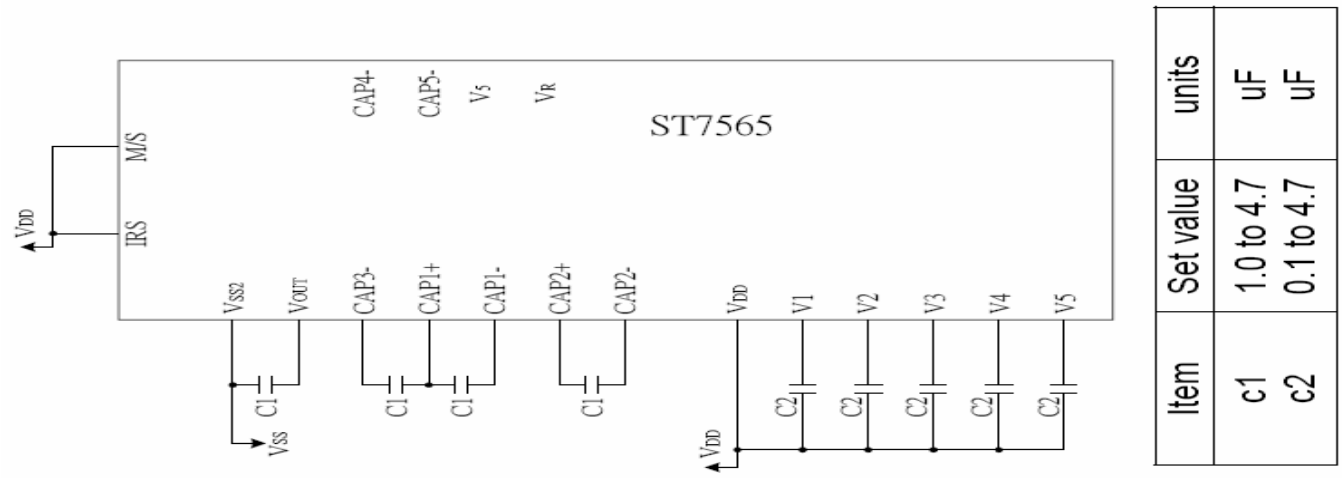
Shared	6800 Series	8080 Series		Function
A0	R/W	/RD	/WR	
1	1	0	1	Reads the display data
1	0	1	0	Writes the display data
0	1	0	1	Status read
0	0	1	0	Write control data (command)

3.2 Voltage Generator Circuit



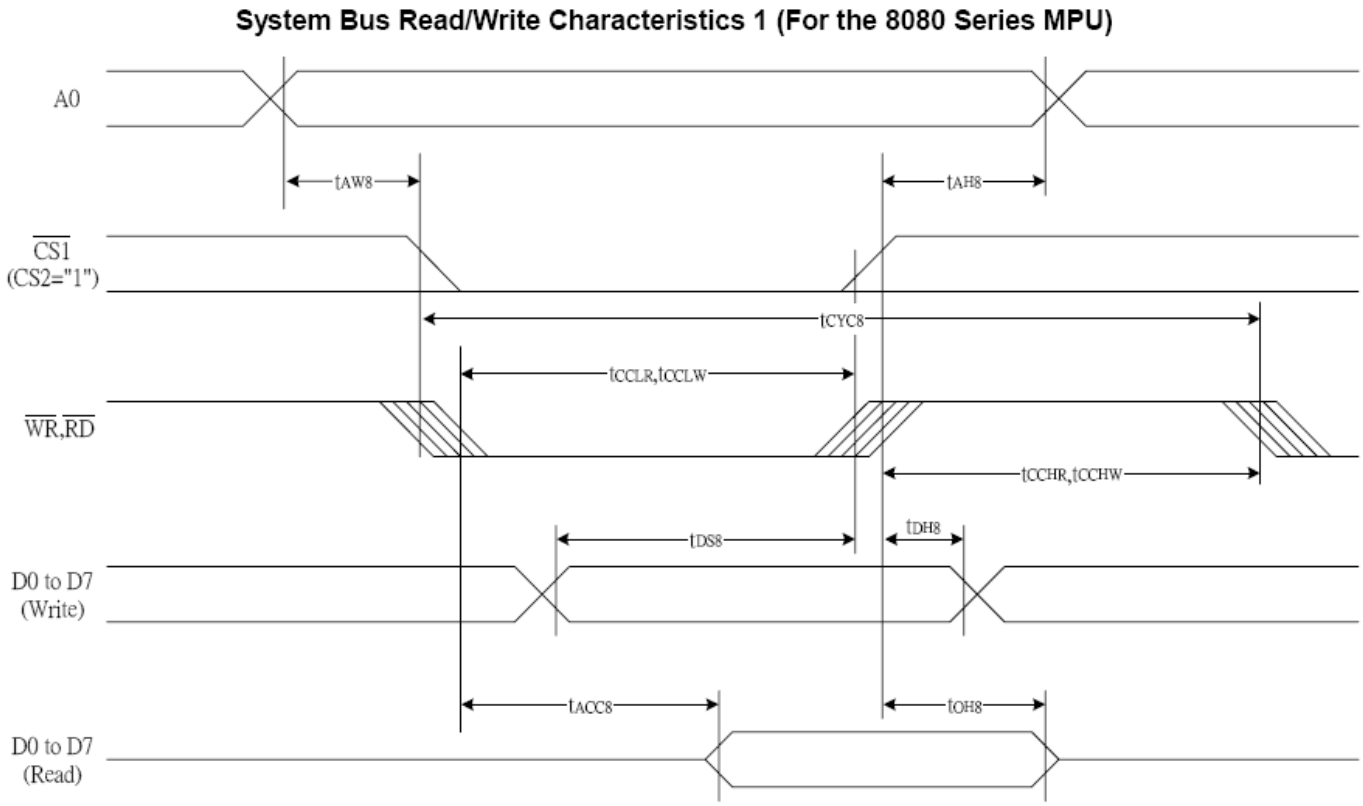




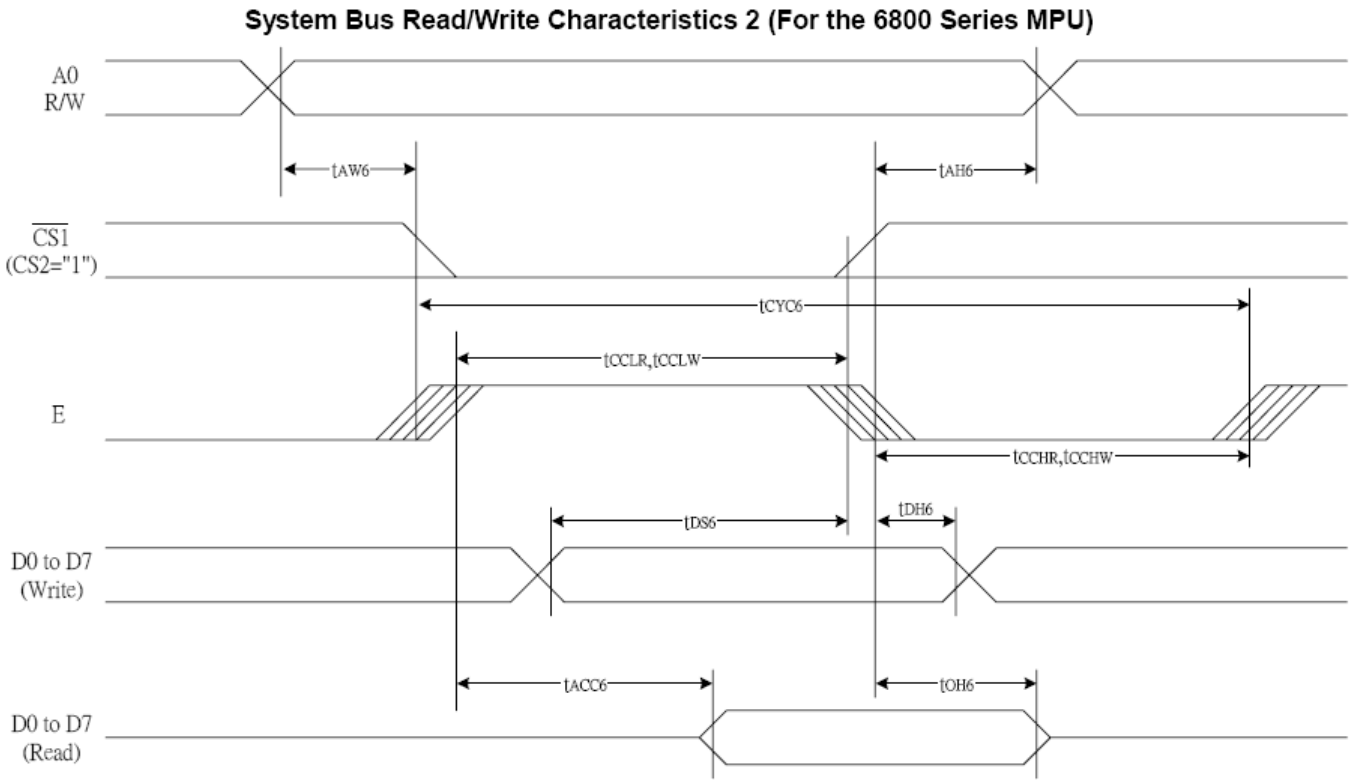


Item	Set value	units
c1	1.0 to 4.7	uF
c2	0.1 to 4.7	uF

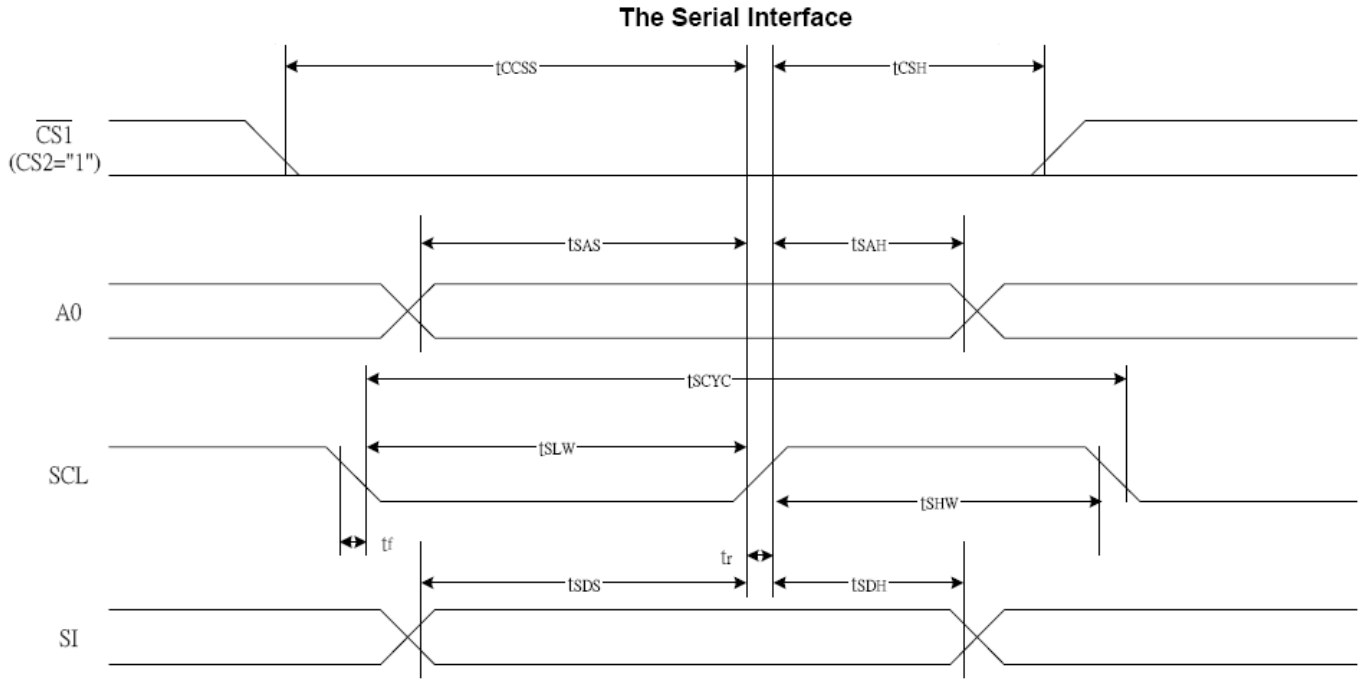
3.3 Timing Diagram



Item	Signal	Symbol	Condition	Rating		Units
				Min	Max.	
Address hold time	A0	t_{AH8}	--	0	--	ns
Address setup time		t_{AW8}		0	--	ns
System cycle time	A0	t_{CYC8}	--	240		
Control L pulse width (WR)	WR	t_{CCLW}	--	80	--	ns
Control L pulse width (RD)	RD	t_{CCLR}		140	--	ns
Control H pulse width (WR)	WR	t_{CCHW}		80	--	ns
Control H pulse width (RD)	RD	t_{CCHR}		80	--	ns
RD access time	D0 to D7	t_{DS8}	--	40	--	ns
		t_{DH8}		10	--	ns
Output disable time		t_{ACC8}	C_L=100pF	--	70	ns
		t_{OH8}		5	50	ns



Item	Signal	Symbol	Condition	Rating		Units
				Min	Max.	
Address hold time	A0	t_{AH8}	--	0	--	ns
Address setup time		t_{AW8}		0	--	ns
System cycle time	A0	t_{CYC8}	--	240		
Control L pulse width (WR)	WR	t_{CCLW}	--	80	--	ns
Control L pulse width (RD)	RD	t_{CCLR}		140	--	ns
Control H pulse width (WR)	WR	t_{CCHW}		80	--	ns
Control H pulse width (RD)	RD	t_{CCHR}		80	--	ns
RD access time	D0 to D7	t_{DS8}	--	40	--	ns
		t_{DH8}		10	--	ns
Output disable time		t_{ACC8}	C_L=100pF	--	70	ns
		t_{OH8}		5	50	ns



Item	Signal	Symbol	Condition	Rating		Units
				Min	Max.	
Serial Clock Period	SCL	Tscyc		50	--	ns
SCL “H” pulse width		Tshw		25	--	ns
SCL “L” pulse width		TSLW		25	--	ns
Address setup time	A0	TSAS		20	--	ns
Address hold time		Tsah		10	--	ns
Data setup time	SI	Tsds		20	--	ns
Data hold time		TSDH		10	--	ns
CS-SCL time	CS	Tcss		20	--	ns
CS-SCL time		Tcsh		40	--	ns

4. NOTES

Safety

- If the LCD panel breaks, be careful not to get the liquid crystal in your mouth. If the liquid crystal touches your skin or clothes, wash it off immediately using soap and plenty of water.

Handling

- Avoid static electricity as this can damage the CMOS LSI.
- The LCD panel is plate glass; do not hit or crush it.
- Do not remove the panel or frame from the module.
- The polarizing plate of the display is very fragile; handle it very carefully

Mounting and Design

- Mount the module by using the specified mounting part and holes.
- To protect the module from external pressure, leave a small gap by placing transparent plates (e.g. acrylic or glass) on the display surface, frame, and polarizing plate
- Design the system so that no input signal is given unless the power-supply voltage is applied.
- Keep the module dry. Avoid condensation, otherwise the transparent electrodes may break.

Storage

- Store the module in a dark place where the temperature is 25 ^{o}C±10 ^{o}C and the humidity below 65% RH.
- Do not store the module near organic solvents or corrosive gases.
- Do not crush, shake, or jolt the module (including accessories).

Cleaning

- Do not wipe the polarizing plate with a dry cloth, as it may scratch the surface.
- Wipe the module gently with soft cloth soaked with a petroleum benzine.
- Do not use ketonic solvents (ketone and acetoe) or aromatic solvents (toluene and xylene), as they may damage the polarizing plate.