DISPLAY Elektronik GmbH

DATA SHEET

LCD MODULE

DEM 128064Q FGH-PW

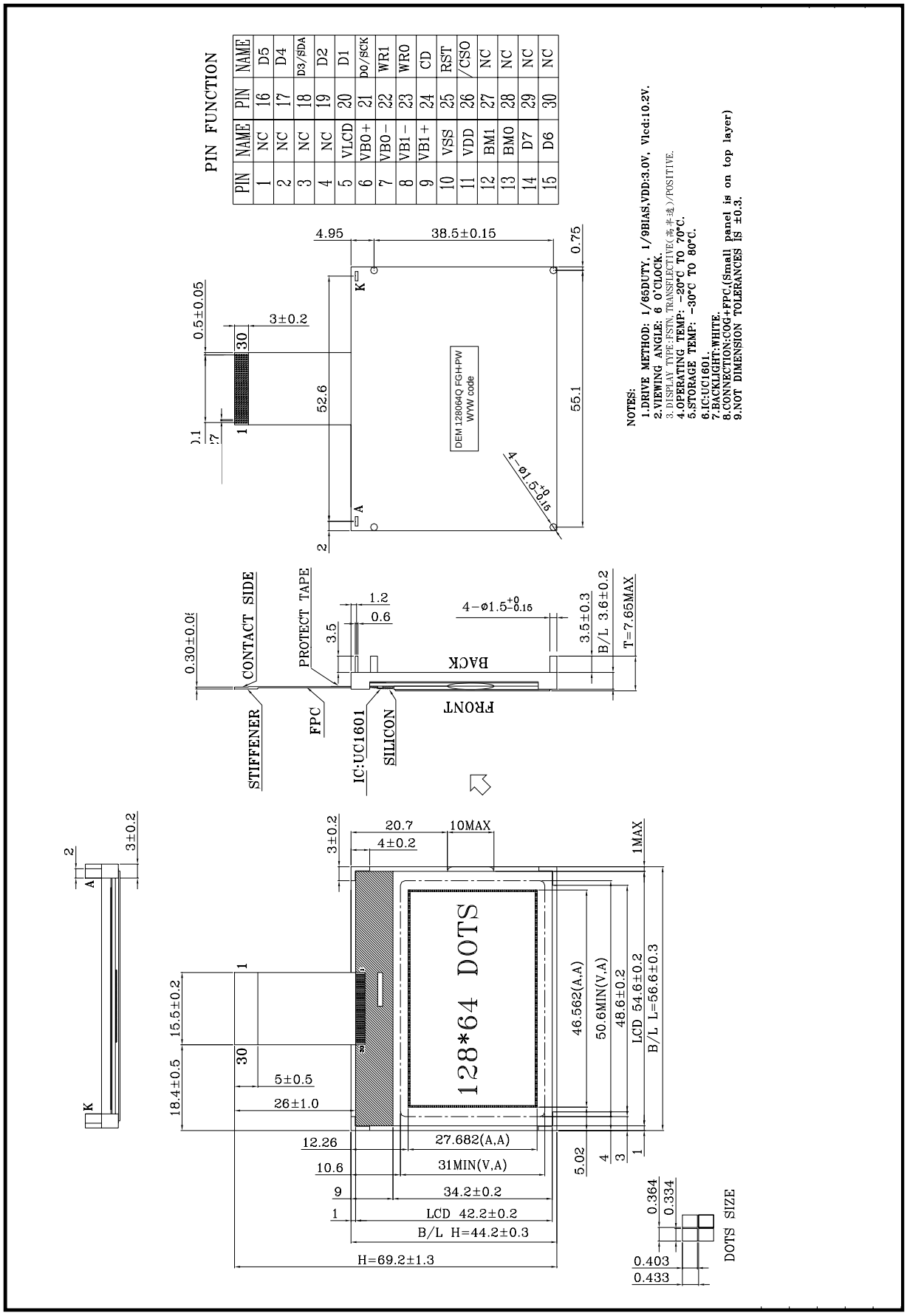
Product Specification **Version: 1**

22.02.2013

Revision Record

DATE	VER.	DESRIPTION	NOTE
07.02.2013	0	Specification released	-
22.02.2013	1	Revise Optical Characteristics	-

LCM Dimension



CONTENTS

1. PRODUCT SPECIFICATIONS

1.1 General

- 128 x 64 Dot Matrix LCD
- FSTN, Positive Mode
- Transflective, Wide Temperature Range
- 6 o'clock
- Backlight: Edge LED (WHITE)
- Multiplexing Driving : 1/65Duty, 1/9Bias
- Controller IC: UC1601 (Ultrachip)

1.2 Mechanical Characteristics

Item	Characteristic
Dot configuration	128 × 64
Dot dimensions(mm)	0.334 × 0.403
Dot spacing (mm)	0.364 × 0.433
Module dimensions (Horizontal × Vertical × Thickness, mm)	56.60 x 44.20 x 7.65 max.
Viewing area (Horizontal × Vertical, mm)	50.60 x 31.00
Active area (Horizontal × Vertical, mm)	46.562 x 27.682
Backlight outline dimension	56.60 x 44.20 x 3.60

1.3 Absolute Maximum Ratings (Without LED Backlight)

Characteristic	Symbol	Unit	Value
Operating Voltage (logic)	**V_{DD}**	**V**	**-0.3 to +4.0**
Input Voltage	**V_{IN}**	**V**	**-0.3 to V_{DD}+0.3**

Note 1: Referenced to V_{SS}=0V

1.4 Electrical Characteristics (Without LED Backlight)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{DD}	Supply for digital circuit		2.4		3.3	V
$V_{DD2/3}$	Supply for bias & pump		2.4		3.3	V
V_{LCD}	Charge pump output	$V_{DD2/3} \geq$ 2.4V, 25°C			11.5	V
V_D	LCD data voltage	$V_{DD2/3} \geq$ 2.4V, 25°C	0.80		1.32	V
V_{IL}	Input logic LOW				0.2V_{DD}	V
V_{IH}	Input logic HIGH		0.8V_{DD}			V
V_{OL}	Output logic LOW				0.2V_{DD}	V
V_{OH}	Output logic HIGH		0.8V_{DD}			V
I_{IL}	Input leakage current				1.5	µA
$R_{0(SEG)}$	SEG output impedance	V_{LCD} = 11V		2	3	kΩ
$R_{0(COM)}$	COM output impedance	V_{LCD} = 11V		2	3	kΩ
F_{FR}	Average Frame Rate	LC[3] = 0b	66	76	--	Hz

1.5 Optical Characteristics Absolute Maximum Ratings

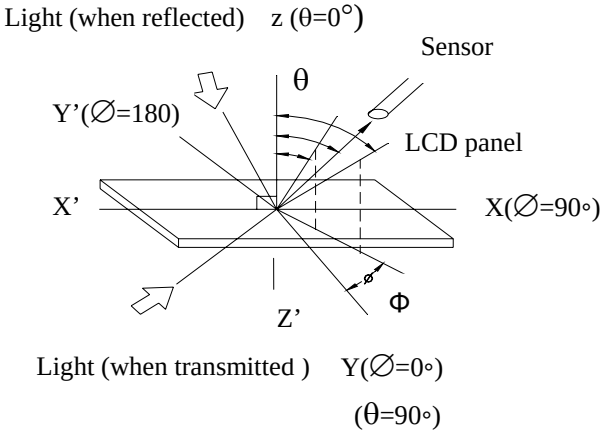
Item	Symbol	Rating	Unit
Operating Temperature Range	**Top**	**-20~+70**	**°C**
Storage Temperature Range	**Tst**	**-30~+80**	**°C**

1.6 Optical Characteristics

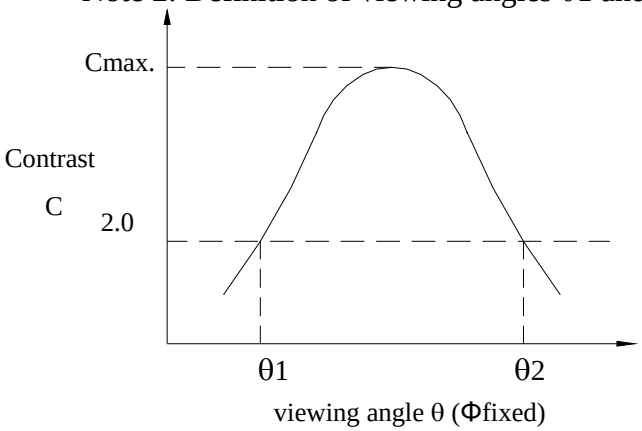
1/65 duty, 1/9bias, Vlcd=10.2V, Ta=25℃

Item	Symbol	Conditions	Min.	Typ.	Max	Reference
Driving voltage	Vlcd=VDD-VO		9.7	10.2	10.7	V
	Vlcd	-20°C	11.4	11.9	12.4	V
		+25°C	9.7	10.2	10.7	V
		+70°C	9.2	9.7	10.2	V
Viewing angle	θ	C≥2.0,∅=0°C	30°	--	--	Notes 1 & 2
Contrast	C	θ=5°, ∅=0°	3.0	--	--	Note 3
Response time(rise)	ton	θ=5°, ∅=0°	--	--	198ms	Note 4
Response time(fall)	toff	θ=5°, ∅=0°	--	--	176ms	Note 4

Note 1: Definition of angles θ and ∅



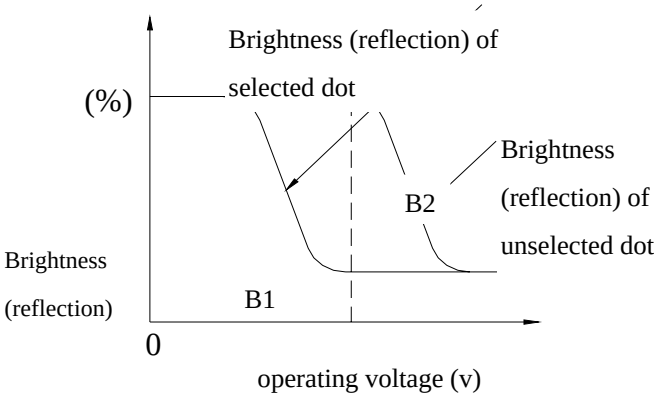
Note 2: Definition of viewing angles θ1 and ∅2



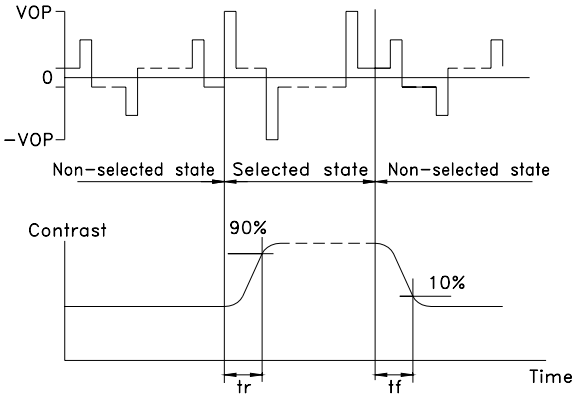
Note : Optimum viewing angle with the naked eye and viewing angle θ at Cmax. Above are not always the same

Note 3: Definition of contrast C

$$C = \frac{\text{Brightness (reflection) of unselected dot (B2)}}{\text{Brightness (reflection) of selected dot (B1)}}$$



Note 4: Definition of response time



Note: Measured with a transmissive LCD panel which is displayed 1 cm^2

V_{OPR} : Operating voltage f_{FRM} : Frame frequency

t_{ON} : Response time (rise) t_{OFF} : Response time (fall)

1.7 LED Backlight Characteristics

1.7.1 Electrical / Optical Specifications

Ta = 25°C

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Forward voltage	V_f	If=30mA, WHITE	2.8	3.0	3.2	V
LED *Luminous Intensity	I_V	If=30mA, WHITE	100	150	--	Cd/m2
Chromaticity Coordinate	x	If=30mA, WHITE	0.26	0.29	0.32	
	y		0.26	0.29	0.32	
Reverse Current	$\mathbf{I_R}$	VR=5V, WHITE	--	--	30	uA

Note: * Measured at the bare LED Backlight Unit.

1.7.2 LED Maximum Operating Range

Item	Symbol	WHITE	Unit
Power Dissipation	P_{AD}	128	mW
Forward Current	I_F	40	mA
Reverse Voltage	V_R	5	V

2. RELIABILITY

2.1 Reliability

Test item	Test condition	Evaluation and assessment
Operation at high temperature and humidity	40 °C±2 °C 90%RH for 500hours	No abnormalities in functions* and appearance**
Operation at high temperature	50 °C±2 °C for 500 hours	No abnormalities in functions* and appearance**
Heat shock	0± ~ +50 °C Left for 1 hour at each temperature, transition time 5 min, repeated 10times	No abnormalities in functions* and appearance**
Low temperature	0±2 °C for 500 hours	No abnormalities in functions* and appearance**
Vibration	Sweep for 1 min at 10 Hz, 55Hz, 10Hz, amplitude 1.5mm 2 hrs each in the X,Y and Z directions	No abnormalities in functions* and appearance**
Drop shock	Dropped onto a board from a height of 10cm	No abnormalities in functions* and appearance**

* Dissipation current, contrast and display functions

** Polarizing filter deterioration, other appearance defects

2.2 Liquid crystal panel service life

100,000 hours minimum at 25 °C±10 °C

2.3 definition of panel service life

- Contrast becomes 30% of initial value
- Current consumption becomes three times higher than initial value
- Remarkable alignment deterioration occurs in LCD cell layer
- Unusual operation occurs in display functions

3. OPERATING INSTRUCTIONS

3.1 Input Signal Function

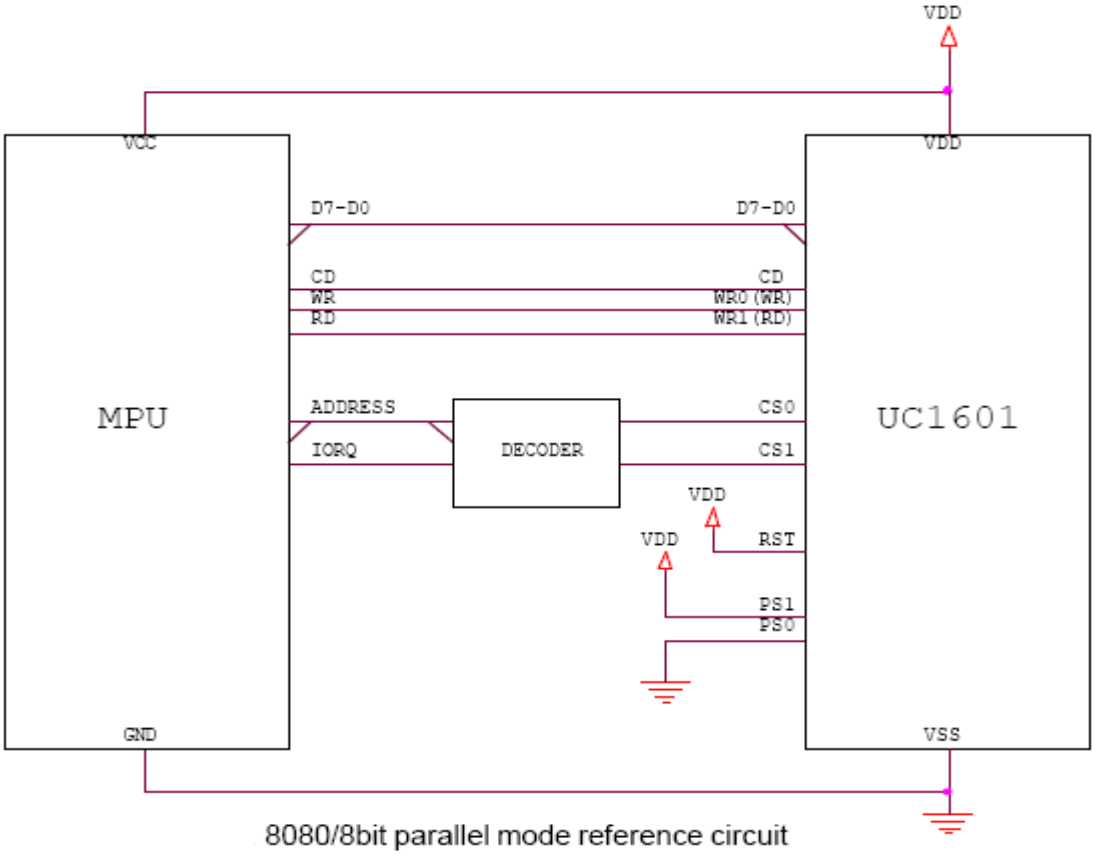
Pin No	Symbol	I/O	Function
1~4	NC	-	No Connection.
5	V_{LCD}	PWR	Main LCD power supply.
6	V_{B0+}	PWR	LCD Bias Voltages. These are the voltage sources to provide SEG driving currents. These voltages are generated internally. Connect capacitors of C_{BX} value between V_{BX+} and V_{BX-}.
7	V_{B0-}	PWR	
8	V_{B1-}	PWR	
9	V_{B1+}	PWR	
10	VSS	PWR	Power Ground.
11	VDD	PWR	Power supply terminal VCC.
12	BM1	I	Bus mode: "HL": 8080 "HH": 6800
13	BM0	I	BM[1:0] "LH": S9 "LL": S8
14	DB7	I/O	Bi-directional bus for both serial and parallel host interfaces. In serial modes, connect DB0 to SCK, DB3 to SDA.
15	DB6	I/O	
16	DB5	I/O	
17	DB4	I/O	
18	DB3/SDA	I/O	
19	DB2	I/O	
20	DB1	I/O	
21	DB0/SCK	I/O	
22	WR1	I	WR [1:0] controls the read/write operation of the host interface. See Host Interface section for details. The meaning of WR [1:0] depends on whether the interface is in the 6800 mode, or the 8080 mode. In serial modes, these two pins are not used and can be connected to Vss.
23	WR0	I	
24	CD	I	Select the incoming command if it is a control instruction or for display data. CD pin is not used in S9 mode, connect it to Vdd or Vss. "L": control instruction "H": display data
25	RST	I	When RST="L", all control registers are re-initialized by their default states.
26	/CS0	I	Chip Select or Chip Address. In parallel mode and S8 mode, chip is selected when /CS0="L". When the chip is not selected, DB[7:0] will be high impedance.
27~30	NC	-	No Connection.

	BM=1x (Parallel)	BM=0x (Serial)
D0	D0	SCK
D1	D1	
D2	D2	
D3	D3	SDA
D4	D4	
D5	D5	
D6	D6	-
D7	D7	-

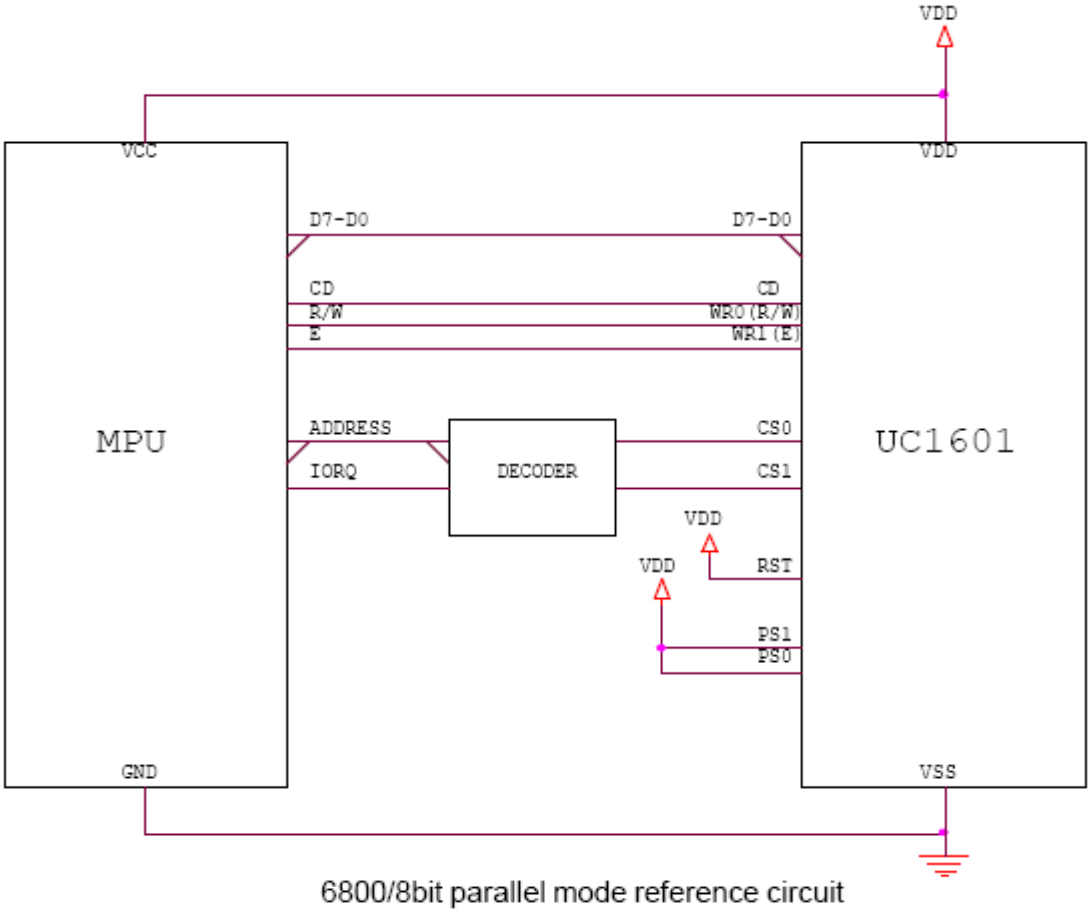
Bus Type		8080	6800	SPI (S8)	SPI (S9)
Control & Data Pins	BM[1:0]	10b	11b	00b	01b
	CS[1:0]	Chip Select			
	CD	Control/Data			–
	WR0	$\overline{WR}$	R/$\overline{W}$	–	
	WR1	$\overline{RD}$	EN	–	
	Access	Read/Write		Write Only	
	D[7:0]	8-bit bus (Tri-state)		D0=SCK, D3=SDA	

* Connect unused control pins and data bus pins to V_{DD} or Vss

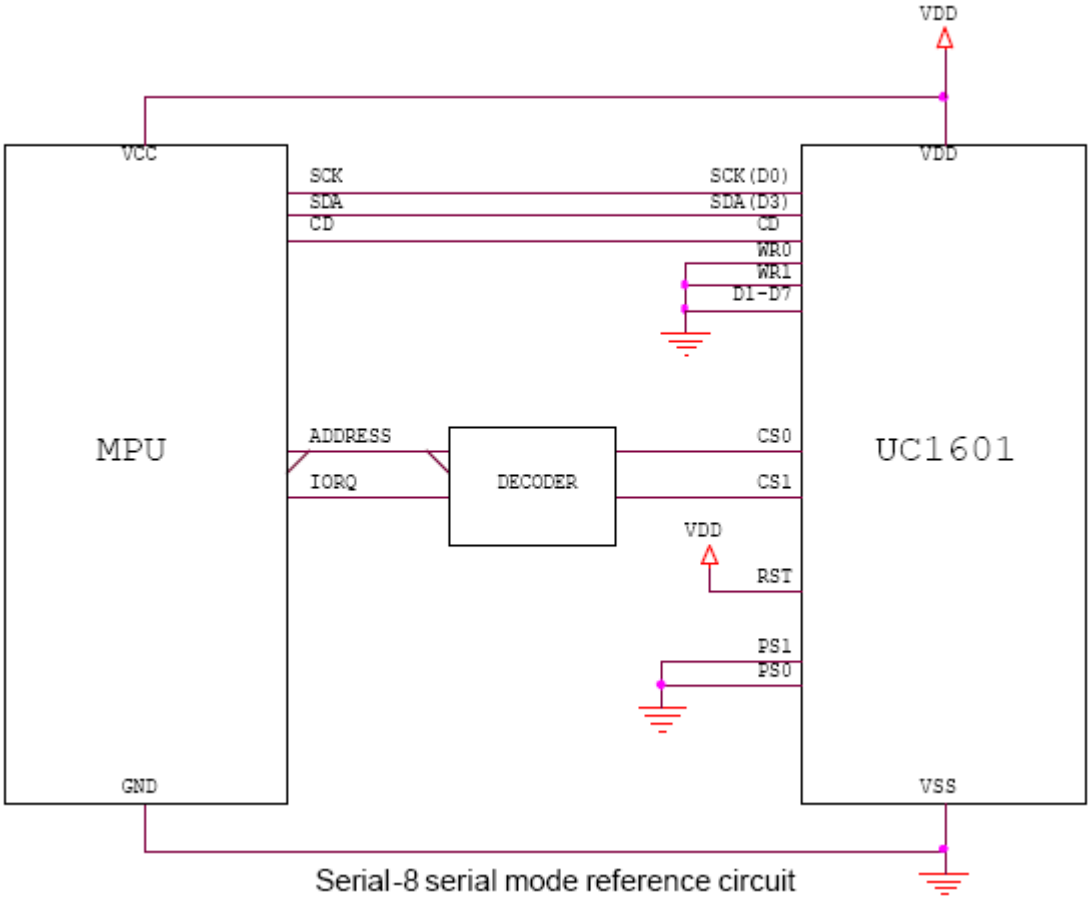
3.2 Voltage Generator Circuit



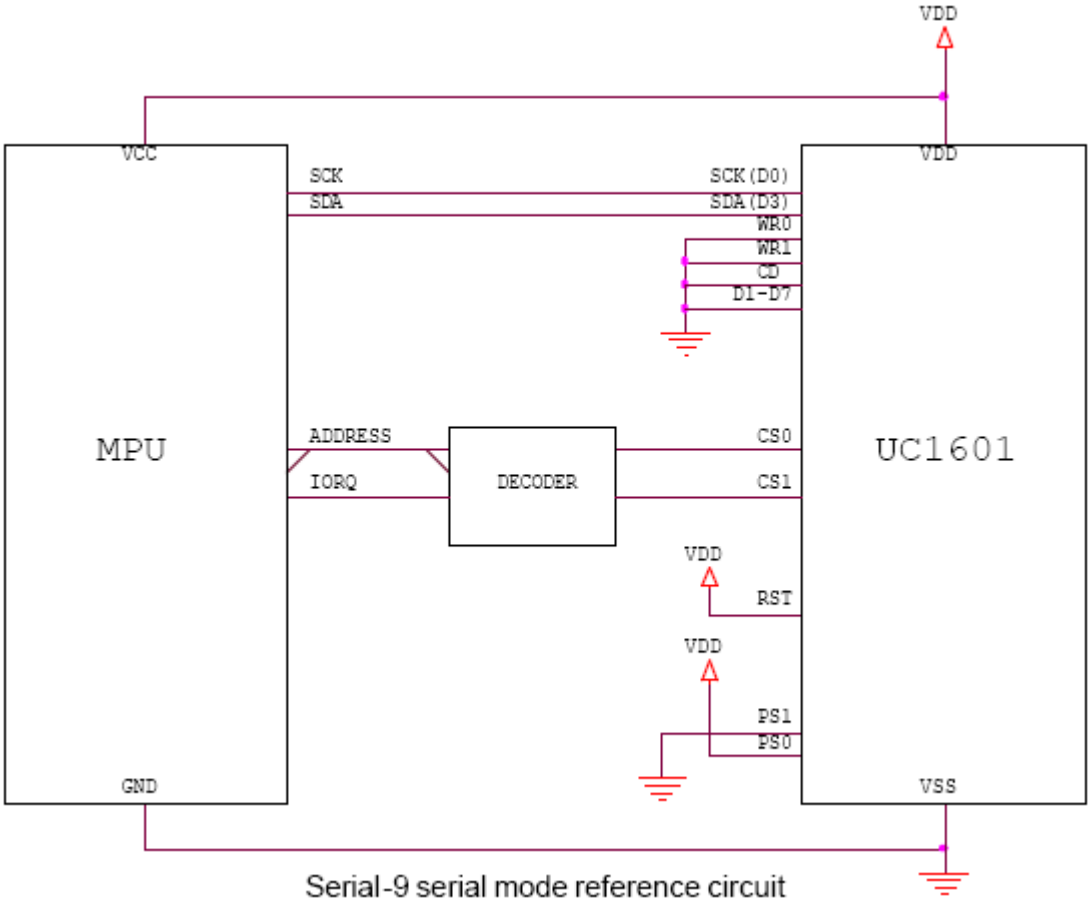
8080/8bit parallel mode reference circuit



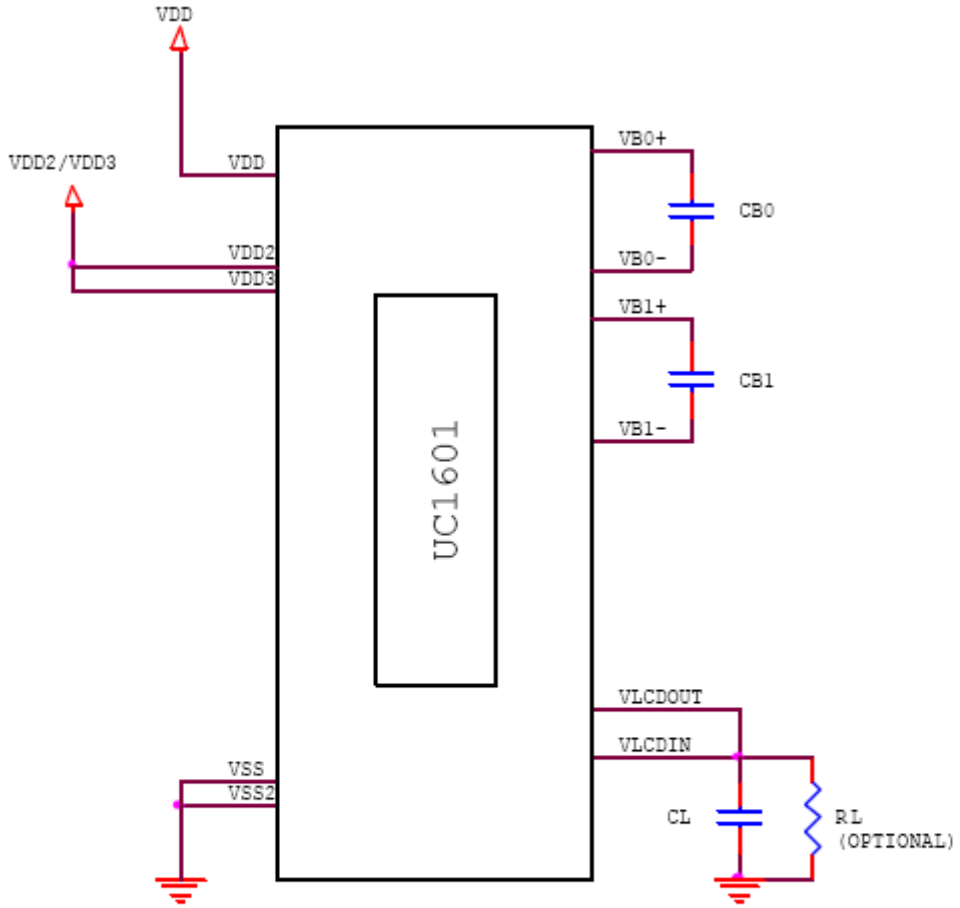
6800/8bit parallel mode reference circuit



Serial-8 serial mode reference circuit



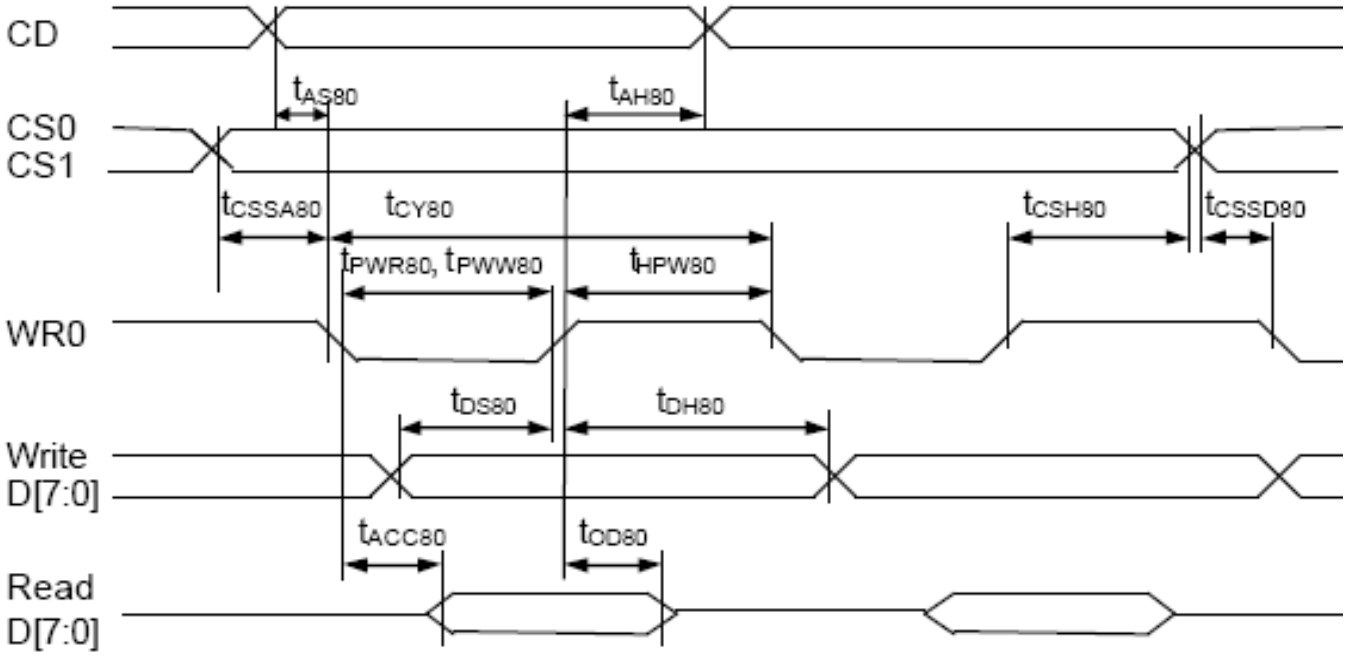
Serial-9 serial mode reference circuit



Note

- Recommended component values:
  C_B: 100x~200x LCD load capacitance or 1.0uF (2V), whichever is higher.
  C_L: 10nF ~ 30nF (25V) is appropriate for most applications.
  R_L: 10MΩ. Acts as a draining circuit when the pow er is abnormally shut down.

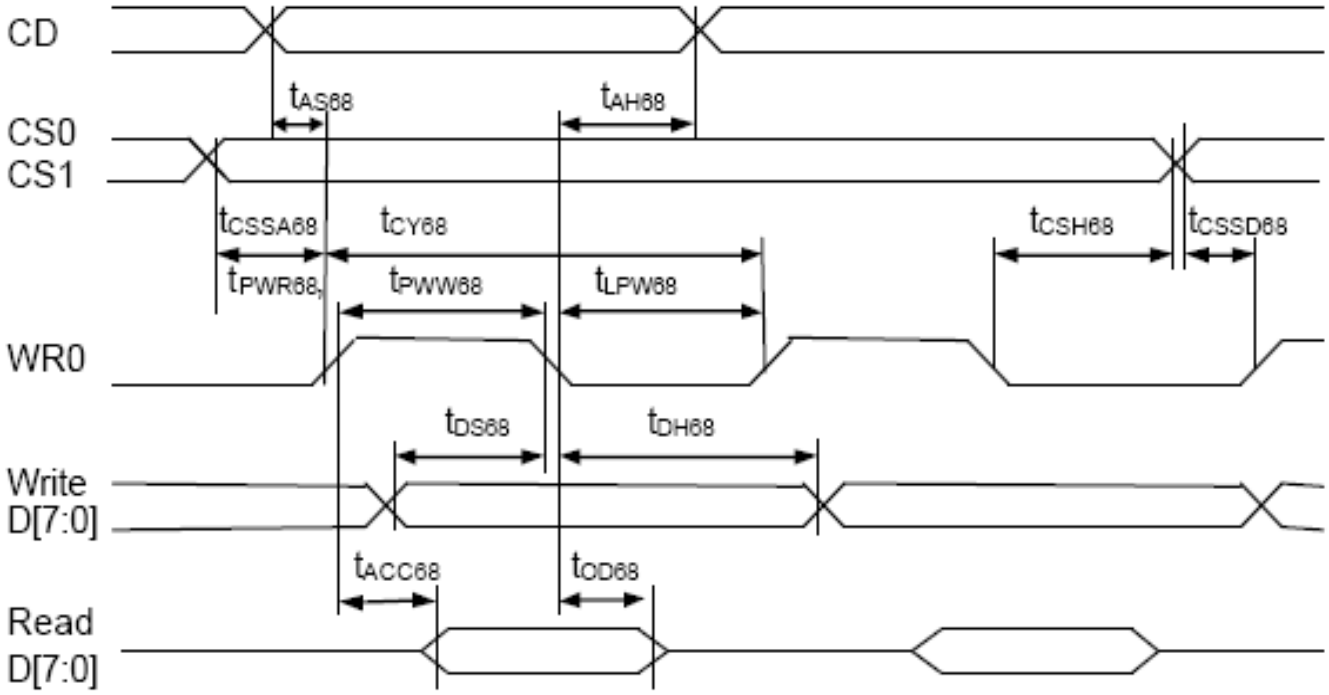
3.3 Timing Diagram



Parallel Bus Timing Characteristics (for 8080 MCU)

(2.5V ≤ V_{DD} < 3.3V, Ta= –30 to +85°C)

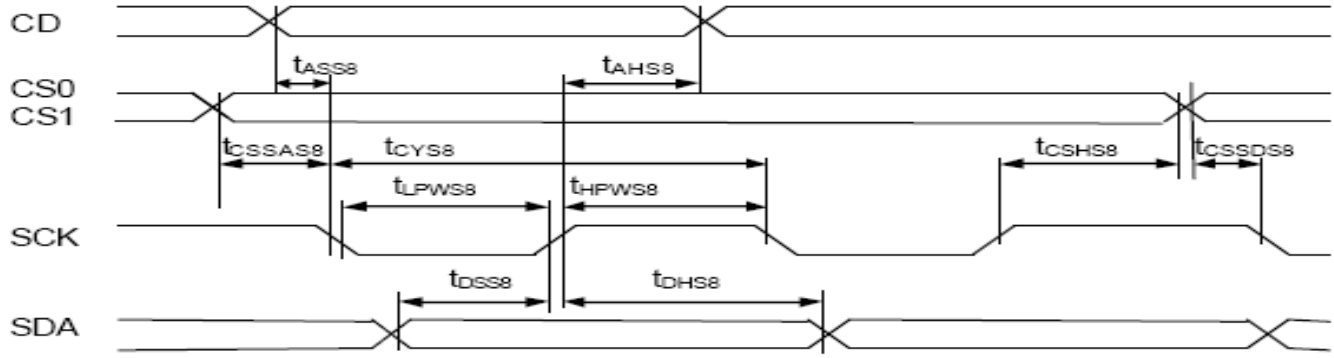
Symbol	Signal	Description	Condition	Min.	Max.	Units
t_{AS80} t_{AH80}	CD	Address setup time Address hold time		0 40	–	nS
t_{CY80}		System cycle time		135	–	nS
t_{PWR80}	WR1	Pulse width (read)		65	–	nS
t_{PWW80}	WR0	Pulse width (write)		65	–	nS
t_{HPW80} t_{DS80} t_{DH80}	WR0, WR1 D0~D7	High pulse width Data setup time Data hold time		65 30 20	– –	nS nS
t_{ACC80} t_{OD80}		Read access time Output disable time	C_L = 100pF	– 10	50 50	nS
t_{CSSA80} t_{CSSD80} t_{CSH80}	CS1/CS0	Chip select setup time		10 10 20		nS



Parallel Bus Timing Characteristics (for 6800 MCU)

(2.5V ≤ V_{DD} < 3.3V, Ta= –30 to +85°C)

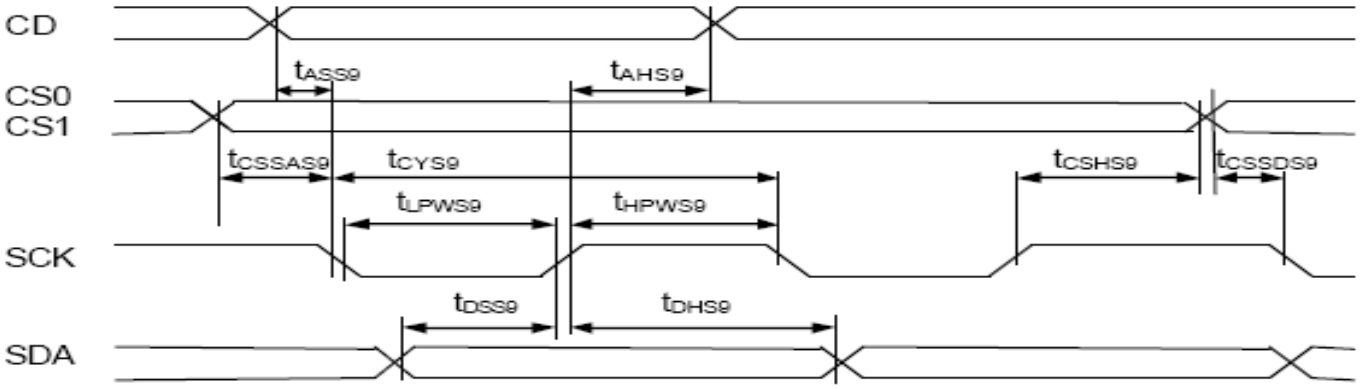
Symbol	Signal	Description	Condition	Min.	Max.	Units
t_{AS68}	CD	Address setup time		0	–	nS
t_{AH68}		Address hold time		40		
t_{CY68}		System cycle time		135	–	nS
t_{PWR68}	WR1	Pulse width (read)		65	–	nS
t_{PWW68}		Pulse width (write)		65	–	nS
t_{LPW68}		Low pulse width		65	–	nS
t_{DS68}	D0~D7	Data setup time		30	–	nS
t_{DH68}		Data hold time		15		
t_{ACC68}		Read access time	C_L = 100pF	–	50	nS
t_{OD68}		Output disable time		10	50	
T_{CSSA68}	CS1/CS0	Chip select setup time		10		nS
T_{CSSD68}				10		
T_{CSH68}				20		



Serial Bus Timing Characteristics (for S8)

(2.5V ≤ V_{DD} < 3.3V, Ta= –30 to +85°C)

Symbol	Signal	Description	Condition	Min.	Max.	Units
t_{ASS8}	CD	Address setup time		0	–	nS
t_{AHS8}		Address hold time		40	–	nS
t_{CYS8}	SCK	System cycle time		135	–	nS
t_{LPWS8}		Low pulse width		65	–	nS
t_{HPWS8}		High pulse width		65	–	nS
t_{DSS8}	SDA	Data setup time		30	–	nS
t_{DHS8}		Data hold time		15		
t_{CSSAS8}	CS1/CS0	Chip select setup time		10		nS
t_{CSSDS8}				10		
t_{CSHS8}				20		



Serial Bus Timing Characteristics (for S9)

(2.5V ≤ V_{DD} < 3.3V, Ta= –30 to +85°C)

Symbol	Signal	Description	Condition	Min.	Max.	Units
t_{ASS9}	CD	Address setup time		0	–	nS
t_{AHS9}		Address hold time		40	–	nS
t_{CYS9}	SCK	System cycle time		135	–	nS
t_{LPWS9}		Low pulse width		65	–	nS
t_{HPWS9}		High pulse width		65	–	nS
t_{DSS9}	SDA	Data setup time		30	–	nS
t_{DHS9}		Data hold time		15		
t_{CSSAS9}	CS1/CS0	Chip select setup time		10		nS
t_{CSSDS9}				10		
t_{CSHS9}				20		

4. NOTES

Safety

- If the LCD panel breaks, be careful not to get the liquid crystal in your mouth. If the liquid crystal touches your skin or clothes, wash it off immediately using soap and plenty of water.

Handling

- Avoid static electricity as this can damage the CMOS LSI.
- The LCD panel is plate glass; do not hit or crush it.
- Do not remove the panel or frame from the module.
- The polarizing plate of the display is very fragile; handle it very carefully

Mounting and Design

- Mount the module by using the specified mounting part and holes.
- To protect the module from external pressure, leave a small gap by placing transparent plates (e.g. acrylic or glass) on the display surface, frame, and polarizing plate
- Design the system so that no input signal is given unless the power-supply voltage is applied.
- Keep the module dry. Avoid condensation, otherwise the transparent electrodes may break.

Storage

- Store the module in a dark place where the temperature is 25 ^{o}C±10 ^{o}C and the humidity below 65% RH.
- Do not store the module near organic solvents or corrosive gases.
- Do not crush, shake, or jolt the module (including accessories).

Cleaning

- Do not wipe the polarizing plate with a dry cloth, as it may scratch the surface.
- Wipe the module gently with soft cloth soaked with a petroleum benzine.
- Do not use ketonic solvents (ketone and acetoe) or aromatic solvents (toluene and xylene), as they may damage the polarizing plate.